Curriculum Vitae

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1 Education

- Ph.D. in Electrical Engineering and Computer Sciences, University of California at Berkeley, 1994.
- M.S. in Electrical Engineering and Computer Sciences, University of California at Berkeley, 1991.
- B.S. in Electrical and Computer Engineering and Computer Science (double major), University of Wisconsin at Madison, 1987.

2 Employment

2.1 Academic Positions

- 2006–present: Full Professor, Dept. of Electrical and Computer Engineering, University of Maryland, College Park, MD (UMD).
- 1997–present: Joint Faculty Appointment, Institute for Advanced Computer Studies (UMIACS), UMD.
- 2001–2006: Associate Professor, Dept. of Electrical and Computer Engineering, UMD.
- 1997–2001: Assistant Professor, Dept. of Electrical and Computer Engineering, UMD.
- 1992–1994: Research Assistant, Electronics Research Laboratory, University of California, Berkeley, CA.
- 1987–1991: Research Assistant, Electronics Research Laboratory, University of California, Berkeley, CA.

2.2 Industry Positions

- 2012–2014: President and Chief Technologist, Streamlined Embedded Technologies, LLC., Ellicott City, MD.
- 1994–1997: Researcher, Semiconductor Research Laboratory, Hitachi America, San Jose, CA.
- 1991–1992: Compiler Developer, Kuck & Associates, Champaign, IL.

2.3 Visiting Positions

- 2018–2020: International Research Chair Professor (2.4 months per year appointment), Institut National Des Sciences Appliquées, and Institut National de Recherche en Informatique et en Automatique, Rennes, France, September 2018 through December 2020.
- 2015–2018: Visiting Professor, Department of Pervasive Computing, Tampere University of Technology (4 months per year appointment), Finland Distinguished Professor Programme (FiDiPro), led and financed by the Finnish funding agency Tekes, January 2015 through December 2018.
- 2009: Visiting Faculty Research Program, Air Force Research Laboratory, Rome, New York, approximately 12 weeks as a visiting researcher within the period May through December, 2009.

3 Honors and Awards

3.1 Professional Awards

- 2015–2018, FiDiPro Professor, Finland Distinguished Professor Programme, TEKES, The Finnish Funding Agency for Innovation (Finland).
- 2015, Fulbright Specialist (Austria).
- 2012, Jimmy Lin Award for Entrepreneurship, University of Maryland.
- 2011, Invention of the Year Finalist, University of Maryland.
- 2011, Fellow of the Institute of Electrical and Electronics Engineers (IEEE) "for contributions to design optimization for signal processing."
- 2009, Fulbright Specialist (Austria).
- 2006, Nokia Distinguished Lecturer (Finland).
- 2005, Fulbright Specialist (Germany).
- 1998, National Science Foundation CAREER Award.

3.2 Keynote Talks at Technical Meetings

- Conference on Design and Architectures for Signal and Image Processing, Dresden, Germany, September 27, 2017.
- ParallaX (Parallel Acceleration) Workshop, Espoo, Finland, March 26, 2015.
- IEEE Global Conference on Signal and Information Processing, Atlanta, Georgia, December 5, 2014.
- Workshop on Methods and Tools for Dataflow Programming, Madrid, Spain, October 7, 2014.
- Embedded Software Workshop, Hsinchu, Taiwan, December 27, 2013.
- International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, Samos, Greece, July 18, 2011.
- Conference on Design and Architectures for Signal and Image Processing, Edinburgh, Scotland, October 27, 2010.
- Advanced School for Computing and Imaging Conference, Lochem, The Netherlands, June 19, 2002.

3.3 Best Paper Awards

- Co-author of a paper that won the Best Student Paper Award at the *IEEE Workshop on Signal Processing Systems*, Beirut, Lebanon, October 2011. See [202] for more details.
- Co-author of a paper that won the Best Paper Award at the *International Workshop on Systems, Architectures, Modeling, and Simulation*, Samos, Greece, July 2008. See [233] for more details.
- Co-author of a paper that won the Best Student Paper Award at the *IEEE Workshop on Signal Processing Systems*, Shanghai, China, October 2007. See [238] for more details.

3.4 Student Awards

- 1987, University of California at Berkeley Regents Fellowship and Tuition Scholarship.
- 1987, Graduation with *Highest Distinction* citation from the University of Wisconsin.
- 1986, University of Wisconsin Ryan Fund Undergraduate Scholarship.

4 Publications

Books

[1] S. S. Bhattacharyya, M. Potkonjak, and S. Velipasalar, editors. *Embedded, Cyber-Physical, and IoT Systems: Essays Dedicated to Marilyn Wolf on the Occasion of Her 60th Birthday*. Springer, 2020. To appear.

[2] S. S. Bhattacharyya, E. Deprettere, R. Leupers, and J. Takala, editors. *Handbook of Signal Processing Systems*. Springer, third edition, 2019. ISBN: 978-3-319-91733-7 (Print); 978-3-319-91734-4 (Online).

[3] S. S. Bhattacharyya, E. Deprettere, R. Leupers, and J. Takala, editors. *Handbook of Signal Processing Systems*. Springer, second edition, 2013. ISBN: 978-1-4614-6858-5 (Print); 978-1-4614-6859-2 (Online).

[4] S. S. Bhattacharyya, E. Deprettere, R. Leupers, and J. Takala, editors. *Handbook of Signal Processing Systems*. Springer, 2010.

[5] S. Sriram and S. S. Bhattacharyya. *Embedded Multiprocessors: Scheduling and Synchronization*. CRC Press, second edition, 2009. ISBN:1420048015.

[6] B. Kisacanin, S. S. Bhattacharyya, and S. Chai, editors. *Embedded Computer Vision*. Springer, 2008.

[7] P. K. Murthy and S. S. Bhattacharyya. *Memory Management for Synthesis of DSP Software*. CRC Press, 2006.

[8] S. S. Bhattacharyya, E. Deprettere, and J. Teich, editors. *Domain-Specific Processors: Systems, Architectures, Modeling, and Simulation*. Marcel Dekker, Inc., 2003.

[9] S. Sriram and S. S. Bhattacharyya. *Embedded Multiprocessors: Scheduling and Synchronization*. Marcel Dekker, Inc., 2000.

[10] S. S. Bhattacharyya, P. K. Murthy, and E. A. Lee. *Software Synthesis from Dataflow Graphs*. Kluwer Academic Publishers, 1996.

Refereed Chapters in Books

[11] F. Qureshi, J. Takala, and S. Bhattacharyya. Rotators in fast Fourier transforms. In S. S. Bhattacharyya, M. Potkonjak, and S. Velipasalar, editors, *Embedded, Cyber-Physical, and IoT Systems*, pages 245–262. Springer, 2020.

[12] B. Theelen, E. F. Deprettere, and S. S. Bhattacharyya. Dynamic dataflow graphs. In S. S. Bhattacharyya, E. F. Deprettere, R. Leupers, and J. Takala, editors, *Handbook of Signal Processing Systems*, pages 1173–1210. Springer, third edition, 2019.

[13] S. S. Bhattacharyya and J. Lilius. Model-based representations for dataflow schedules. In *Principles of Modeling*, pages 88–105. Springer, 2018.

[14] E. Blasch, A. Aved, and S. S. Bhattacharyya. Dynamic data driven application systems (DDDAS) for multimedia content analysis. In E. P. Blasch, S. Ravela, and A. J. Aved, editors, *Handbook of Dynamic Data Driven Applications Systems*, pages 631–651. Springer, 2018.

[15] H. Li, Y. Liu, K. Sudusinghe, J. Yoon, E. Blasch, M. van der Schaar, and S. S. Bhattacharyya. Design of a dynamic data-driven system for multispectral video processing. In E. P. Blasch, S. Ravela, and A. J. Aved, editors, *Handbook of Dynamic Data Driven Applications Systems*, pages 529–545. Springer, 2018.

[16] S. Lin, Y. Liu, K. Lee, L. Li, W. Plishker, and S. S. Bhattacharyya. The DSPCAD framework for modeling and synthesis of signal processing systems. In S. Ha and J. Teich, editors, *Handbook of Hardware/Software Codesign*, pages 1–35. Springer, 2017.

[17] S. S. Bhattacharyya and M. Wolf. Tools and methodologies for system-level design. In L. Lavagno, I. L. Markov, G. E. Martin, and L. K. Scheffer, editors, *Electronic Design Automation for Integrated Circuits Handbook — Volume 1: EDA for IC System Design, Verification, and Testing*, pages 39–58. CRC Press, Taylor & Francis Group, second edition, 2016.

[18] S. S. Bhattacharyya, M. van der Schaar, O. Atan, C. Tekin, and K. Sudusinghe. Data-driven stream mining systems for computer vision. In B. Kisacanin and M. Gelautz, editors, *Advances in Embedded Computer Vision*, Advances in Computer Vision and Pattern Recognition, pages 249–264. Springer, 2014.

[19] H.-H. Wu, C.-C. Shen, H. Kee, N. Sane, W. Plishker, and S. S. Bhattacharyya. Mapping parameterized dataflow graphs onto FPGA platforms. In R. Chellappa and S. Theodoridis, editors, *Academic Press Library in Signal Processing*, volume 4, pages 643–673. Academic press, Elsevier Ltd., 2014.

[20] Z. Zhou, C. Shen, W. Plishker, and S. S. Bhattacharyya. Dataflow-based, cross-platform design flow for DSP applications. In A. Sangiovanni-Vincentelli, H. Zeng, M. Di Natale, and P. Marwedel, editors, *Embedded Systems Development: From Functional Models to Implementations*, volume 20 of *Embedded Systems*, pages 41–65. Springer, 2014.

[21] S. S. Bhattacharyya, E. F. Deprettere, and B. Theelen. Dynamic dataflow graphs. In S. S. Bhattacharyya, E. F. Deprettere, R. Leupers, and J. Takala, editors, *Handbook of Signal Processing Systems*, pages 905–944. Springer, second edition, 2013.

[22] C. Shen, W. Plishker, and S. S. Bhattacharyya. Dataflow-based design and implementation of image processing applications. In L. Guan, Y. He, and S. Kung, editors, *Multimedia Image and Video Processing*, pages 609–629. CRC Press, second edition, 2012. Chapter 24.

[23] W. Plishker, N. Sane, M. Kiemb, and S. S. Bhattacharyya. Heterogeneous design in functional DIF. In P. Stenström, editor, *Transactions on High-Performance Embedded Architectures and Compilers IV*, volume 6760 of *Lecture Notes in Computer Science*, pages 391–408. Springer Berlin / Heidelberg, 2011.

[24] S. S. Bhattacharyya, E. F. Deprettere, and J. Keinert. Dynamic and multidimensional dataflow graphs. In S. S. Bhattacharyya, E. F. Deprettere, R. Leupers, and J. Takala, editors, *Handbook of Signal Processing Systems*, pages 899–930. Springer, 2010.

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[26] S. S. Bhattacharyya and W. Wolf. Tools and methodologies for system-level design. In L. Scheffer, L. Lavagno, and G. Martin, editors, *Electronic Design Automation for Integrated Circuits Handbook — Volume 1: EDA for IC System Design, Verification, and Testing*, pages 3–1–3–19. Taylor & Francis Group, 2006.

[27] S. Lohani and S. S. Bhattacharyya. Goal-driven reconfiguration of polymorphous architectures. In S. S. Bhattacharyya, E. Depretter, and J. Teich, editors, *Domain-Specific Processors: Systems, Architectures, Modeling and Simulation*, pages 151–170. Marcel Dekker, Inc., 2003.

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[30] S. S. Bhattacharyya. Hardware/software co-synthesis of DSP systems. In Y. H. Hu, editor, *Programmable Digital Signal Processors: Architecture, Programming, and Applications*, pages 333–378. Marcel Dekker, Inc., 2002.

Refereed Journal Papers that Are Accepted and Awaiting Publication

[31] J. Wu, T. Blattner, W. Keyrouz, and S. S. Bhattacharyya. Model-based dynamic scheduling for multicore signal processing. *Journal of Signal Processing Systems*, 2018. To appear.

Refereed Journal Papers that Have Been Published

[32] L. Li, C. Sau, T. Fanni, J. Li, T. Viitanen, F. Christophe, F. Palumbo, L. Raffo, H. Huttunen, J. Takala, and S. S. Bhattacharyya. An integrated hardware/software design methodology for signal processing systems. *Journal of Systems Architecture*, 93:1–19, 2019.

[33] Y. Liu, L. Barford, and S. S. Bhattacharyya. Optimized implementation of digital signal processing applications with gapless data acquisition. *EURASIP Journal on Advances in Signal Processing*, 2019(19):1–13, March 2019.

[34] D. F. Noor, Y. Li, Z. Li, S. Bhattacharyya, and G. York. Multi-scale gradient image super-resolution for preserving key SIFT points in low-resolution images. *Signal Processing: Image Communication*, 78:236–245, October 2019.

[35] J. Boutellier, J. Wu, H. Huttunen, and S. S. Bhattacharyya. PRUNE: Dynamic and decidable dataflow for signal processing on heterogeneous platforms. *IEEE Transactions on Signal Processing*, 66(3):654–665, February 2018.

[36] S. Lin, J. Wu, and S. S. Bhattacharyya. Memory-constrained vectorization and scheduling of dataflow graphs for hybrid CPU-GPU platforms. *ACM Transactions on Embedded Computing Systems*, 17(2):50:1–50:25, January 2018.

[37] M. Pelcat, A. Mercat, K. Desnos, L. Maggiani, Y. Liu, J. Heulot, J.-F. Nezan, W. Hamidouche, D. Menard, and S. S. Bhattacharyya. Reproducible evaluation of system efficiency with a model of architecture: From theory to practice. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(10):2050–2063, October 2018.

[38] A. Sapio, L. Li, J. Wu, M. Wolf, and S. S. Bhattacharyya. Reconfigurable digital channelizer design using factored Markov decision processes. *Journal of Signal Processing Systems*, 90(10):1329–1343, 2018.

[39] L. Barford, S. S. Bhattacharyya, and Y. Liu. Data flow algorithms for processors with vector extensions. *Journal of Signal Processing Systems*, 87(1):21–31, April 2017.

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[41] T. Fanni, L. Li, T. Viitanen, C. Sau, R. Xie, F. Palumbo, L. Raffo, H. Huttunen, J. Takala, and S. S. Bhattacharyya. Hardware design methodology using lightweight dataflow and its integration with low power techniques. *Journal of Systems Architecture*, 78:15–29, August 2017.

[42] S. C. Kim and S. S. Bhattacharyya. Implementation of a multirate resampler for multicarrier systems on GPUs. *Journal of Signal Processing Systems*, 89(3):445–455, December 2017.

[43] H. Li, K. Sudusinghe, Y. Liu, J. Yoon, M. van der Schaar, E. Blasch, and S. S. Bhattacharyya. Dynamic, data-driven processing of multispectral video streams. *IEEE Aerospace & Electronic Systems Magazine*, 32(7):50–57, 2017.

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[48] S. C. Kim and S. S. Bhattacharyya. A wideband front-end receiver implementation on GPUs. *IEEE Transactions on Signal Processing*, 64(10):2602–2612, 2016.

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[50] S. Lin, L.-H. Wang, A. Vosoughi, J. R. Cavallaro, M. Juntti, J. Boutellier, O. Silvén, M. Valkama, and S. S. Bhattacharyya. Parameterized sets of dataflow modes and their application to implementation of cognitive radio systems. *Journal of Signal Processing Systems*, 80(1):3–18, July 2015.

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[52] I. Chukhman, S. Lin, W. Plishker, C. Shen, and S. S. Bhattacharyya. Instrumentation-driven model detection and actor partitioning for dataflow graphs. *International Journal of Embedded and Real-Time Communication Systems*, 4:1–21, June 2013.

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[54] L. Wang, C.-C. Shen, S. Wu, and S. S. Bhattacharyya. Parameterized scheduling of topological patterns in signal processing dataflow graphs. *Journal of Signal Processing Systems*, 71(3):275–286, June 2013. DOI:10.1007/s11265-012-0719-x.

[55] G. Zaki, W. Plishker, S. S. Bhattacharyya, C. Clancy, and J. Kuykendall. Integration of dataflow-based heterogeneous multiprocessor scheduling techniques in GNU radio. *Journal of Signal Processing Systems*, 70(2):177–191, February 2013. DOI:10.1007/s11265-012-0696-0.

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[58] C. Shen, S. Wu, N. Sane, H. Wu, W. Plishker, and S. S. Bhattacharyya. Design and synthesis for multimedia systems using the targeted dataflow interchange format. *IEEE Transactions on Multimedia*, 14(3):630–640, June 2012.

[59] S. S. Bhattacharyya, J. Eker, J. W. Janneck, C. Lucarz, M. Mattavelli, and M. Raulet. Overview of the MPEG reconfigurable video coding framework. *Journal of Signal Processing Systems*, 63(2):251–263, May 2011.

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[61] C. Hsu, J. Pino, and S. S. Bhattacharyya. Multithreaded simulation for synchronous dataflow graphs. *ACM Transactions on Design Automation of Electronic Systems*, 16(3):25–1–25–23, June 2011.

[62] N. Sane, H. Kee, G. Seetharaman, and S. S. Bhattacharyya. Topological patterns for scalable representation and analysis of dataflow graphs. *Journal of Signal Processing Systems*, 65(2):229–244, 2011.

[63] J. Boutellier, S. S. Bhattacharyya, and O. Silven. A low-overhead scheduling methodology for fine-grained acceleration of signal processing systems. *Journal of Signal Processing Systems*, 60(3):333–343, September 2010.

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[65] W. Plishker, O. Dandekar, S. S. Bhattacharyya, and R. Shekhar. Utilizing hierarchical multiprocessing for medical image registration. *IEEE Signal Processing Magazine*, 27(2):61–68, March 2010.

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[68] R. Gu, J. W. Janneck, S. S. Bhattacharyya, M. Raulet, M. Wipliez, and W. Plishker. Exploring the concurrency of an MPEG RVC decoder based on dataflow program analysis. *IEEE Transactions on Circuits and Systems for Video Technology*, 19(11):1646–1657, November 2009.

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[73] S. Saha, S. Puthenpurayil, J. Schlessman, S. S. Bhattacharyya, and W. Wolf. The signal passing interface and its application to embedded implementation of smart camera applications. *Proceedings of the IEEE*, 96(10):1576–1587, October 2008. Invited paper.

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[76] C. Hsu, M. Ko, S. S. Bhattacharyya, S. Ramasubbu, and J. L. Pino. Efficient simulation of critical synchronous dataflow graphs. *ACM Transactions on Design Automation of Electronic Systems*, 12(3):21, 2007. 28 pages.

[77] S. Hua, G. Qu, and S. S. Bhattacharyya. Probabilistic design of multimedia embedded systems. *ACM Transactions on Embedded Computing Systems*, 6(3):15, 2007. 24 pages.

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[80] M. Sen, I. Corretjer, F. Haim, S. Saha, J. Schlessman, T. Lv, S. S. Bhattacharyya, and W. Wolf. Dataflow-based mapping of computer vision algorithms onto FPGAs. *EURASIP Journal on Embedded Systems*, 2007:Article ID 49,236, 12 pages, 2007. Doi:10.1155/2007/49236.

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Refereed Abstracts and Extended Abstracts Presented at Conferences and Workshops

[324] L. Li, Z. Li, Y. Liy, B. Kathariya, and S. Bhattacharyya. Gradual deep neural network pruning based on Hessian approximation. In *Proceedings of the Data Compression Conference*. Snowbird, Utah, March 2019. To appear.

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[335] C. Hsu and S. S. Bhattacharyya. Integrating VSIPL support in the dataflow interchange format. In *Proceedings of the Annual Workshop on High Performance Embedded Computing*, pages 75–76. Lexington, Massachusetts, September 2005.

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[337] N. Bambha and S. S. Bhattacharyya. Optically-connected multiprocessors for rapidly training a neural network. In *Proceedings of the Army Science Conference*. Orlando, Florida, December 2002. Extended abstract in online proceedings, 2 pages.

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[339] H. N. Tran, S. S. Bhattacharyya, J.-P. Talpin, and T. Gautier. Toward efficient many-core scheduling of partial expansion graphs. In *Proceedings of the International Workshop on Software and Compilers for Embedded Systems*, pages 100–103. Sankt Goar, Germany, May 2018. Invited paper.

[340] K. Lee, H. Ben Salem, T. Damarla, W. Stechele, and S. S. Bhattacharyya. Prototyping real-time tracking systems on mobile devices. In *Proceedings of the ACM International Conference on Computing Frontiers*, pages 301–308. Como, Italy, May 2016. Invited paper.

[341] W. Plishker, C. Shen, S. S. Bhattacharyya, G. Zaki, S. Kedilaya, N. Sane, K. Sudusinghe, T. Gregerson, J. Liu, and M. Schulte. Model-based DSP implementation on FPGAs. In *Proceedings of the International Symposium on Rapid System Prototyping*. Fairfax, Virginia, June 2010. Invited paper, DOI 10.1109/RSP_2010.SS4, 7 pages.

[342] H. Wu, C. Shen, S. S. Bhattacharyya, K. Compton, M. Schulte, M. Wolf, and T. Zhang. Design and implementation of real-time signal processing applications on heterogeneous multiprocessor arrays. In *Proceedings of the IEEE Asilomar Conference on Signals, Systems, and Computers*, pages 2121–2125. Pacific Grove, California, November 2010. DOI:10.1109/ACSSC.2010.5757924. Invited paper.

[343] A. Gregerson, A. Farmahini-Farahani, W. Plishker, Z. Xie, K. Compton, S. Bhattacharyya, and M. Schulte. Advances in architectures and tools for FPGAs and their impact on the design of complex systems for particle physics. In *Proceedings of the Topical Workshop on Electronics for Particle Physics*, pages 617–626. Paris, France, September 2009. Invited paper.

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[345] Y. Hemaraj, M. Sen, R. Shekhar, and S. S. Bhattacharyya. Model-based mapping of image registration applications onto configurable hardware. In *Proceedings of the IEEE Asilomar Conference on Signals, Systems, and Computers*, pages 1453–1457. Pacific Grove, California, October 2006. Invited paper.

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[347] S. S. Bhattacharyya, N. Bambha, M. Khandelia, and V. Kianzad. Mapping DSP applications onto self-timed multiprocessors. In *Proceedings of the IEEE Asilomar Conference on Signals, Systems, and Computers*, volume 1, pages 441–448. Pacific Grove, California, November 2001. Invited paper.

Other Non-refereed Articles

[348] S. Ha, J. Teich, C. Haubelt, M. Glaß, T. Mitra, R. Dömer, P. Eles, A. Shrivastava, A. Gerstlauer, and S. S. Bhattacharyya. Introduction to hardware/software codesign. In S. Ha and J. Teich, editors, *Handbook of Hardware/Software Codesign*, pages 1–24. Springer, 2017.

5 Theses Supervised

Ph.D. Theses Supervised as Chair

[349] K. Lee. *Design Optimization of Embedded Signal Processing Systems for Target Detection*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2018.

[350] L. Li. *Design Space Exploration for Signal Processing Systems using Lightweight Dataflow Graphs*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2018.

[351] Y. Liu. *Model-Based Design and Implementation of Deep Waveform Analysis Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2018.

[352] S. Lin. *Modeling and Software Synthesis for Multiprocessor Implementation of Wireless Communication Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2016.

[353] I. Chukhman. *Profile- and Instrumentation-Driven Methods for Embedded Signal Processing*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2015.

[354] S. C. Kim. *Baseband Radio Modem Design using Graphics Processing Units*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2015.

[355] K. Sudusinghe. *Design Tools for Dynamic, Data-Driven, Stream Mining Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2015.

[356] I. Cho. *Hardware and Software Architectures for Energy- and Resource-Efficient Signal Processing Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2014.

[357] L. Wang. *Hierarchical Mapping Techniques for Signal Processing Systems on Parallel Platforms*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2014.

[358] H.-H. Wu. *Modeling and Mapping of Optimized Schedules for Embedded Signal Processing Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2013.

[359] G. Zaki. *Scalable Techniques for Scheduling and Mapping DSP Applications onto Embedded Multiprocessor Platforms*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2013.

[360] Z. Zhou. *Multi-Scale Scheduling Techniques for Signal Processing Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2013.

[361] N. Sane. *Rapid Prototyping of High Performance Signal Processing Applications*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2011.

[362] R. Gu. *Modeling and Optimization Techniques for Efficient Implementation of Parallel Embedded Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2010.

[363] H. Kee. *Systematic Exploration of Trade-offs between Application Throughput and Hardware Resource Requirements in DSP Systems*. Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2010.

[364] C. Shen. *Energy-driven Optimization of Hardware and Software for Distributed Embedded Systems.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2008.

[365] C. Hsu. *Dataflow Integration and Simulation Techniques for DSP System Design tools.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, April 2007.

[366] S. Saha. *Design Methodology for Embedded Computer Vision Systems.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2007.

[367] V. Kianzad. *System Synthesis for Embedded Multiprocessors.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2006.

[368] D. Ko. *System Synthesis for Image Processing Applications.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2006.

[369] M. Ko. *Integrated Software Synthesis for Signal Processing Applications.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2006.

[370] M. Sen. *Model-based Hardware Design for Image Processing Systems.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2006.

[371] N. K. Bambha. *Communication-driven Codesign for Multiprocessor Systems.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2004.

[372] N. Chandrachoodan. *Performance Analysis and Hierarchical Timing for DSP System Synthesis.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, August 2002.

Ph.D. Theses Supervised as Co-Advisor

[373] O. Dandekar. *High-performance 3D Image Processing Architectures for Image-guided Interventions.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2008.

[374] G. Spivey. *Logic Foundry: A Design Environment for the Rapid Prototyping of FPGA-based DSP Systems.* Ph.D. thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, April 2002.

M.S. Theses Supervised

[375] A. Raina. *Synthesis of Embedded Software using Dataflow Schedule Graphs.* Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, March 2017.

[376] H. Ben Salem. *Adaptive Tracking of People and Vehicles on Mobile Platforms.* Master's thesis, Department of Electrical and Computer Engineering, Technical University of Munich, Germany, May 2015.

[377] S. Won. *A Networked Dataflow Simulation Environment for Signal Processing and Data Mining Applications.* Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2012.

[378] S. Wu. *Representation and Scheduling of Scalable Dataflow Graph Topologies.* Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2011.

[379] S. Kedilaya. *Design and Testing Methodologies for Signal Processing Systems using DICE.* Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2010.

[380] C. Badr. *Synthesis of Embedded Software for Sensor Nodes*. Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2006.

[381] F. Haim. *Integrated Input Modeling and Memory Management for Image Processing Applications*. Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, December 2005.

[382] F. Keceli. *Dataflow Interchange Format and a Framework for Processing Dataflow Graphs*. Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2004.

[383] S. Lohani. *Performance Analysis of Polymorphous Computing Architectures*. Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, January 2003.

[384] A. Varma. *A Retargetable Optimizing Java-to-C for Embedded Systems*. Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2003.

[385] M. Khandelia. *Communication Scheduling in Embedded Multiprocessor Systems*. Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, 2001.

[386] B. Bhattacharya. *Parameterized Modeling and Scheduling for Dataflow Graphs*. Master's thesis, Department of Electrical and Computer Engineering, University of Maryland, College Park, November 1999.

6 Teaching Experience

6.1 Courses Taught at the University of Maryland

This is a list of courses that I have taught at the University of Maryland, ordered roughly in decreasing order of how frequently I have been teaching them.

- ENEE 408C: *Capstone Design Project — Modern Digital System Design*
- ENEE 150: *Intermediate Programming Concepts for Engineers*
- ENEE 114: *Programming Concepts for Engineers*
- ENEE 101: *Introduction to Electrical & Computer Engineering: Module on Engineering Software Development*
- ENEE 759E: *Synthesis of Embedded Software*
- ENEE 206: *Fundamental Electric and Digital Circuit Laboratory*
- ENEE 644: *Computer-aided Design of Digital Systems*
- ENEE 698B: *Computer Engineering Seminar*

6.2 Courses Developed at the University of Maryland

- ENEE 150: *Intermediate Programming Concepts for Engineers*
- ENEE 759E: *Synthesis of Embedded Software*
- ENPM 808R *Design and Synthesis of Digital Systems*

6.3 Summer School Organization

- Steering Committee Member, *Summer School on 3D and High Definition / High Contrast Video Processing Systems*, Hsinchu, Taiwan, July 4 through July 8, 2011.
- Co-Chair, *Summer School on Embedded Signal Processing Systems*, Leiden, The Netherlands, August 30 through September 3, 2010.

6.4 Summer School Lectures

- *Design and Implementation of Video Processing Systems*, Summer School on 3D and High Definition / High Contrast Video Processing Systems, Hsinchu, Taiwan, July 7, 2011.
- *Dynamic and Parameterized Dataflow Graphs*, Summer School on Embedded Signal Processing Systems, Leiden, The Netherlands, August 31, 2010.

6.5 Special Courses Taught at other Institutions

(Reverse chronological in terms of the most recent offering.)

- *Design Methodologies for Adaptive Stream Mining Systems*: University of Oulu, Finland (2015).
- *Signal Processing Design Flow: Simulation and Software*: Hughes Network Systems, USA (with Will Plishker, 2011).
- *FPGA-Based Design and Implementation of Signal Processing Systems*: Hughes Network Systems, USA (2010).
- *Design and Implementation of Signal Processing Software*: Tampere University of Technology, Finland (2005, 2007); University of Erlangen-Nuremberg, Germany (2005); University of Oulu, Finland (2006).
- *Software Synthesis from Dataflow Graphs*: Tampere University of Technology, Finland (2006).

7 Invited Talks

1. "Embedded System Design Optimization for Sensor Processing at the Edge", Army Research Laboratory, Adelphi, MD, April 17, 2019.
2. "Design and Synthesis of Software for Edge Intelligence Using Dataflow Schedule Graphs", Edge Intelligence Summit, Atlanta, Georgia, April 8, 2019.
3. "Design and Implementation of Multicore Signal Processing Systems", National Chiao-Tung University, Hsinchu, Taiwan, March 20, 2019.
4. "Design and Implementation of Multicore Signal Processing Systems", National Tsing Hua University, Hsinchu, Taiwan, March 13, 2019.
5. "The DSPCAD Framework for Dataflow-based Design and Implementation of Signal Processing Systems", Army Research Laboratory, Adelphi, MD, February 27, 2019.
6. "A Framework for Research on Edge Intelligence", Microsoft Research, Redmond, Washington, November 29, 2018.
7. "Software Synthesis from Dataflow Schedule Graphs", National Chung Hsing University, Taichung, Taiwan, October 5, 2018.
8. "Hardware/Software Design Optimization for Wireless Communication Systems", Laboratory for Telecommunications Sciences, College Park, Maryland, August 9, 2018.

9. "A Design Tool for High Performance Image Processing on Multicore Platforms", Special Session on Smart Vision Systems at the Design, Automation and Test in Europe Conference, Dresden, Germany, March 22, 2018.

10. "The DSPCAD Framework for Dataflow-based Design and Implementation of Signal Processing Systems", IRISA, Rennes, France, December 14, 2017.

11. "PRUNE: Dynamic and Decidable Dataflow for Signal Processing on Heterogeneous Platforms", Dataflow Workshop, Rennes, France, December 12, 2017.

12. "Design and Implementation of Multicore Signal Processing Systems", Workshop on Algorithm/Architecture Co-design for Artificial Intelligence, Tainan, Taiwan, November 2, 2017.

13. "Multiobjective Optimization Using Evolutionary Algorithms", National Institute of Standards and Technology, Gaithersburg, Maryland, October 4, 2017.

14. "The DSPCAD Framework for Dataflow-based Design and Implementation of Signal Processing Systems", **keynote talk**, Conference on Design and Architectures for Signal and Image Processing, Dresden, Germany, September 27, 2017.

15. "The DSPCAD Framework for Dataflow-based Design and Implementation of Signal Processing Systems", KTH, Kista, Sweden, March 17, 2017.

16. "The DSPCAD Framework for Dataflow-based Design and Implementation of Signal Processing Systems", National Chung Hsing University, Taichung, Taiwan, October 7, 2016.

17. "The DSPCAD Framework for Dataflow-based Design and Implementation of Signal Processing Systems", National Cheng Kung University, Tainan, Taiwan, October 6, 2016.

18. "Dynamic Data-Driven Methods for Multispectral Video Processing using Lightweight Dataflow Graphs", International Workshop on 3D Multimedia Systems, Tainan, Taiwan, October 3, 2016.

19. "Prototyping Real-Time Tracking Systems on Mobile Devices", Special Session on Funded International Projects, ACM International Conference on Computing Frontiers, Como, Italy, May 17, 2016.

20. "Methodologies and Tools for Design and Implementation of Secure Wireless Communications Systems", Maryland Cybersecurity Center Symposium, University of Maryland College Park, Maryland, December 7, 2015.

21. "Design and Implementation of Adaptive Stream Mining Systems using Lightweight Dataflow Graphs", Air Force Research Laboratory, Rome, New York, October 30, 2015.

22. "An Overview of Research in the Maryland DSPCAD Research Group", Aalto University, Espoo, Finland, August 19, 2015.

23. "Dataflow Techniques for Multicore Digital Signal Processors", University of Erlangen-Nuremburg, Erlangen, Germany, August 14, 2015.

24. "An Overview of the Maryland DSPCAD Research Group", Salzburg University of Applied Sciences, Puch/Salzburg, Austria, July 17, 2015.

25. "A Brief Overview of the Maryland DSPCAD Research Group", Naval Research Laboratory, Washington, DC, June 26, 2015.

26. "Design and Implementation of Adaptive Stream Mining Systems using Lightweight Dataflow Graphs", Åbo Akademi, Turku, Finland, May 22, 2015.

27. "A Brief Overview of the Maryland DSPCAD Research Group", National Institute of Standards and Technology, Gaithersburg, Maryland, May 4, 2015.

28. "Design and Implementation of Adaptive Stream Mining Systems using Lightweight Dataflow Graphs", Georgia Institute of Technology, Atlanta, Georgia, April 21, 2015.

29. "Dataflow Techniques for Multicore Digital Signal Processors", **keynote talk**, ParallaX (Parallel Acceleration) Workshop, Espoo, Finland, March 26, 2015.

30. "Dataflow Scheduling Techniques for Multicore Digital Signal Processors", **keynote talk**, IEEE Global Conference on Signal and Information Processing, Atlanta, Georgia, December 5, 2014.

31. "Dataflow-based Design and Implementation of Signal Processing Systems", National Institute of Standards and Technology, Gaithersburg, Maryland, November 13, 2014.

32. "Model-Based Design and Implementation of Adaptive Stream Mining Systems", Keysight Technologies, Santa Clara, California, November 5, 2014.

33. "Partial Expansion of Dataflow Graphs for Resource-Aware Scheduling of Multicore Signal Processing Systems", IEEE Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, California, November 3, 2014.

34. "Vectorization and Mapping of Software Defined Radio Applications on GPU Platforms", GPU Summit at the UMD/NVIDIA CUDA Center for Excellence, College Park MD, October 27, 2014.

35. "Design and Implementation of Adaptive Stream Mining Systems using Lightweight Dataflow Graphs", **keynote talk**, Workshop on Methods and Tools for Dataflow Programming, Madrid, Spain, October 7, 2014.

36. "Model-Based Design and Implementation of Adaptive Stream Mining Systems", Laboratory for Telecommunications Sciences, College Park, Maryland, August 28, 2014.

37. "Model-based Design and Implementation of Signal Processing Systems", Samsung Research America, Dallas, Texas, August 22, 2014.

38. "A System-level Design Approach for Dynamic Resource Coordination and Energy Optimization in Sensor Network Platforms", Institut National des Sciences Appliquées, Rennes, France, May 16, 2014.

39. "Methods for Design and Implementation of Dynamic, Data-Driven Signal Processing Systems", Army Research Laboratory, Adelphi, MD, February 11, 2014.

40. "Design and Implementation of Adaptive Stream Mining Software using Lightweight Dataflow Graphs", **keynote talk**, Embedded Software Workshop, Hsinchu, Taiwan, December 27, 2013.

41. "A System-level Design Approach for Dynamic Resource Coordination and Energy Optimization in Sensor Network Platforms", IEEE Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, California, November 5, 2013.

42. "Multicore DSP Software Synthesis using Partial Expansion of Dataflow Graphs", Workshop on Software Synthesis, Montreal, Canada, October 4, 2013.

43. "A Framework for Design and Implementation of Adaptive Stream Mining Systems", National Chiao-Tung University, Hsinchu, Taiwan, June 21, 2013.

44. "A Framework for Design and Implementation of Adaptive Stream Mining Systems", Academia Sinica, Taipei, Taiwan, June 18, 2013.

45. "A Framework for Design and Implementation of Adaptive Stream Mining Systems", National Tsing Hua University, Hsinchu, Taiwan, June 17, 2013.

46. "A Framework for Design and Implementation of Adaptive Stream Mining Systems", University of Victoria, British Columbia, Canada, May 24, 2013.

47. "Methods for Design and Implementation of Dynamic Signal Processing Systems", Laboratory for Telecommunications Sciences, College Park, Maryland, October 25, 2012.

48. "Modeling and Optimization of Dynamic Signal Processing in Resource-Aware Sensor Networks", Northrop Grumman Electronic Systems, Linthicum, Maryland, September 20, 2012.

49. "Methods for Design and Implementation of Dynamic Signal Processing Systems", Georgia Institute of Technology, Atlanta, Georgia, September 5, 2012.

50. "Adaptive Platforms for Multi-Dimensional Optimization of Sensor Network Deployments", The Johns Hopkins University Applied Physics Laboratory, Laurel, Maryland, August 29, 2012.

51. "Instrumentation Techniques for Cyber-Physical Systems Using the Targeted Dataflow Interchange Format", International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, Samos, Greece, July 17, 2012.

52. "Model-based Design and Implementation of Signal Processing Systems using the Dataflow Interchange Format", Qualcomm Flarion Technologies, Bridgewater, New Jersey, May 8, 2012.

53. "Lightweight Dataflow Programming for Signal Processing Systems", University of Oulu, Oulu, Finland, November 30, 2011.

54. "Software Synthesis from Dataflow Graphs: State of the Art and Emerging Trends", Workshop on Software Synthesis, Taipei, Taiwan, October 14, 2011.

55. "Lightweight Dataflow Programming for Signal Processing Systems", National Taiwan University, Taipei, Taiwan, October 13, 2011.

56. "Lightweight Dataflow Programming for Signal Processing Systems", National Tsing Hua University, Hsinchu, Taiwan, October 11, 2011.

57. "The Dataflow Interchange Format: Towards Co-Design of DSP-oriented Dataflow Models and Transformations", Klagenfurt University, Austria, August 29, 2011.

58. "Methods for Design and Implementation of Dynamic Signal Processing Systems", **keynote talk**, International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation, Samos, Greece, July 18, 2011.

59. "Methods for Design and Implementation of Dynamic Signal Processing Systems", National Taiwan University, Taipei, Taiwan, July 5, 2011.

60. "Design and Implementation of Dynamic Signal Processing Systems", National Instruments, Austin, Texas, April 1, 2011.

61. "The Dataflow Interchange Format: Towards Co-Design of DSP-oriented Dataflow Models and Transformations", National Radio Astronomy Observatory, Green Bank, West Virginia, March 25, 2011.

62. "The Dataflow Interchange Format: Towards Co-Design of DSP-oriented Dataflow Models and Transformations", Ptolemy Miniconference, Berkeley, California, February 16, 2011.

63. "Dataflow-based Design and Implementation of Signal Processing Systems: State of the Art and Emerging Trends", Royal Institute of Technology, Stockholm, Sweden, December 16, 2010.

64. "Model-based DSP Implementation on FPGAs", IEEE Signal Processing Washington DC Chapter Lecture Series, College Park, Maryland, USA, December 7, 2010.

65. "Model-based Design for Embedded Signal Processing Systems: A Brief Overview", University of Hawaii, Manoa, Hawaii, USA, December 3, 2010.

66. "Dataflow-based Design and Implementation of Signal Processing Systems: State of the Art and Emerging Trends", **keynote talk**, Conference on Design and Architectures for Signal and Image Processing, Edinburgh, Scotland, October 27, 2010.

67. "The Dataflow Interchange Format: Towards Co-Design of DSP-oriented Dataflow Models and Transformations", University of Minnesota, Minneapolis, April 1, 2010.

68. "The Dataflow Interchange Format: Towards Co-Design of DSP-oriented Dataflow Models and Transformations", University of Erlangen-Nuremburg, Erlangen, Germany, October 5, 2009.

69. "Dataflow-based Design and Implementation of Signal Processing Systems", Salzburg University of Applied Sciences, Salzburg, Austria, June 18, 2009.

70. "The Dataflow Interchange Format: An Environment for Integrating and Transforming DSP-Oriented Dataflow Models of Computation", Halmstad University, Halmstad, Sweden, June 10, 2009.

71. "Dataflow-based Design and Implementation of Signal Processing Systems", Ericsson Research, Lund, Sweden, June 11, 2009.

72. "Design and Implementation of Signal Processing Software for Lightweight Vehicles", Light Armored Vehicles & Stryker Summit, Tyson's Corner, VA November 17, 2008.

73. "Experimenting with Dataflow Scheduling Techniques using DIF", CAL Actor Language Workshop, Washington DC Metropolitan Area, USA, October 10, 2008.

74. "High Level Dataflow Techniques for Design and Implementation of Signal Processing Systems", National Radio Astronomy Observatory, Green Bank, West Virginia, August 28, 2008.

75. "The Dataflow Interchange Format: A Language and Environment for Experimenting with DSP-Oriented Dataflow Methods", IBM T. J. Watson Research Center, Hawthorne, New York, July 22, 2008.

76. "The Dataflow Interchange Format: An Environment for Integrating and Transforming DSP-Oriented Dataflow Models of Computation", Artist Workshop on Models of Computation and Communication, Eindhoven, The Netherlands, July 3 2008.

77. "High Level Design Transformations for DSP Systems", Nokia Innovation Center, Tampere, Finland, June 5, 2008.

78. "The Dataflow Interchange Format (DIF): A Framework for Specifying, Analyzing, and Integrating Dataflow Representations of DSP Systems", Workshop on Compiler Assisted SoC Assembly, Salzburg, Austria, September 30, 2007.

79. "Dataflow transformations in high-level DSP system design", Indian Institute of Technology, Kharagpur, India, July 26, 2007.

80. "Dataflow transformations in high-level DSP system design", Indian Institute of Technology, Chennai (Madras), Chennai, India, July 19, 2007.

81. "Dataflow transformations in high-level DSP system design", International Symposium on System-on-Chip, Tampere, Finland, November 16, 2006.

82. "Dataflow-based design and implementation of signal processing systems", Nokia Research Center, Tampere, Finland, August 23, 2006.

83. "Energy-driven partitioning of signal processing algorithms in sensor network", International Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation, Samos, Greece, July 17 2006.

84. "Software Synthesis from the Dataflow Interchange Format", Xilinx, Inc., San Jose, California, February 13, 2006.

85. "Design and Synthesis of Image Processing Systems using Reconfigurable Dataflow Graphs", Workshop on Distributed Embedded Systems, Leiden, The Netherlands, November 22, 2005.

86. "Design and Implementation of Multiprocessor DSP Systems", Pennsylvania State University, University Park, Pennsylvania, November 9, 2005.

87. "Dataflow-based Design of Multiprocessor DSP Systems", Texas Instruments, Inc., Dallas, Texas, September 30, 2005.

88. "Parallel Implementation of Embedded Signal Processing Systems", National Instruments, Austin, Texas, June 7, 2005.

89. "Multiprocessor System Synthesis for Embedded Signal Processing", University of Wisconsin at Madison, February 28, 2005.

90. "Software Synthesis Trade-offs in Dataflow Representations of DSP Applications", Streaming Systems Workshop, Dedham, Massachusetts, August 23, 2003.

91. "DIF: An Intermediate Representation Suite for DSP Design Tools", Cadence Design Systems, San Jose, California, December 19, 2002.

92. "Software Synthesis for Digital Signal Processing", Georgia Institute of Technology, Atlanta, Georgia, November 19, 2002.

93. "Software Synthesis for Digital Signal Processing", **keynote lecture**, Advanced School for Computing and Imaging Conference, Lochem, The Netherlands, June 19, 2002.

94. "Software Synthesis for Digital Signal Processing", Princeton University, Princeton, New Jersey, April 8, 2002.

95. "Mapping DSP Applications onto Self-timed Multiprocessors", IEEE Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, California, November 5, 2001.

96. "Modeling and Synthesis using Reconfigurable Dataflow Specifications", International Workshop on Systems, Architectures, Modeling, and Simulation, Samos, Greece, July 17 2001.

97. "Design and Synthesis of DSP Software using Dataflow-based Block Diagrams", LSI Logic Corp., Rockville, Maryland, June 5, 2001.

98. "Software Synthesis for Signal Processing Systems", Vienna Institute of Technology, Vienna, Austria, March 16, 2001.

99. "Module characterization for memory management in embedded software", Katholieke Universiteit, Leuven, Belgium. June 2, 2000.

100. "Hardware/software co-design", Annual Electrical Engineering, Computing and Systems Research Review Day, University of Maryland, College Park, MD. May 12, 2000.

101. "Software Synthesis for Signal Processing Systems", Department of Electrical and Computer Engineering, University of Delaware, Newark, Delaware, April 21, 2000.

102. "Hierarchical Design of Dynamic Software Systems", United Technologies Research Center, Hartford CT, April 7, 2000.

103. "High-level Modeling and Synthesis of DSP Software", Lockheed Advanced Technology Laboratory, Camden, NJ, November 1, 1999.

104. "Performance Analysis and Optimization of Multiprocessor Digital Signal Processing Systems" Lockheed Martin Corp, Bethesda, MD, September 22, 1999.

105. "An Overview of Research in the Maryland DSP-CAD Group", UMIACS Research Review Day, University of Maryland, College Park, February 19, 1999.

106. "Asynchrony in Computer Engineering Education", Annual Workshop on Computer Architecture Education, Orlando, Florida, January 9, 1999.

107. "Performance Analysis and Optimization of Multiprocessor Digital Signal Processing Systems" Atlantic Aerospace Electronics Corp., October 7, 1998.

108. "Compiling Dataflow Programs for Digital Signal Processing", Dortmund University, Dortmund, Germany, October 1, 1998.

109. "Performance Analysis and Optimization of Multiprocessor Schedules for Dataflow Programs", Naval Research Laboratory, Washington, DC, January 23, 1998.

110. "Computer-Aided Synthesis of Digital Signal Processing Systems", Bay Networks, Gaithersburg, MD, November 21, 1997.

111. "Low Power DSP Architectures and CAD Issues", Hitachi America, Ltd., Semiconductor Research Laboratory, San Jose, California, October 24, 1997.

112. "Modeling and Mapping of Signal and Image Processing Applications for Implementation on Special-Purpose Computing Platforms", Army Research Laboratory, Adelphi, MD, September 23, 1997.

113. "Optimized Software Synthesis from Dataflow Graphs", Department of Electrical Engineering, University of Maryland, College Park, April 1997.

114. "Optimized Software Synthesis from Dataflow Graphs", Department of Electrical and Computer Engineering, University of Wisconsin, Madison, April 1997.

115. "Optimized Software Synthesis from Dataflow Graphs", School of Electrical Engineering, Purdue University, March 1997.

116. "Optimized Software Synthesis from Dataflow Graphs", Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, March 1997.

117. "Optimized Software Synthesis from Dataflow Graphs", Department of Electrical and Computer Engineering, Iowa State University, March 1997.

118. "Optimized Software Synthesis from Dataflow Graphs", Department of Electrical Engineering, University of California, Riverside, April 1997.

119. "Optimization Issues in the Synthesis of Software from Dataflow Graphs", Department of Electrical Engineering, Swiss Federal Institute of Technology, Zurich, Switzerland, August, 1996.

120. "Optimization Issues in the Synthesis of Software from Dataflow Graphs", Katholieke Universiteit Leuven, Belgium, August, 1996.

121. "Optimization Issues in the Synthesis of Software from Dataflow Graphs", Darmstadt University of Technology, Darmstadt, Germany, August, 1996.

122. "A scheduling framework for minimizing memory requirements of multirate DSP systems represented as dataflow graphs", Aachen University of Technology, Aachen, Germany, October, 1993.

8 Professional Service

8.1 Service for Journals

- Co-Editor-in-Chief for the *Journal of Signal Processing Systems* (2013–present).
- Steering committee member for the *EURASIP Journal on Embedded Systems* (2005–2011).

- Editorial board member for the *EURASIP Journal on Embedded Systems* (2005–2011), *IEEE Transactions on Signal Processing* (2004–2007), *International Journal of Embedded Systems* (2004–2010), and *Journal of Signal Processing Systems* (2007–2013).

- Guest editor of special issues for the *ACM Transactions on Embedded Computing Systems*; *EURASIP Journal on Applied Signal Processing*; *EURASIP Journal on Embedded Systems*; *Journal of Signal Processing Systems* (and its earlier version, the *Journal of VLSI Signal Processing Systems for Signal, Image, and Video Technology*); *IEEE Computer Magazine*; *IEEE Signal Processing Magazine*; *IEEE Transactions on Biomedical Circuits and Systems*; and *International Journal of Embedded Systems.*

- Reviewer for many journals and magazines.

8.2 Society and Technical Committee Service

- Fellow Evaluation Committee, *IEEE Computer Society*, 2011.

- Director of Membership Services, *IEEE Signal Processing Society*, January 2010 through December 2012.

- Member of the *IEEE Circuits and Systems Society Technical Committee on VLSI Systems and Applications*, July 2009 to 2012.

- Past Chair of the *IEEE Signal Processing Society Technical Committee on Design and Implementation of Signal Processing Systems*, January 2010 through December 2011.

- Chair of the *IEEE Signal Processing Society Technical Committee on Design and Implementation of Signal Processing Systems*, January 2008 through December 2009.

- Member of the *IEEE Signal Processing Society Technical Committee on Design and Implementation of Signal Processing Systems*, 2002 through 2011.

8.3 Service for Conferences and Workshops

8.3.1 Chairing Roles

- General Chair for the *International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation* (2012); and *International Workshop on Systems, Architectures, Modeling and Simulation* (2004).

- General Co-chair for the *IEEE GlobalSIP Symposium on Signal Processing on Graphics Processing Units and Multicores* (2015); *IEEE International Conference on Application Specific Systems, Architectures, and Processors* (2003); *IEEE Workshop on Embedded Computer Vision* (2007); *IEEE Workshop on Signal Processing Systems* (2010); *International Conference on Compilers, Architectures, and Synthesis for Embedded Systems* (2002); and *International Conference on Embedded Software and Systems* (2008).

- Technical Program Chair for the *IEEE Workshop on Embedded Computer Vision* (2006).

- Technical Program Co-chair for the *ACM/IEEE International Conference on Distributed Smart Cameras* (2009); *IEEE International Conference on Application Specific Systems, Architectures, and Processors* (2002); *IEEE Workshop on Signal Processing Systems* (2008); *IEEE Biomedical Circuits and Systems Conference* (2008); and *International Workshop on Embedded Software Optimization* (2006).

- Co-chair for the *Workshop on Accelerating Time-to-market through Compiler Driven Optimization of Embedded Platforms*, held in conjunction with the *International Conference on Compilers, Architectures, and Synthesis for Embedded Systems* (2004).

- Topic Co-chair for "Compilers and Code Generation for Embedded Systems" in the *Design Automation and Test in Europe Conference and Exhibition* (2008, 2009, 2010).

- Finance Chair for the *ACM/IEEE International Conference on Distributed Smart Cameras* (2010); and *IEEE Workshop on Signal Processing Systems* (2008).

8.3.2 Organization of Special Sessions

- Special session entitled "Insights from Negative Results" organized by Karol Desnos and Shuvra S. Bhattacharyya, *IEEE International Conference on Embedded Computer Systems*, Samos, Greece, July 2019.
- Special session on "Analytics Algorithm/Architecture for Smart System Design," organized by Shuvra S. Bhattacharyya and Gwo-Giun Lee, *IEEE International Conference on Artificial Intelligence Circuits and Systems*, Hsinchu, Taiwan, March 2019.
- Special session entitled "Negative Results Matter Too!" organized by Karol Desnos and Shuvra S. Bhattacharyya, *IEEE International Conference on Embedded Computer Systems*, Samos, Greece, July 2018.
- Special session on "DSP System Design for Wireless Communications," organized by Shuvra S. Bhattacharyya and Marilyn Wolf, *IEEE International Workshop on Signal Processing Systems*, Lorient, France, October 2017.
- Special session on "System-Level Modeling and Design Methodologies for Signal Processing Systems," organized by Shuvra S. Bhattacharyya and Karol Desnos, *IEEE International Workshop on Signal Processing Systems*, Dallas, Texas, October 2016.
- Special session on "Model-based Design Optimization for Signal Processing Systems," organized by S. Saha and S. S. Bhattacharyya, *IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, November 2011.
- Special session on "Model-based Design Optimization for Signal Processing Systems," organized by S. Saha and S. S. Bhattacharyya, *IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, November 2011.
- Special session on "Design Challenges in Energy Efficient Software Defined Radio," organized by B. Bougard, S. S. Bhattacharyya, and J. Takala, *International Conference on Acoustics, Speech, and Signal Processing*, Las Vegas, Nevada, March 2008.

8.3.3 Program Committee Service

Served on numerous technical program committees for international conferences and workshops, including ASAP, CASES, DATE, ECVW, EMSOFT, ESTIMEDIA, EUSIPCO, HCW, ICASSP, ICCAD, ICME, ICPR, IC-SAMOS, ISCAS, MEMOCODE, SCOPES, SDR, SiPS, and SoC.

8.3.4 Tutorials

- "Design for Low-Power Internet-of-Things (IoT) Systems" (with F. Palumbo, J. Takala, and M. Wolf), *International Symposium on Circuits and Systems*, Florence, Italy, May 27, 2018.
- "FPGA Tools and Techniques for High Performance Digital Systems" (with M. Schulte and A. Gregerson), *Topical Workshop on Electronics for Particle Physics*, Paris, France, September 25, 2009.
- "Accelerated Image Processing with FPGAs and GPUs" (with R. Shekhar, W. Plishker, J. Fung, J. Stam, R. Koch, C. Zach), *International Conference on Image Processing*, San Diego, USA, October 12, 2008.
- "Software Radio Tutorial" (with K. Choi), *International Workshop on Embedded Software*, Jersey City, USA, September 18, 2005.

8.3.5 Other Service for Conferences and Workshops

- Member of the *IEEE Signal Processing Society Conference Board*, 2009.
- Steering Committee member for the *International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation* and its earlier versions, including the *International Workshop on Systems, Architectures, Modeling and Simulation* (2004 to present).
- Coordination Vice-chair for the *International Conference on Compilers, Architectures, and Synthesis for Embedded Systems* (2001).
- Reviewer for many conferences and workshops.

8.4 Ph.D. Thesis Committees

- Ph.D. Thesis Defense Service for the following institutions: Eindhoven University of Technology, The Netherlands; Georgia Institute of Technology, USA; Halmstad University, Sweden; Institute National des Sciences Appliquees, Rennes, France; Leiden University, The Netherlands; Queen's University Belfast, United Kingdom; Royal Institute of Technology, Stockholm, Sweden; Tampere University of Technology, Finland; University of Erlangen-Nuremburg, Germany; University of Maryland, College Park, USA; University of Oulu, Finland; University of Twente, The Netherlands.
- Ph.D. Thesis Reviewer for the following institutions: Tampere University of Technology, Finland; University of Auckland, New Zealand; University of Oulu, Finland.

8.5 Reviewing Activities for Agencies

- Grant proposal evaluation panel member for the Deutsche Forschungsgemeinschaft (German Research Council); Portuguese Foundation for Science and Technology; U. S. Department of Energy; and U. S. National Science Foundation.
- Grant proposal reviewer for the Academy of Finland; American University of Beirut; Austrian Science Fund, Austria; Binational Fulbright Commission in Egypt; Christian Doppler Research Association, Austria; Dutch Technology Foundation; French National Research Agency; Kazakhstani National Center of Science and Technology Evaluation; Netherlands Organization for Scientific Research; Romanian–U.S. Fulbright Commission; Royal Society of New Zealand; Swedish Research Council for Engineering Sciences; Swiss National Science Foundation; University of Missouri Research Board; U.S. Air Force Office of Scientific Research; U.S. Air Force Research Laboratory; U.S. National Institutes of Health.

8.6 Service for Book Publication

- Reviewer of book proposals and book chapters for for Addison-Wesley, Brooks/Cole Publishing, Kluwer Academic Publishers, McGraw-Hill, Morgan Kaufmann, Prentice Hall, Springer, and Wiley.