

Make the Most of On-Chip Memory for Embedded DSP Systems

NEW!

# Memory Management for Synthesis of DSP Software

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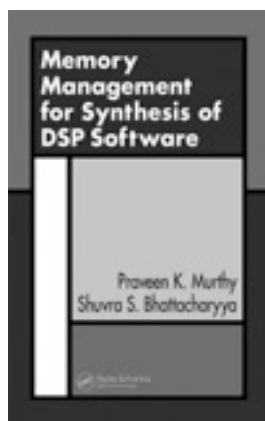
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## Effective Strategies for Aggressive Memory Optimization

Although programming in memory-restricted environments is never easy, this holds especially true for digital signal processing (DSP). The data-rich, computation-intensive nature of DSP makes memory management a chief and challenging concern for designers. **Memory Management for Synthesis of DSP Software** focuses on minimizing memory requirements during the synthesis of DSP software from dataflow representations. Dataflow representations are used in many popular DSP design tools, and the methods of this book can be applied in that context, as well as other contexts where dataflow is used.



This book systematically reviews research conducted by the authors on memory minimization techniques for compiling synchronous dataflow (SDF) specifications. Beginning with an overview of the foundations of software synthesis techniques from SDF descriptions, it examines aggressive buffer-sharing techniques that take advantage of specific and quantifiable tradeoffs between code size and buffer size to achieve high levels of buffer memory optimization.

The authors outline coarse-level strategies using lifetime analysis and dynamic storage allocation (DSA) for efficient buffer sharing as one approach and demonstrate the role of the CBP (*consumed-before-produced*) parameter at a finer level using a merging framework for buffer sharing. They present two powerful algorithms for combining these sharing techniques and then introduce techniques that are not restricted to the single appearance scheduling space of the other techniques.

Extensively illustrated to clarify the mathematical concepts, **Memory Management for Synthesis of DSP Software** presents a comprehensive survey of state-of-the-art research in DSP software synthesis.

## FEATURES

- ▶ Focuses on techniques for minimizing memory requirements during the synthesis of software from dataflow representations of DSP systems
- ▶ Describes buffer-sharing models and techniques
- ▶ Addresses the DSA problem and its various solutions
- ▶ Contains an extensive list of references for more in-depth information
- ▶ Collects a large amount of SDF compiler work in a single source and explains it coherently and systematically
- ▶ Reviews related and background work in the area comprehensively

## CONTENTS

### INTRODUCTION

Electronic Embedded Systems  
Digital Signal Processing Systems  
Actor-Oriented Design  
Dataflow MoCs for DSP Systems  
Synthesis Techniques in AOPes  
Advances in Compilers for DSPs  
Other Related Work—Nested Loop Scheduling

### NOTATION AND BACKGROUND

Graph Terminology  
Synchronous Dataflow  
Synthesis from SDF Graphs  
Scheduling Problems for SDF Graphs  
Constructing Memory-Efficient Loop Structures  
Scheduling for Other Metrics  
Other Topics: Holes  
Summary

See reverse side for continuation of Contents and ordering information

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**LIFETIME ANALYSIS**

Introduction  
 The Shared Buffer Model  
 Creating the Interval Instances from a SAS  
 Conclusion

**DYNAMIC STORAGE ALLOCATION**

Some Notation  
 Heuristic for DSA  
 Computing the Maximum Clique Weight  
 Experimental Results  
 Approximation Algorithms

**THE CBP PARAMETER**

Related Work  
 Introduction to Buffer Merging  
 The CBP Parameter

Multirate FIR Filters  
 Chop  
 Autocorrelation  
 CBP Tables  
 Summary of Derivations  
 Conclusion

**BUFFER SHARING VIA MERGING TECHNIQUES**

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Recursive Decomposition of a Two-Actor SDF Graph  
 Extension to Arbitrary SAS  
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 Conclusion

**CONCLUSION**

Regularity  
 Fixed-Point Optimizations  
 Reconfigurable Systems  
 Grand Challenge

**REFERENCES INDEX**



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