http://www.ece.umd.edu/~pabshire/enee312h.htm due Thursday, April 25, 2002

1) Derive the transconductance g_m and the normalized transconductance g_m / I_D for an nMOS transistor biased in weak inversion (subthreshold operation) and in strong inversion. Keeping in mind that the current I_D changes smoothly from one regime of operation to the other, answer the following questions:
   a. If you want to use this transistor in a circuit and obtain the maximum gain, how would you bias the transistor?
   b. If you want to use this transistor and obtain the maximum gain per unit current, how would you bias the transistor?

2) – 8) Complete Sedra & Smith problems 5.1, 5.3, 5.7, 5.19, 5.27, 5.38, 5.43

Research Question:
An MOS transistor does not require a gate current, only a voltage. This characteristic makes possible a class of devices which employ a *floating gate* for the MOS transistor – that is, there is no direct connection to the gate terminal of the device, only capacitive coupling to control this voltage (which in turn is capacitively coupled to the channel) and charge storage at the intermediate node. This scheme is widely used in digital integrated circuits to create arrays of devices that can be turned on or off, for example to make EEPROMs or PLAs. Analog circuits make use of floating gates as well – the floating node can provide long term charge storage, for example.

Find a patent which has employed a floating gate in an analog circuit. Provide the patent number, name, abstract, and inventors.