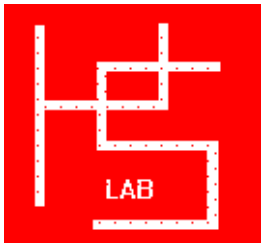

Semistate Theory and Design of Analog VLSI Circuits

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Describing Equations - I

General Nonlinear Time-Varying Circuit

$$0 = F(x, \dot{x}, u, t)$$
$$0 = G(x, y, u, t)$$

x=internal description vector, k-vector

$\dot{x}$=time derivative

u=input, m-vector

y=output, n-vector

Difficulty: too cumbersome to use for most purposes of analysis or synthesis.

Describing Equations - II

State Variable Equations

$$\dot{x} = F(x,u,t)$$
$$y = G(x,t)$$

x = internal state, k-vector

$\dot{x}$ = time derivative

u = input, m-vector

y = output, n-vector

Advantage: covered by years of mathematical theories

Difficulty: must augment G separately to include resistors, differentiators, etc..

$$G(x,t) \Rightarrow G(x,u,\dot{u},\ddot{u},\ldots,t)$$

Describing Equations - III

Semistate Equations State Equations

Canonical Form

$$E\dot{x} = A(x,t) + Bu$$
$$y = Cx$$

B, C, E constant matrices
x=internal state, k-vector
$\dot{x}$=time derivative
u=input, m-vector
y=output, n-vector

This is the form needed for VLSI where $A(x,t)=A(x)$ is usually nonlinear.

Describing Equations - IV

Linear Time-Invariant (LTI) Circuits

$$E\dot{x} = Ax + Bu$$
$$y = Cx\ (+Du)$$

A, B, C, D, E = constant matrices
x=semi-state, k-vector
$\dot{x}$=time derivative
u=input, m-vector
y=output, n-vector

If $E=1_k$ reduces to state variable case. Most useful time-domain description for design of linear circuits.

We will assume all quantities real.

Setting Up Equations - I

Use graph theory:

b = branches & # of branches
ℓ = links & # of independent link branches
t = tree & # of independent tree branches
Assume only one separate part by attaching common grounds
number tree branches first and links last

$$v_b = \begin{bmatrix} v_t \\ v_\ell \end{bmatrix}, \quad i_b = \begin{bmatrix} i_t \\ i_\ell \end{bmatrix}$$

$0 = Ci_b$, KCL, 1 equation for each t branch

$C = \begin{bmatrix} 1_t & M \end{bmatrix}$ = cut-set matrix

$0 = Tv_b$, KVL, 1 equation for each ℓ branch

$T = \begin{bmatrix} N & 1_\ell \end{bmatrix}$ = tie-set matcix

Setting Up Equations - II

$$\text{Power\_in} = 0 = v_b^T i_b = v_t^T \begin{bmatrix} 1_t \\ M^T \end{bmatrix} \begin{bmatrix} N & 1_\ell \end{bmatrix} i_\ell$$

As a graph exists where v_t and i_ℓ are independent sources, $N = -M^T$;

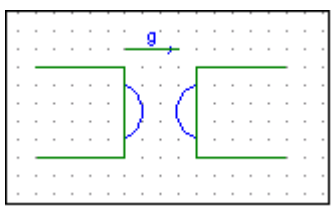
$$v_b = C^T v_t = \begin{bmatrix} 1_t \\ M^T \end{bmatrix} v_t \,,\; v_\ell = M^T v_t$$

$$i_b = T^T i_\ell = \begin{bmatrix} -M \\ 1_\ell \end{bmatrix} i_\ell \,,\; i_t = -M i_\ell$$

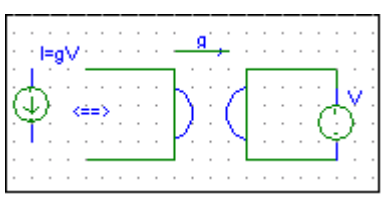
$$x = \begin{bmatrix} v_t \\ i_\ell \end{bmatrix}$$

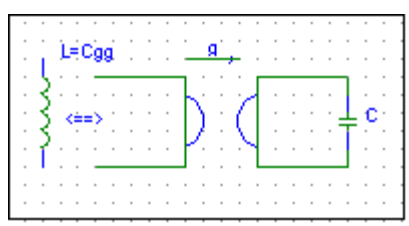
Setting Up Equations - III

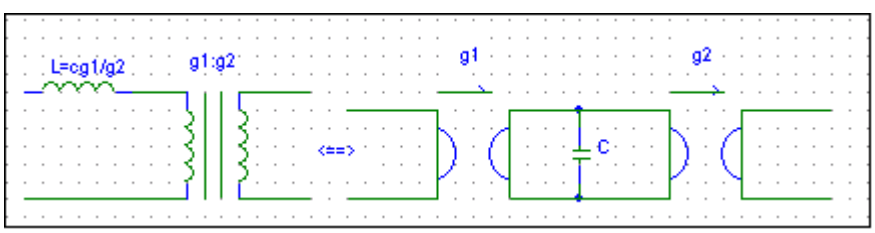
Assume, for convenience of seeing the theory, and by available equivalences usually using gyrators, that all dynamics is in capacitors and all sources are current sources. For a linear time-invariant circuit we can also assume a branch by branch admittance matrix exists.



$$Y = \begin{bmatrix} 0 & g \\ -g & 0 \end{bmatrix}$$

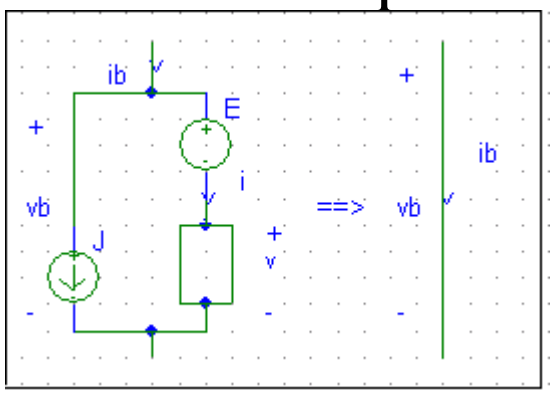






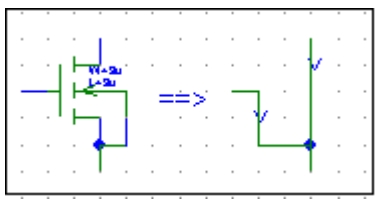
Setting Up Equations - IV

Generic Graph Element

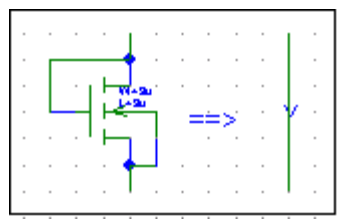


$$i_b = i + J$$

$$v_b = v + E$$



$$\beta = \frac{K_P}{2}\frac{W}{L}$$

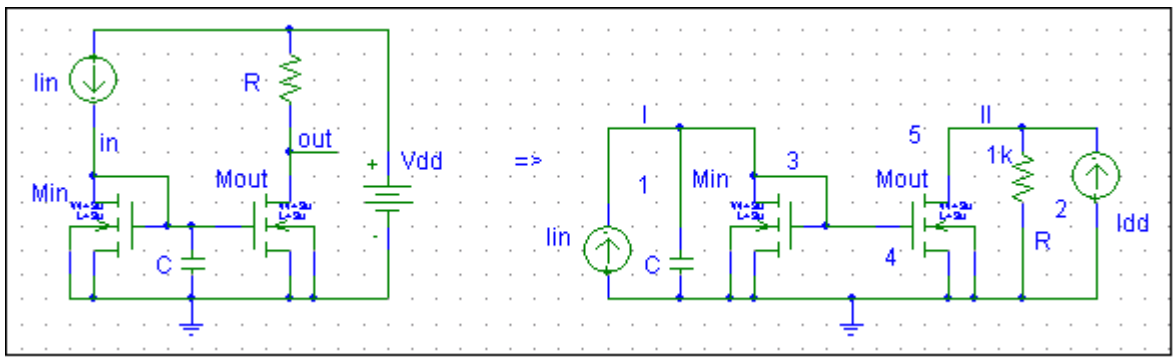


$$i_d = f(v_{gs}, v_{ds}; \beta)$$

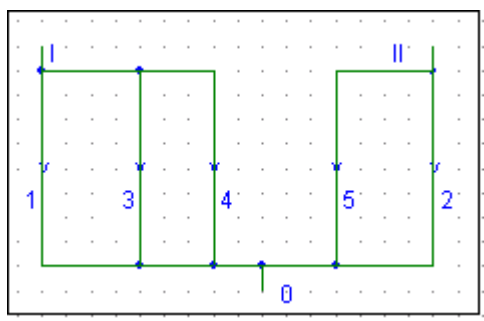
$$= \begin{cases} 0 & \text{if } v_{gs} - V_{th} \le 0 \le v_{ds} \\ \beta(2(v_{gs} - V_{th})v_{ds} - v_{ds}^2)(1 + \lambda v_{ds}) & \text{if } 0 \le v_{gs} - V_{th} \le v_{ds} \\ \beta(v_{gs} - V_{th})^2(1 + \lambda v_{ds}) & \text{if } v_{gs} - V_{th} \ge v_{ds} \ge 0 \end{cases}$$

Setting Up Equations Example 1 - I

Current Mirror



Graph



$$x = \begin{bmatrix} v_t \\ i_\ell \end{bmatrix} = \begin{bmatrix} v_{b1} \\ v_{b2} \\ i_{b3} \\ i_{b4} \\ i_{b5} \end{bmatrix} = \begin{bmatrix} v_1 \\ v_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix}$$

$$u = I_{in};\ y = i_{b5} = Cx = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} x$$

Setting Up Equations Example 1 - II

KCL – cut sets for nodes I & II

$$\begin{bmatrix}0\\0\end{bmatrix}=\begin{bmatrix}1 & 0 & 1 & 1 & 0\\0 & 1 & 0 & 0 & 1\end{bmatrix}\begin{bmatrix}i_{b1}\\i_{b2}\\i_{b3}\\i_{b4}\\i_{b5}\end{bmatrix}=Ci_b$$

KVL – tie sets for links 3,4,5

$$\begin{bmatrix}0\\0\\0\end{bmatrix}=\begin{bmatrix}-1 & 0 & 1 & 0 & 0\\-1 & 0 & 0 & 1 & 0\\0 & -1 & 0 & 0 & 1\end{bmatrix}\begin{bmatrix}v_{b1}\\v_{b2}\\v_{b3}\\v_{b4}\\v_{b5}\end{bmatrix}=Tv_b$$

$$\begin{bmatrix}v_{b3}\\v_{b4}\\v_{b5}\end{bmatrix}=\begin{bmatrix}1 & 0\\1 & 0\\0 & 1\end{bmatrix}v_t=M^{T}v_t,\quad \begin{bmatrix}i_{b1}\\i_{b2}\end{bmatrix}=\begin{bmatrix}-1 & -1 & 0\\0 & 0 & -1\end{bmatrix}i_\ell=-Mi_\ell$$

$$=v_\ell \qquad\qquad =i_t$$

Setting Up Equations Example 1 - III

$$v_b = v, \quad i_b = i + J; \; J = \begin{bmatrix} -I_{in} & -GV_{dd} & 0 & 0 & 0 \end{bmatrix}^T$$

Device Equations

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} C\dot{v}_1 \\ Gv_2 \\ f(v_1, v_1; \beta_1) \\ 0 \\ f(v_1, v_2; \beta_2) \end{bmatrix} = i_b - J = \begin{bmatrix} i_{b1} \\ i_{b2} \\ i_{b3} \\ i_{b4} \\ i_{b5} \end{bmatrix} + \begin{bmatrix} I_{in} \\ GV_{dd} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$= \begin{bmatrix} -M \\ 1_3 \end{bmatrix} i_\ell + \begin{bmatrix} 0 \\ GVdd \\ 0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u$$

Setting Up Equations Example 1 - IV

Final Semistate Equations

$$\begin{bmatrix} C & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \dot{x} = \begin{bmatrix} 0 & 0 & -1 & -1 & 0 \\ 0 & -G & 0 & 0 & -1 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} x + \begin{bmatrix} 0 \\ GVdd \\ -f(v1,v1,\beta 1) \\ 0 \\ -f(v1,v2,\beta 2) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u$$

$$y = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \end{bmatrix} x$$

Reducing

$$C\dot{v}_1 = -f(v_1, v_1; \beta_1) + u$$

$$x_5 = f(v_1, v_2; \beta_2) = -Gv_2 + GV_{dd}$$

$$y = f(v_1, v_2; \beta_2)$$

Common case:

$$f(v1,v1;\beta 1) = \frac{\beta_1}{\beta_2} f(v1,v2;\beta 2)$$

$$C\dot{v}_1 = -\frac{\beta_1}{\beta_2} y + u$$

$$C = 0 \Rightarrow y = \frac{\beta_2}{\beta_1} u = \frac{W_2}{W_1} \frac{L_1}{L_2} u$$

Semistate for LTI Circuits - I

$$E\dot{x} = Ax + Bu$$
$$y = Cx$$

We will assume a "regular" system i.e. inverse exists for sE-A

Examples:

Admittance matrix, u=v, y=i:

$Y(s) = C(sE-A)^{-1}B$

Resistive circuit on admittance basis:

$Y = CA^{-1}B$

Derivative:

$$\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}\dot{x} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}x + \begin{bmatrix} 0 \\ 1 \end{bmatrix}u$$
$$y = \begin{bmatrix} -1 & 0 \end{bmatrix}x$$

$$C(sE-A)^{-1}B = \begin{bmatrix} -1 & 0 \end{bmatrix}\begin{bmatrix} 1 & -s \\ 0 & 1 \end{bmatrix}\begin{bmatrix} 0 \\ 1 \end{bmatrix} \text{ as } \det(sE-A) = \det\begin{bmatrix} 1 & s \\ 0 & 1 \end{bmatrix} = 1$$

or $y = su$

Semistate for LTI Circuits - II

Addition of admittances:

$$Y_1(s)=C_1(sE_1-A_1)^{-1}B_1;\quad Y_2(s)=C_2(sE_1-A_2)^{-1}B_2$$

$$u=u_1=u_2,\ y=y_1+y_2,\ x=\begin{bmatrix}x_1\\x_2\end{bmatrix}$$

$$\begin{bmatrix}E_1 & 0\\0 & E_2\end{bmatrix}sx=\begin{bmatrix}A_1 & 0\\0 & A_2\end{bmatrix}x+\begin{bmatrix}B_1\\B_2\end{bmatrix}u$$

$$y=\begin{bmatrix}C_1 & C_2\end{bmatrix}x$$

Semistate Properties - I

Index of a matrix: smallest nonnegative i for which

$$\text{rank}(A^i) = \text{rank}(A^{i+1})$$

Examples: Nonsingular = index 0

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}^1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}^2 \Rightarrow \text{index } 1$$

$$\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \Rightarrow index = 2$$

$$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \Rightarrow \text{index} = 3$$

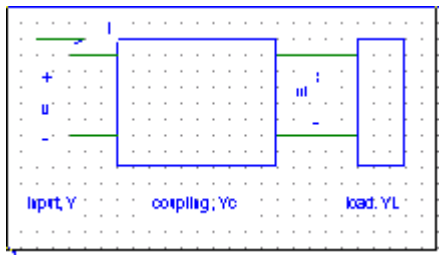
Semistate Properties - II

$$\begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \Rightarrow \text{index}1, \quad \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \Rightarrow \text{index}4$$

$$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \bullet\!\!+ \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \Rightarrow \text{index 3; block indices (3,2)}$$

Physical meaning:
Sum of (block index-1)
= # of differentiators needed

Semistate Design - I



$$Y(s)=Y_{11}+Y_{12}(Y_L(s)+Y_{22})^{-1}Y_{21}$$

Compare with

$$Y(s)=C(sE-A)^{-1}B$$

Therefore identify

$$sEx=Y_L(s)x=-Y_{22}x+Y_{21}u$$
$$y=Y_{12}x$$

In order to realize Y_L with capacitors, for VLSI, transform E to symmetric positive semidefinite

Semistate Design - II

Transformation: multiply by P and replace x by Qx to replace

E by

$$PEQ = C_{ap} \overset{\bullet}{+} 0_{k-c}$$

$$\text{where } \overset{\bullet}{+} = \text{direct sum},$$

$$C_{ap} = C_{ap}^{T} \text{ and } c = \text{rank} E$$

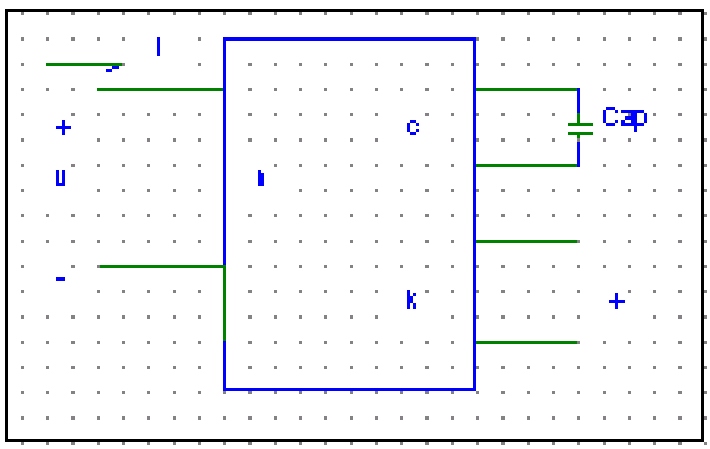
Semistate Design - III

$$PEQsx = [C_{ap} \dot{+} 0_{k-c}]sx = PAQx + PBv$$

$$i = CQx$$

$$Y_{Load} = sC_{ap} \dot{+} 0_{k-c}$$

$$Y_{coupling} = \begin{bmatrix} 0 & CQ \\ PQ & -PAQ \end{bmatrix} = \begin{bmatrix} 1_n & 0 \\ 0 & P \end{bmatrix} \begin{bmatrix} 0 & C \\ B & -A \end{bmatrix} \begin{bmatrix} 1_n & 0 \\ 0 & Q \end{bmatrix}$$



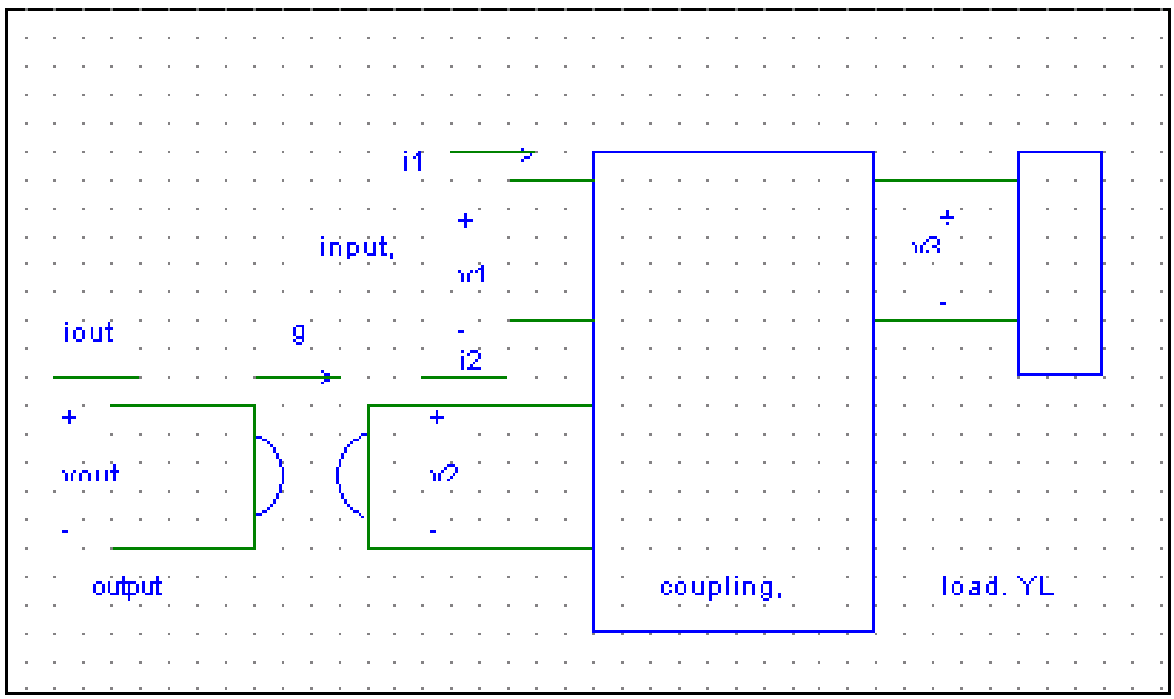
Bring C_{ap} to diagonal positive definite form (always possible) to synthesize by uncoupled positive capacitors.
Synthesize $Y_{coupling}$ by differential pairs.
Note that $Y_{coupling}$ may be active.

Semistate Design - IV

Transfer function synthesis:

Transform to Y and use gyrators to get $u=v_1$, $y=i_2$

Case of voltage transfer function:



Identify: $v_3=x$

$i_2=-gv_{out}=-gy$, $i_{out}=0$, $v_1=u$, i_1=don't care

Semistate Design - V

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} * \\ -gv_{out} \\ -Y_L(s) \end{bmatrix} = \begin{bmatrix} * \\ -gy \\ -sE \end{bmatrix} =$$

$$\begin{bmatrix} * & * & * \\ 0 & 0 & C \\ -B & * & -A \end{bmatrix} \begin{bmatrix} u \\ 0 \\ x \end{bmatrix} = \begin{bmatrix} * & * & * \\ 0 & 0 & C \\ -B & * & -A \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}$$

$$Y_{coupling} = \begin{bmatrix} * & * & * \\ 0 & 0 & C \\ -B & * & -A \end{bmatrix}, \quad *=\text{don't care}$$

Therefore, synthesize $Y_{coupling}$ by VCCSs = differential pairs and load in $Y_L(s)$ = capacitors and opens.

Semistate Design - VI

Again transform with P & Q:

$$YL(s)=sPEQ=sC_{ap}\dot{+}0_{k-c}$$

$$Y_{coupling}=\begin{bmatrix} * & * & * \\ 0 & * & CQ \\ -PB & * & -PAQ \end{bmatrix}$$

Choose the don't care so the coupling admittance is as lossless (skew symmetric as possible and –PAQ as passive as possible. Eventually scale for VLSI.

$$Y_{coupling}=\begin{bmatrix} 0 & 0 & (PB)^T \\ 0 & 0 & CQ \\ -PB & -(CQ)^T & -PAQ \end{bmatrix}$$

Semistate Design - VII

Example:

$$\frac{v_2}{v_1}=\frac{3s^3}{s^2+2s+1}=3s-6+\frac{3s+6}{s^2+2s+1}$$

Realize as the sum of three admittances

For $\frac{3s+6}{s^2+2s+1}$:

$$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}sx_a=\begin{bmatrix}0 & 1\\ -1 & -2\end{bmatrix}x_a+\begin{bmatrix}1\\ 0\end{bmatrix}u$$

$$y_a=\begin{bmatrix}6 & 3\end{bmatrix}x_a$$

For 3s:

$$\begin{bmatrix}0 & 1\\ 0 & 0\end{bmatrix}sx_b=\begin{bmatrix}-1 & 0\\ 0 & -1\end{bmatrix}x_b+\begin{bmatrix}0\\ 1\end{bmatrix}u$$

$$y_b=\begin{bmatrix}-1 & 0\end{bmatrix}x_b$$

For –6:

$$\begin{bmatrix}0\end{bmatrix}sx_c=\begin{bmatrix}-1\end{bmatrix}x_c+\begin{bmatrix}1\end{bmatrix}u$$

$$y_c=\begin{bmatrix}-6\end{bmatrix}x_c$$

Semistate Design - VIII

$$\begin{bmatrix} 1 & 0 & & & & \\ 0 & 1 & & & & \\ & & 0 & 1 & & \\ & & 0 & 0 & & \\ & & & & 0 \end{bmatrix} sx = \begin{bmatrix} 0 & 1 & & & & \\ -1 & -2 & & & & \\ & & -1 & & & \\ & & & -1 & & \\ & & & & -1 \end{bmatrix} x + \begin{bmatrix} 0 \\ 1 \\ 0 \\ 1 \\ 1 \end{bmatrix} u$$

$$y = \begin{bmatrix} 6 & 3 & -1 & 0 & -6 \end{bmatrix} x$$

To get E diagonal we permute the 3rd and 4th columns using

$$P = 1_2 \dot{+} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \dot{+} 1, Q = 1_5$$

Filling in the don't care entries to obtain skew-like symmetry

$$Y_{coupling} = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 6 & 3 & 0 & -1 & -6 \\ 0 & -6 & 0 & -1 & & & \\ -1 & -3 & 1 & 2 & & & \\ 0 & 6 & & & 0 & 1 & \\ -1 & 1 & & & 1 & 0 & \\ -1 & 0 & & & & & 1 \end{bmatrix}$$

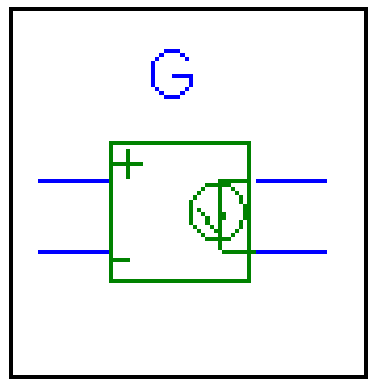
Semistate Design - IX

This is realized by a seven port of differential pairs, some back to back as gyrators. The second port has a gyrator, of gyrator conductance –1, to convert i_2 to $-gv_{out}$. The last 5 ports are loaded with 3 unit capacitors and two open circuits.

Note that the third capacitor could have been placed in parallel with the input but that possibility is outside of this design method (though not outside of semistate theory) since no coupling Y would exist.

Basic VLSI Components

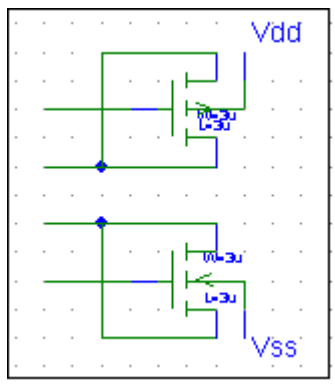
Differential Pair



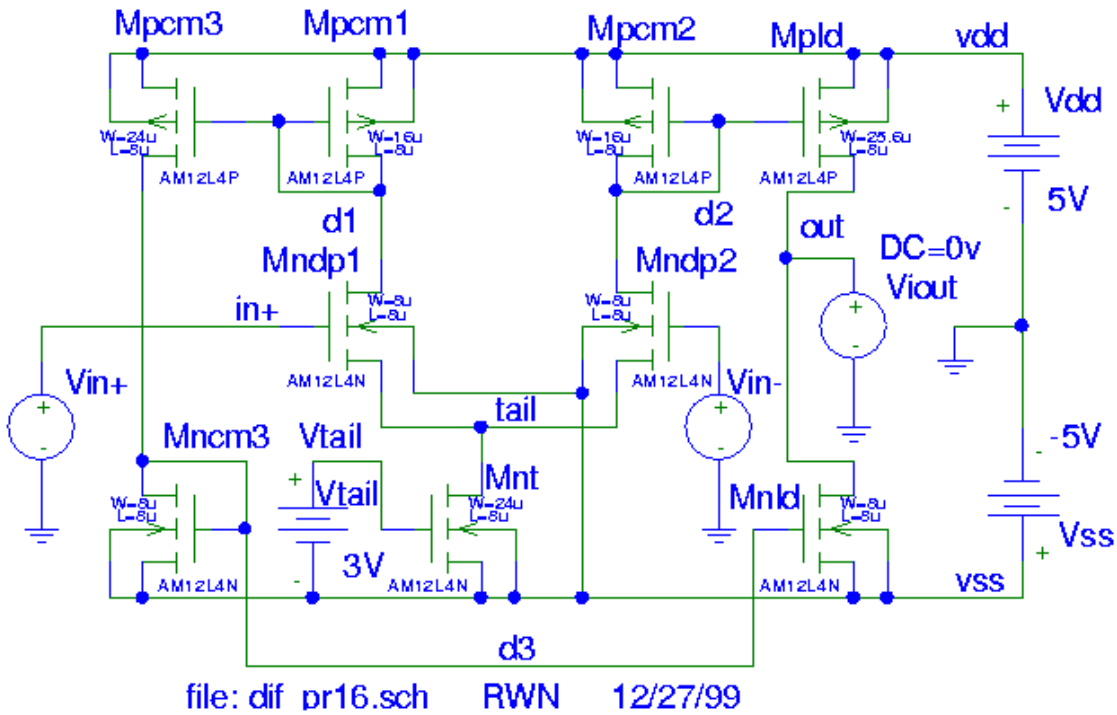
Symbol = VCCS
= Spice G

$$Y = \begin{bmatrix} 0 & 0 \\ G & 0 \end{bmatrix}$$

PMOS & NMOS Capacitors



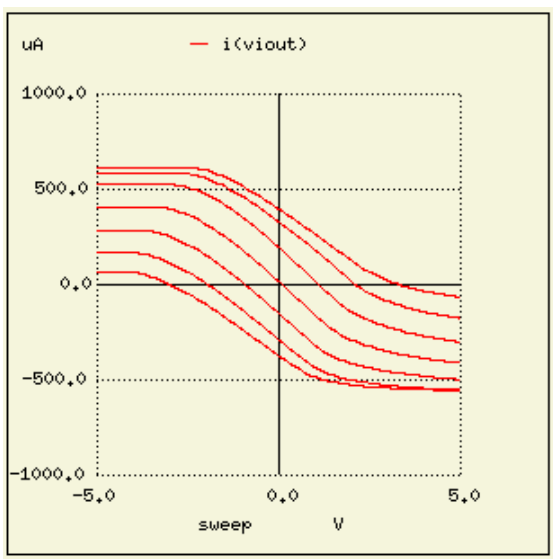
Differential Pair - Circuit



Differential Pair for 1.6u technology & layout

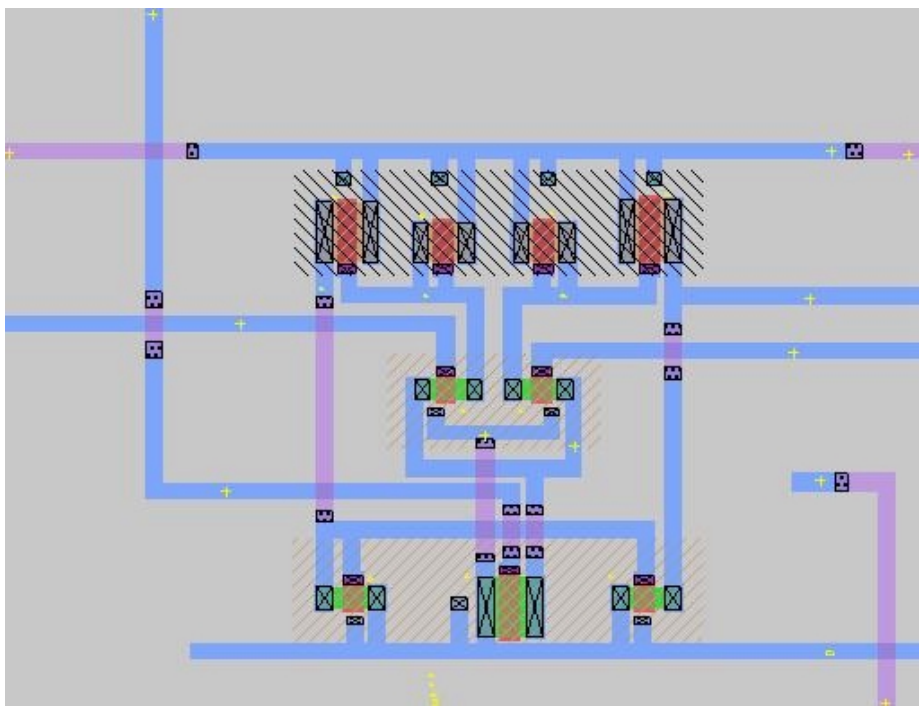
DC analysis: Vin+ -5 to +5, 0.1v steps;
nest: Vin- -5 to +5, 1v steps

Response



Differential Pair - Layout

[Ne3]



LTI Semistate Canonical Form - I

The standard canonical form is

$$\begin{bmatrix} 1_\sigma & 0 \\ 0 & N_{il} \end{bmatrix} \dot{x} = \begin{bmatrix} A_{11} & 0 \\ 0 & 1_{k-\sigma} \end{bmatrix} x + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} u$$

$$y = \begin{bmatrix} C_1 & C_2 \end{bmatrix} x$$

Where N_{il} is nilpotent (or absent if E is nonsingular).

Proof: Rather messy (in Gantmacher [GA2])

$$T(sE-A)T^{-1} = s(E_{ns} \dot{+} E_{nil}) - A_1 \text{ with } A_1 = TAT^{-1}$$

$$= (s-\alpha)(E_{ns} \dot{+} E_{nil}) + \left[\alpha(E_{ns} \dot{+} E_{nil}) - A_1\right];$$

Choose real α such that $\left[\alpha(E_{ns} \dot{+} E_{nil}) - A_1\right]$ is nonsingular. Multiply by inverse of

$$\left[\alpha(E_{ns} \dot{+} E_{nil}) - A_1\right] \text{ then } (sE-A) \Rightarrow$$

$$1_k + (s-\alpha)\left[\alpha(E_{ns} \dot{+} E_{nil}) - A_1\right]^{-1} (E_{ns} \dot{+} E_{nil})$$

LTI Semistate Canonical Form - II

With a new T bring

$$\left[\alpha(E_{ns} \dot{+} E_{nil}) - A_1\right]^{-1} (E_{ns} \dot{+} E_{nil}) \Rightarrow$$

$$F_{ns} \dot{+} F_{nil} \text{ or } sE\text{-}A \Rightarrow$$

$$s\left[F_{ns} \dot{+} F_{nil}\right] - \left[\alpha(F_{ns} \dot{+} F_{nil}) - 1_k\right]$$

Multiply by the inverse of

$$F_{ns} \dot{+} \left[\alpha F_{nil} - 1_{k\text{-}\sigma}\right]$$

Sends sE-A to the desired form

$$(s1_\sigma - [\alpha 1_\sigma - F_{ns}^{-1}]) \dot{+} (s\left[\alpha F_{nil} - 1_\sigma\right]^{-1} F_{nil} - 1_{k-\sigma})$$

LTI Semistate Canonical Form - III

Use in design:

$$1_{c1}x_1(t)=\int_0^t[A_{11}x_1(\tau)+B_1u(\tau)]d\tau+x_1(0)$$

$$x_2(t)=\frac{d(N_{il}x_2(t))}{dt}-B_2u(t)$$

$$y(t)=C_1x_1(t)+C_2x_2(t)$$

For synthesis replace the middle term by its transformed such that the derivative term is diagonal

$$s(1_{c2}\dot{+}0_{k-c1-c2})x_2=A_{22}x_2+B_2u$$

Synthesis can now take place by the use of c1+c2 unit capacitors fed by differential pairs for A_{11}, A_{22}, B_1 and B_2 with u=voltage, y=current.

References

[CA1] S. L. Campbell, "Singular Systems of Differential Equations," Pitman Advanced Publishing Program, San Francisco, 1980. See p. 44 for Drazin inverse solution.

[CA2] S. L. Campbell, "Singular Systems of Differential Equations II," Pitman Advanced Publishing Program, San Francisco, 1982. See p. 16 for the standard canonical form.

[GA1] F. R. Gantmacher, "The Theory of Matrices, volume two" Chelsea Publishing Company, New York, 1959. See p. 28 for the derivation of the standard canonical form

[Ne1] R. W. Newcomb and B. Dziurla, "Some Circuits and Systems Applications of Semistate Theory," Circuits Systems and Signal Processing, Vol. 8, No. 3, 1989, pp. 235 – 260.

[Ne2] R. W. Newcomb, "Semistate Design Theory," Circuits Systems and Signal Processing, Vol. 1, No. 1, 1982, pp. 204 – 216.

[Ne3] http://www.ee.umd.edu/newcomb/VLSI_circuits.htm