All-Pass RF Phase Shifter for Bio-Antennas

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***Abstract*—An RF phase shifter is designed using the all-pass filter topology. The shifter will be used in bio-antenna array circuits for an operating frequency of 1GHz. The phase shifter was simulated using the AMI 0.5µm CMOS technology. Using a 3V voltage supply, two phase shift ranges were achieved with a voltage gain of approximately 5dB. The phase shifting was achieved using an analog bias voltage with voltage range from 0.4V to 0.8V. The maximum power consumption of the phase shifter was 339µW.**

I. INTRODUCTION

Phase shifters are essential building blocks in the design of antenna array transceivers. In the transmitter case, they provide the necessary phase shift for each RF signal in each antenna element to achieve electronic beamforming. The shifter is going to be used to build an antenna array for magnetic field pattern control within the human's brain. There are many types of phase shifter topologies in the literature. In [1] the phase shifter is realized by utilizing a high pass filter topology where the phase shift is achieved by varying a tunable element. In this case a varactor and an active inductor are used for phase adjusting in which a phase shift range of 96° is achieved (from 14° to 110°) at 4 GHz. Reference [2] uses two common source transistors with a capacitor to the gate of one transistor and an inductor connected to each gate of the other to form a combination of highpass-lowpass amplifiers. Phase shifting is achieved by varying the bias voltage (V_{GS}) of the transistors. The inductor is implemented using bondwire interconnects. The phase range achieved is 400°.

The phase shifters in [3] and [4] perform phase shifting using similar methods. They both use a two Gilbert-cell type VGAs (*variable gain amplifiers*) where the gains are controlled by using *digital to analog converters* (DACs). The phase shifting of the signal is achieved by adding the signal to a 90° phase shifted replica of it (I & Q components) with proper gains in the current domain. In [5] the phase shifter is designed by using a ring oscillator with phase-locked loop architecture to achieve phase shifting.

In this paper a new phase shifter is designed using the all-pass filter topology utilized in [6]. It is important to mention that the design strategy followed in [6] yielded phase shifting but not at high RF frequencies so therefore it was necessary to try and follow a different approach to sustain phase shifting at high frequencies (1 GHz and above). The phase shifter is utilized by using MOS technology with fixed valued capacitors and resistors. No inductors are needed which is a big advantage when considering the different issues in designing on chip inductors such as quality factor, losses and bandwidth associated with the inductor. Another advantage is that gain control through DACs is not needed which will lead to a great deal of simplification when considering circuit design. Phase shifting is accomplished in an analog manner by simply changing the bias gate voltage of a transistor (shown later).

II. THEORY

The main idea of this phase shifter was presented in [6] and it works by first considering the simple circuit in Fig. 1. The circuit shows a simple RC circuit in which the voltage v_x across the capacitor is given by equation (1) in the Laplace transform s-domain.

$$v_x(s) = \frac{v_{in}(s)}{1+sRC} \tag{1}$$

Where v_{in} is the input signal, R is the resistance, $s=j\omega$ (ω frequency) and C is the capacitance. One can realize a first order all-pass filter if the following equation can be accomplished.

$$v_o(s) = 2v_x(s) - v_{in}(s) = \frac{1-sRC}{1+sRC}v_{in}(s) \tag{2}$$

Where v_o is the desired output voltage that will allow phase shifting. If (2) can be realized then the phase difference (Φ) between the output and input voltage signal is given by (3).

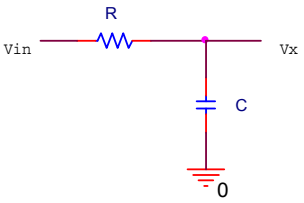

Fig. 1. RC Circuit to be used for the All-Pass Filter.

$$\Phi = -2\tan^{-1}(\omega RC) \tag{3}$$

Phase shifting is achieved by varying the resistance, capacitance or both. It is clear from (3) that the maximum phase shift that can be achieved by this topology is 180° (theoretically), therefore to extend the shifting to 360° another equation should be realized.

$$v_o'(s) = v_{in}(s) - 2v_o(s) = \frac{sRC-1}{sRC+1}v_{in}(s)$$
$$\Phi' = -\pi - 2\tan^{-1}(\omega RC) \tag{4}$$

From (4) it is clear how the other 180° phase shift can be obtained.

The approach taken in this paper is to try and select circuit topologies that are known to have high upper frequency values such as the common gate MOSFET since the gate-to-drain capacitance is shorted at one end and so it will not cause feedback problems from output to input at high frequencies. The circuit topology used in this paper is shown in Fig. 2. As it can be seen M1 is an NMOS transistor connected in the common gate configuration (to improve performance at high frequencies) with the input small-signal connected to its source and output drain connected to a diode connected PMOS transistor M2. M2 is diode connected because it is desired to connect a load to M1 that gives a conductance equal to half the transconductance of M1.

When considering the small-signal model for transistors M1 and M2 and solving for the output voltage seen from the drain of M1, one can derive the following expression.

$$\frac{v_{m1d}}{v_{in}} = \frac{\dfrac{g_{m1}+g_{o1}}{g_{m2}+g_{o1}+g_{o2}}}{1+\dfrac{s(C_{gd1}+C_{gs2})}{g_{m2}+g_{o1}+g_{o2}}} \approx \frac{\dfrac{g_{m1}}{g_{m2}}}{1+\dfrac{s(C_{gd1}+C_{gs2})}{g_{m2}}} \tag{5}$$

Where v_{m1d} is the voltage at the drain of M1, g_{m1} and g_{m2} are the transconductance of M1 and M2 respectively, g_{o1} and g_{o2} are the Early conductances of M1 and M2 respectively, C_{gd1} is the gate-to-drain capacitance of M1 and C_{gs2} is the gate-to-source capacitance. Note that in (5) it is assumed that $g_{m1}>>g_{o1}$ and $g_{m2}>>g_{o1}+g_{o2}$. By using two comparators or difference circuits the desired output voltages could be realized and are given by the following expressions.

$$\frac{v_{o1}}{v_{in}} = \alpha_1 \frac{\dfrac{g_{m1}}{g_{m2}} - \dfrac{s(C_{gd1}+C_{gs2})}{g_{m2}} - 1}{\dfrac{s(C_{gd1}+C_{gs2})}{g_{m2}}+1} \tag{6}$$

$$\frac{v_{o2}}{v_{in}} = \alpha_2 \frac{\dfrac{s(C_{gd1}+C_{gs2})}{g_{m2}} + 1 - \dfrac{g_{m1}}{g_{m2}}}{\dfrac{s(C_{gd1}+C_{gs2})}{g_{m2}}+1} \tag{7}$$

Where α_1 and α_2 are the small-signal voltage gains of the comparators circuits (see later). By setting $g_{m2}=g_{m1}/2$, two first order all-pass filters similar to those in (2) and (4) will be realized where input/output transfer function and phase difference are given by (8) and (9).

$$\frac{v_{o1}}{v_{in}} = \alpha_1 \frac{1-\dfrac{s2(C_{gd1}+C_{gs2})}{g_{m1}}}{1+\dfrac{s2(C_{gd1}+C_{gs2})}{g_{m1}}}$$
$$\Phi_1 = -2\tan^{-1}\left(\frac{2\omega(C_{gd1}+C_{gs2})}{g_{m1}}\right) \tag{8}$$

$$\frac{v_{o2}}{v_{in}} = -\frac{\alpha_2}{\alpha_1}\frac{v_{o1}}{v_{in}}$$
$$\Phi_2 = -\pi - 2\tan^{-1}\left(\frac{2\omega(C_{gd1}+C_{gs2})}{g_{m1}}\right) \tag{9}$$

Phase shifting is accomplished by varying V_{BIAS} of transistor M1 which in turn will vary g_{m1} and g_{m2} according to equation (10) as long as the dimension relationship between M1 and M2 in (11) is satisfied. Note that there are two regions of operation in which M1 and M2 simultaneously operate in and these are the saturation (V_{BIAS}-$R_{BIAS}I>V_{t1}$) and subthreshold (V_{BIAS}-$R_{BIAS}I<V_{t1}$), thus the two different equations for expressing g_m.

$$g_{m1}^{saturation} = k_n\left(\frac{W}{L}\right)_1(V_{BIAS}-R_{BIAS}I-V_{t1})$$
$$g_{m1}^{subthreshold} \approx \frac{I_o}{V_T}\exp\left(\frac{V_{BIAS}-R_{BIAS}I}{V_T}\right) \tag{10}$$

$$\left(\frac{W}{L}\right)_2 = \frac{1}{4}\frac{k_n}{k_p}\left(\frac{W}{L}\right)_1 = \frac{1}{4}\frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_1 \tag{11}$$

Where V_{BIAS} is the gate voltage of M1, R_{BIAS} is the resistor connected to the source of M1 to allow a dc path to ground, I is the dc current running of M1 and M2, V_{t1} is the threshold voltage of M1, W is the MOSFET channel width, L is the MOSFET channel length, k_n and k_p are the PSPICE parameters, μ_n and μ_p are the electron and hole mobilities respectively, I_o is the subthreshold saturation current and V_T is the thermal voltage. Note as long as (11) is satisfied g_{m2} is always going to be half of g_{m1} for all values of V_{BIAS} since M1 and M2 share the same current (I) and therefore only

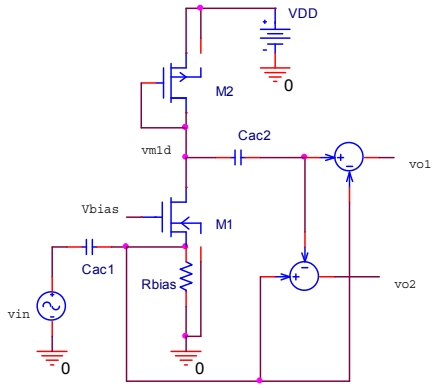

Fig. 2. Circuit Topology for the First Order All-Pass Filter.

the design parameters are going to affect the relationship between g_{m1} and g_{m2}.

It is important to note that the capacitors C_{ac1} and C_{ac2} are both used for appropriate dc blocking such that the inputs to the comparators are only small signal thus it will not interfere with the biasing of the comparator. Also C_{ac1} will allow for correct dc biasing of the circuit of M1 and M2 without any interruption from the small-signal input signal v_{in}.

The comparator circuits are accomplished by using a differential-to-single ended amplifier with active PMOS current-mirror load like the one shown in Fig. 3 (Note that Fig. 3 only shows the two comparators used for the realization of the phase shifter, not the entire circuit. The inputs of the comparators are v_{m1d} and v_{in}). An additional advantage of using these amplifiers is that they can be designed to provide amplification in the output voltage with the desired phase shift. As it can be seen from Fig. 3, the differential inputs are applied to NMOS transistors M3, M4, M8 and M9 (which form the differential pair) and the output is taken from the drains of M4 and M9. Assuming that the differential pairs are perfectly matched and operate with equal dc currents, as do the current-mirror loads (M5, M6, M10 and M11), then the small-signal transconductances are $g_{m3}=g_{m4}=g_{m8}=g_{m9}=g_{m(dp)}$ ($g_{m(dp)}$ is defined as the differential pair transconductance) and $g_{m5}=g_{m6}=g_{10}=g_{m11}=g_{m(mir)}$ and the output current i_o is given by [7].

$$i_{out1} = g_{m(dp)}(v_{m1d} - v_{in}); i_{out2} = -i_{out1} \qquad (12)$$

Now depending on the designer's requirements, the output currents are going to be fed to the input stage of the next circuit component (in most cases a power amplifier). If a voltage amplification stage is necessary for some reason, then this can be provided by selecting a high resistance load (R_o) where all the output currents will sink into and so give the following output voltage (here only v_{o1} is considered).

$$v_{o1} = g_{m(dp)}(R_o \,||\, r_{o4} \,||\, r_{o6})(v_{m1d} - v_{in}) \qquad (13)$$

Where r_{o4}, and r_{o6} are the Early resistances of transistors M4 and M6 respectively (a similar analysis can be made for

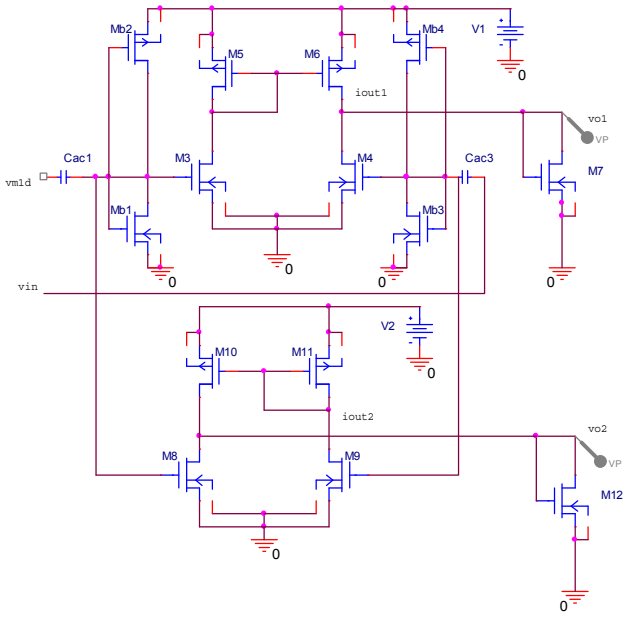

Fig. 3. The two differential-to-single ended amplifiers to realize the voltage differences needed.

v_{o2}). On the other hand, if an ideal first order all-pass filter response is needed (i.e. no voltage gain) then one can terminate the output of the amplifiers with diode-connected NMOS transistors (M7 and M12) and in this way the output voltages of the amplifier and the entire circuit are given by (14).

$$v_{o1} = g_{m(dp)}\left(\frac{1}{g_{m7}} \,||\, r_{o4} \,||\, r_{o6}\right)(v_{m1d} - v_{in})$$

$$\approx \frac{g_{m(dp)}}{g_{m7}}(v_{m1d} - v_{in}) \approx (v_{m1d} - v_{in}) \qquad (14)$$

$$v_{o2} \approx \frac{g_{m(dp)}}{g_{m12}}(v_{in} - v_{m1d}) \approx (v_{in} - v_{m1d})$$

In theory, it is desired to set the transconductances of transistors M7 and M12 to be equal to those of M3, M4, M8 and M9. It was evident from the PSPICE simulation that under the prior conditions the voltage gain at 1GHz suffers a drop of around 3dB. Therefore, g_{m7} and g_{m12} were set smaller than those for M3, M4, M8 and M9 to compensate for this voltage gain drop. As it is clear from (14) that if $g_{m7,12}<g_{m(dp)}$ a voltage gain is sustained.

III. PSPICE SIMULATION RESULTS

The phase shifter was designed and simulated in PSPICE using the AMI 0.5µm technology. The voltage supply used was 3V and also the control voltage supplies for the comparators in Fig. 3 (V_1 and V_2). The transistor dimensions for M1 and M2 are (10µm/0.5µm) and (7µm/0.5µm). The transistors M3-M11 all have dimensions (1µm/0.5µm) while the bias transistors Mb1-Mb4 have

dimensions of (1μm/10μm). The dc blocking capacitors C_{ac1}, C_{ac2} and C_{ac3} have values of 1μF.

Since the phase shifting is applied through the varying V_{BIAS} of transistor M1, the power consumption of the phase shifter will also vary with the desired phase shift. The maximum power consumption of the phase shifter when a phase shift from 0^o to 180^o is desired is 332μW, on the other hand, when a phase shift between 180^o to 360^o is desired the consumption is 339μW.

There were two phase shift ranges realized by the phase shifter and these were -93.4^o to -174.6^o ($\Delta\Phi_1 \approx 81.2^o$) and -231.4^o to -363.0^o ($\Delta\Phi_2 \approx 131.6^o$) (see Fig. 6). The voltage gain resulting from the phase shift for all cases was around 5dB at 1GHz.

Figures 4 and 5 show the voltage gain characteristics for v_{o1} and v_{o2} respectively. Figure 6 shows the phase characteristics for v_{o1} and v_{o2}. As it can be seen from Figures 4 and 5, the voltage gain at dc is not 0 dB and this is because of the reason explained in Section II. From Figure 6 it is clear how the phase shifter covers the two phase ranges $-93.4^o > \Phi_1 > -174.6^o$ and $-231.4^o > \Phi_2 > -363.0^o$ specified in the previous paragraph. Also an important remark is that for V_{BIAS} values of 0.5V and 0.6V there is a large phase change present since here M1 is in subthreshold and any change in V_{BIAS} will result in an exponential change in the transconductance g_{m1}, hence a larger phase change.

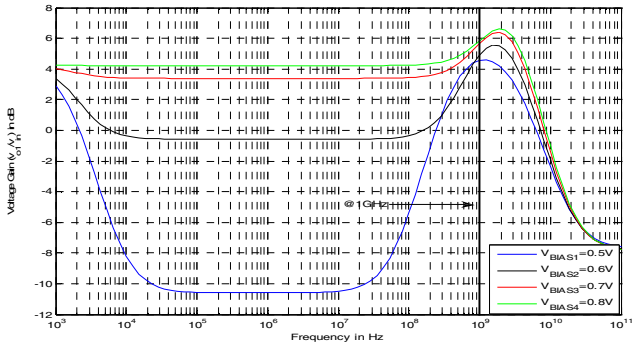

Fig. 4. Voltage Gain versus Frequency for v_{o1}.

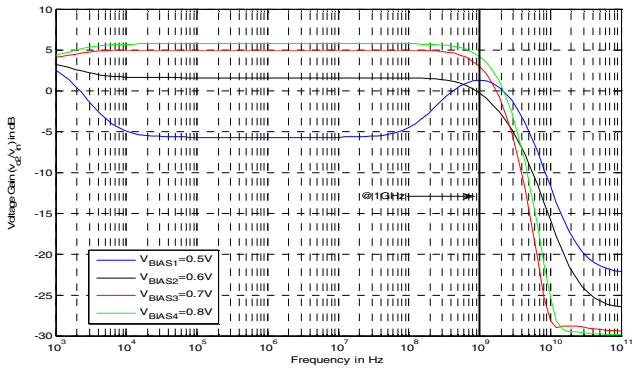

Fig. 5. Voltage Gain versus Frequency for v_{o2}.

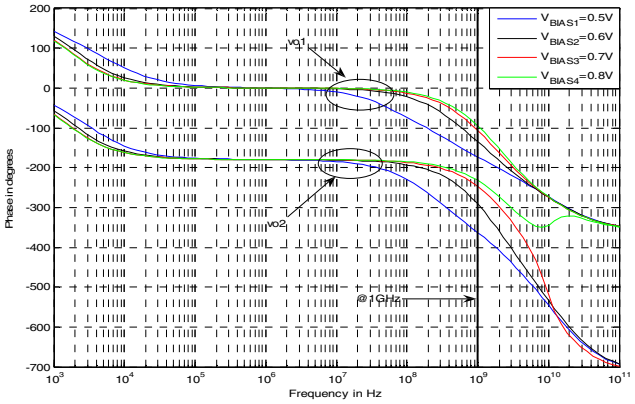

Fig. 6. Phase Response versus Frequency for v_{o1} & v_{o2}.

For V_{BIAS} values of 0.5V and 0.6V (subthreshold), there is a severe voltage gain drop in the frequency range ~10^4 Hz to 10^8 Hz and this is because the value of g_{m1} is small and therefore the Early conductances in (5) cannot be ignored anymore for that frequency range.

IV. Conclusions

An RF phase shifter, to be used in a bio-antenna array circuit, is designed to operate at 1GHz. The phase shifter uses the all-pass filter topology and is designed using CMOS transistors without the need to use any inductors (on-chip or off-chip) or varactors. The phase shifting is adjusted using an analog bias voltage with maximum power consumption of 339μW while achieving two phase shifting ranges of -93.4^o to -174.6^o and -231.4^o to -363.0^o with a voltage gain of around 5dB (@ 1GHz).

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