An Adjustable CMOS Floating Resistor

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***Abstract*— A floating node resistor has a wide range of usage in analog integrated circuits. In this paper, we propose a new CMOS linear floating resistor circuit which is based on a transconductor circuit. The proposed circuit topology is capable of implementing both positive and negative resistance. The introduced floating resistor has simple circuit implementation and its resistance is tunable by adjusting the gate voltage of a MOS transistor. PSpice simulation results show that the example circuit made by AMI 1.5 μm CMOS process presents a constant resistance of 2.6 $M\Omega$ to 5.1 $M\Omega$ when the adjust voltage ranges from -3.4 V to -2.4 V and the corresponding adjusted current is 16 μA to 57 μA, with $\pm 5V$ voltage supplies. The cutoff frequency is about 1 MHz.**

I. Introduction

Floating resistors in silicon technology can be found in applications such as continuous-time filters, amplifiers, artificial neural networks (ANN), etc. Passive resistors made with polysilicon or diffusion area have disadvantages of sensitivity to temperature and consequently poor stability in values, low sheet resistance and area inefficiency. Thus, various active resistor circuits have been proposed for replacing inaccurate passive resistors [1]-[6]. In [1], a linear floating resistor that was composed of two enhancement-type PMOS transistors was presented. [2][3] introduced floating resistors that were based on current conveyors and their resistances depended on the thermal voltage. [4] summarized two commonly used circuit configurations for realizing floating resistors, and presented a floating resistor tunable by two voltage supplies, which provided currents to the sources of input transistors. [5] described a floating resistor circuit which was based on the linear relationship of I_{ds} vs. V_{ds} of a MOS device working in the linear region, and some other MOS transistors, working in the saturation region, served as voltage shifters to compensate the variation in the gate voltage of the device that works in the linear region.

In this paper, a new CMOS circuit for realizing floating resistor is introduced. The circuit uses a linear transconductor modified to provide two copies of output currents. The currents are equal in magnitude and opposite in direction. The proposed floating resistor is simple in circuit configuration. Its resistance is adjustable by controlling the gate voltage of a MOS transistor, and can be selected to be positive or negative by changing feedback connections.

The rest of the paper is organized as follows. Section II presents the approach of constructing the proposed floating resistor using a modified ideal transconductance component. Section III describes the CMOS circuit we use to realize the floating resistor. PSpice simulation results are introduced and the influences of the body effect on the floating resistor is discussed in Section IV. Finally, conclusions are drawn in Section V.

II. Ideal Component Description

The implementation of the proposed floating resistor using a linear transconductor is illustrated in Figure 1. The electrical symbol with g_m on it represents an ideal operational transconductance amplifier (OTA) modified to have two outputs. A common transconductance circuit has two terminals V_+ and V_- for taking input voltages and an output terminal I_o for sinking current. As an ideal transconductance, no currents are allowed to flow through the input ports, and the output voltage can be any value, dependent on its loading circuit by $V_{out} = R_{load} \times I_o$. The output current and the input voltages have the relation that is described as:

$$I_o = g_m(V_+ - V_-), \tag{1}$$

where g_m is the transconductance. The transconductance block shown in Figure 1 has two output currents. The one with positive sign is the same as the I_o in equation (1), and the one with negative sign is identical in magnitude but opposite in direction. The positive and the negative output currents are fedback to provide currents to the input terminals, as depicted in the figures, and the value of the currents are proportional to the difference of the input voltages, as described by equation (1). Thus, the circuit behaves exactly the same as a linear resistor with two terminals V_+ and V_-.

Figure 1(a) depicts the circuit configuration for a positive resistance $1/g_m$. To implement a negative resistor, we only need to switch the connections between the outputs and inputs, as illustrated in Figure 1(b).

III. CMOS Circuit Realization

One of the techniques to implement a linear transconductance is using differential pairs as shown in Figure 2 [7](pp. 532). Here we assume that the bodies of the transistors are connected to their sources. The body effect on the threshold voltages will be discussed in Section IV. $M1$ and $M2$ are the NMOS input stage, whose tail current I_{adj} is provided by the current sink transistor $M9$. The current distribution in the two input transistors $M1$ and $M2$ is controlled by their gate voltages, and these two currents are transmitted to the output stage by current mirrors that are composed of $M3 - M8$. The output I_o current is the difference between the two currents passing through transistors $M6$ and $M8$. By varying the sink current I_{adj}, and the amplification factors of

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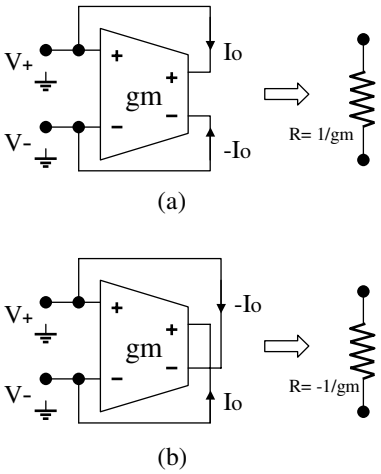

Fig. 1. Floating resistor circuit based on modified linear transconductance. (a) Positive resistor. (b) Negative resistor.

the current mirrors, the transconductance of the differential pair can be adjusted.

Assume that $M1$ and $M2$ are identical and both working in the saturation region, neglecting the channel length modulation, the source currents of $M1$ and $M2$ are expressed by:

$$I_{M1} = K_{1,2}(V_{gs1} - V_{tn})^2 = K_{1,2}(\Delta V + V_{gs2} - V_{tn})^2, \quad (2)$$

$$I_{M2} = K_{1,2}(V_{gs2} - V_{tn})^2, \quad (3)$$

where V_{tn} is the threshold voltage of NMOS transistors, ΔV is the difference between the two voltage inputs:

$$\Delta V = V_+ - V_- = V_{gs1} - V_{gs2}, \quad (4)$$

and $K_{1,2}$ is the fabrication-dependent parameter of $M1$ and $M2$. The fabrication-dependent parameter K of a transistor is decided by the transistor aspect ratio W/L, electron mobility μ_0, and gate oxide capacitance C_{OX}:

$$K = \frac{1}{2}\frac{W}{L}\mu_0 C_{OX}. \quad (5)$$

From equations (2) and (3), we can derive the following equations by using $I_{adj} = I_{M1} + I_{M2}$:

$$I_{M1} = \frac{1}{2}\left(I_{adj} + K_{1,2}\Delta V\sqrt{\frac{2I_{adj}}{K_{1,2}} - \Delta V^2}\right), \quad (6)$$

$$I_{M2} = \frac{1}{2}\left(I_{adj} - K_{1,2}\Delta V\sqrt{\frac{2I_{adj}}{K_{1,2}} - \Delta V^2}\right). \quad (7)$$

Therefore, the transconductance of the circuit is expressed by:

$$g_m = \frac{I_{M8} - I_{M6}}{\Delta V} = A\frac{I_{M1} - I_{M2}}{\Delta V} = AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}} - \Delta V^2}, \quad (8)$$

where A is the amplification factor of the current mirrors composed of $M3 - M8$, and $M4$ and $M6$, i.e. $A = (I_{M8} : I_{M1}) = (I_{M6} : I_{M2})$. When ΔV^2 is much smaller than $2I_{adj}/K_{1,2}$ and is ignored, g_m is a constant $A\sqrt{2K_{1,2}I_{adj}}$.

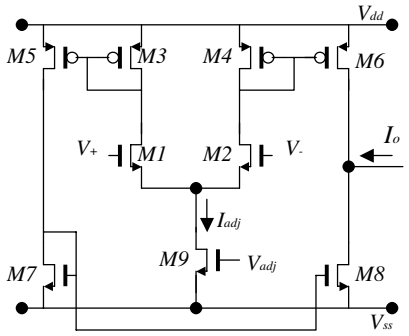

Fig. 2. CMOS differential pair circuit.

The input terminals of the differential pair are the gates of $M1$ and $M2$ and consequently take nearly no currents, and, thus, the circuit in Figure 2 works as a linear transconductor.

Equations (2)-(8) are satisfied under the condition that all the transistors in Figure 2 work in the saturation region. Input voltages can not be too high in order to let $M1$ and $M2$ meet this constraint, expressed in equation, $V_{gs} - V_t < V_{ds} \Rightarrow V_{gd} < V_t$. Considering that the gate voltages of $M1$ and $M2$ are the input voltages, and their drain voltages can be derived from $M3$ and $M4$, we can find the upper bound limit on V_+ and V_- referenced to ground:

$$V_+ < V_{dd} - V_{tn} - V_{tp} - \sqrt{\frac{I_{M1}}{K_3}}, \quad (9)$$

$$V_- < V_{dd} - V_{tn} - V_{tp} - \sqrt{\frac{I_{M2}}{K_4}}. \quad (10)$$

The lower bound limit of the input voltages exists because of the saturation working requirement on $M9$. By using $V_{gd} < V_t$ on $M9$, we can derive:

$$V_+ (or\ V_-) > V_{adj} - 2V_{tn} + \sqrt{\frac{I_{adj}}{K_9}}. \quad (11)$$

In order to let the differential pair in Figure 2 work as a linear transconductance, ΔV needs to be limited into a certain range. Ignoring the slight changes in I_{adj} caused by the variation of V_{ds9}, the non-linearity of the transconductance relies on the term ΔV^2 in equation (8). Take a Taylor series expansion on the square root of equation (7) and take an approximation by ignoring high order terms, we have:

$$g_m = AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}}}\left(1 - \frac{K_{1,2}\Delta V^2}{2I_{adj}}\right)^{1/2} \approx AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}}}\left(1 - \frac{K_{1,2}\Delta V^2}{4I_{adj}}\right), \quad (12)$$

where, the first part of the right side of the equation $AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}}}$ is a constant, and the second part $AK_{1,2}\sqrt{\frac{2I_{adj}}{K_{1,2}}}\frac{K_{1,2}\Delta V^2}{4I_{adj}}$ varies along ΔV, and, thus, causes a nonlinearity. Given the maximum allowable transconductance difference in ratio η, i.e. $\eta = max[(g_{m0} - g_m)/g_{m0}]$ where g_{m0} is the transconductance at $\Delta V = 0$, and g_m is an arbitrary

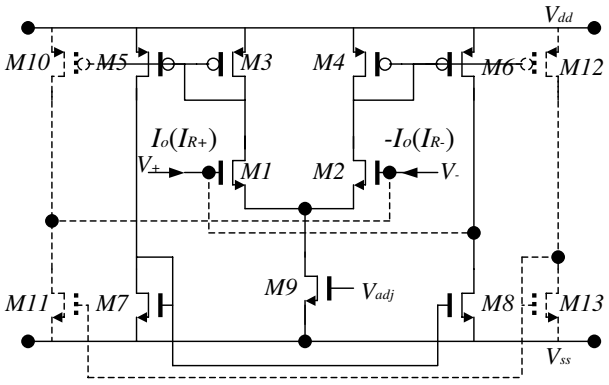

Fig. 3. CMOS linear floating resistor.

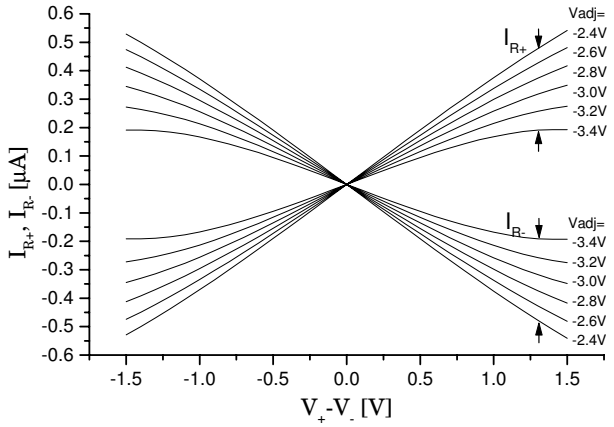

Fig. 4. I-V characteristic of proposed floating resistor. I_{R+} and I_{R-} are the currents that flow into two different resistor terminals (refer to Figure 3). V_- is fixed to 0V. V_{adj} ranges from -3.4V to -2.4V, with a step of 0.2V.

transconductance, from equation (12), we can derive the range of ΔV:

$$\frac{K_{1,2}\Delta V^2}{4I_{adj}} < \eta \quad \Rightarrow \quad \Delta V^2 < \eta\frac{4I_{adj}}{K_{1,2}}. \tag{13}$$

Hence, according to equation (13), in order to achieve a good linearity of the transconductance, the magnitude of the differential input ΔV needs to be kept much smaller than $I_{adj}/K_{1,2}$, or at the same ΔV, I_{adj} can be enlarged, under the restriction that all transistors are still in the saturation region, described by equations (9)-(11).

To the presented differential pair circuit can be easily added another current output to serve as the modified linear transconductance described in Section II. Then, following the method introduced earlier, a positive floating resistor can be realized by connecting the inputs and outputs of the differential pair. This is illustrated in Figure 3. The transistors and wires drawn with dotted lines are newly added upon the circuit shown in Figure 2. The added transistors make the circuit topology of the left side and the right side perfectly symmetrical. When $V_+ > V_-$, the current flowing into the V_+ port is provided by $M6$ and $M8$, and the current flowing out of the V_- port is sourced from $M10$ and $M11$. The circuit configuration in Figure 3 shows the case of a positive resistance, which is, from equation (12), expressed by:

$$\begin{aligned} R &= \frac{1}{g_m} \approx \frac{1}{A\sqrt{2K_{1,2}I_{adj}}} \\ &= \frac{1}{A(V_{adj}-V_{ss})\sqrt{2K_{1,2}K_9}}. \end{aligned} \tag{14}$$

To obtain a negative resistance, we only need to switch the feedback connections in the circuit in Figure 3, following the way illustrated in Figure 1(b).

IV. Simulation Results and Discussion

PSpice simulations were carried out for the proposed floating resistor circuit. AMI 1.5 μm N-well CMOS technology provided by MOSIS is used in simulations. Power supplies are $V_{dd} = 5V$ and $V_{ss} = -5V$. The proposed resistor circuit, being non-ideal two-terminal devices, can experience current differences in two terminals, that is the current flowing into V_+ is different from the current flowing out of V_- due to the impact from the external circuits. This happens when the currents in the output transistors in Figure 3 do not mirror properly the currents decided by the input stage. Hence, good current mirrors are important to ensure the resistor properties of the circuit, and, thus, cascode current mirrors [8](pp. 281) are employed for our simulation.

TABLE I

$W{:}L$ used in PSpice simulation. $\Delta = 0.8\mu m$.

$M1$, $M2$	$M3$, $M4$	$M5$, $M6$, $M10$, $M12$	$M7$, $M8$, $M11$, $M13$	$M9$
10Δ:30Δ	79Δ:8Δ	8Δ:37Δ	10Δ:10Δ	10Δ:15Δ

In our simulation, the proposed floating resistor circuit is configured to have a positive resistance (refer to Figure 3). The MOS parameters of level 7 are used in PSpice. The sizes of the transistors are provided in Table I. In the table, except $M1$, $M2$, and $M9$, for all the other MOS devices, each one is replaced by two transistors because cascode current mirrors are used. Figure 4 shows the I-V characteristic of the simulated CMOS floating resistor. V_- is fixed to ground, and V_+ is scanned to achieve the voltage change across the circuit. The two groups of curves in this figure are the currents flowing into two different resistor terminals. With V_{adj} scanned from -3.4 V to -2.4 V, the simulated circuit presents a resistance from 2.6 $M\Omega$ to 5.1 $M\Omega$ in the linear working region. The resistances at different V_{adj} are provided in Table II. Figure 5 illustrates the frequency response of the floating resistor. The DC components of the inputs are set to $V_+ = V_- = 0V$. An AC signal is provided at V_+ and its magnitude is 0.1 V. All the curves in Figure 5 shows an up-turn at around 1 MHz. This can be caused by the parasitic capacitances C_{gd} of $M1$ and $M2$, which short high-frequency signals and consequently introduce a zero in the frequency response. By adjusting V_{adj} to I_{M9}, the transconductances of MOS devices $M1$-$M4$ are enlarged, so that the zero as well as the pole is slightly shifted to a higher frequency. This is illustrated in Figure 5.

The discussion in Section III ignores the body effect, though it is included in the simulation. Since N-well technology is used in our simulation circuit, PMOS transistors can be in

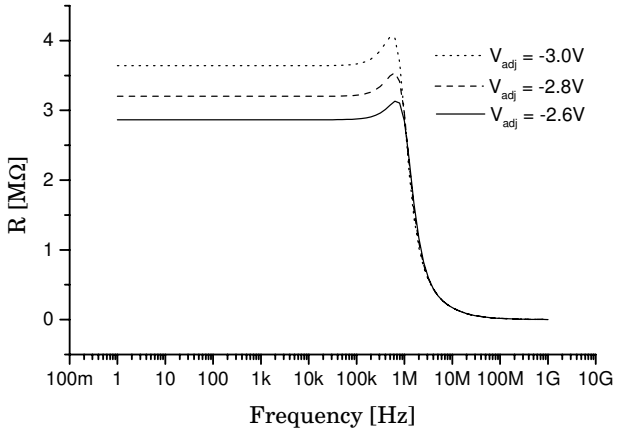

Fig. 5. Frequency response of the CMOS resistor current.

separate wells and their bodies can be tied to their sources to cancel the body effect. The bodies of NMOS transistors are all connected to V_{ss}. This introduces the body effect to the NMOS devices that are not sourced to V_{ss}, i.e. the two input transistors, and the upper part of the transistors that compose cascode current mirrors. For the sake of clarity, Figure 6 shows the NMOS transistors that are affected by the body effect, namely, $M7'$, $M8'$, $M11'$ and $M13'$. The existence of the body effect helps to reduce the current mirror output current change caused by the channel-length modulation effect. Take $M8$ and $M8'$ in Figure 6 as an example, when the current mirror output V_a increases, the gate-source voltage of $M8'$ decreases, which leads to the enhancement of $M8'$ threshold voltage due to the body effect and consequently causes a larger gate-source voltage of $M8'$. This negative feedback on the gate-source voltage of $M8'$ helps to reduce the change on V_b, assuming V_c depends on $M7'$ only and is fixed, and, thus, assists to minimize the output current change. This reducing influence of the body effect on current mismatch is also applicable to PMOS cascode current mirrors. Therefore, to save layout areas, all PMOS transistors of cascode current mirrors can connect their bodies to V_{dd} to enable them sharing a single N-well.

While the input transistors $M1$ and $M2$ are also influenced by the body effect, the changes on their threshold voltages are equal and cancel each other, because their sources are connected to the same point. Therefore, equation (12) is still satisfied, and the resistance of the floating resistor shown in Figure 3 remains expressed by equation (14). However, since the body effect increases the threshold voltages, the dynamic range of input voltages for satisfying the saturation working condition becomes less, and equations (9)-(11) are changed to the following as a result:

$$V_+ < V_{dd} - V_{tn1,2} - V_{tp3} - V_{tp3'} - 2\sqrt{\frac{I_{M1}}{K_3}}, \qquad (15)$$

$$V_- < V_{dd} - V_{tn1,2} - V_{tp4} - V_{tp4'} - 2\sqrt{\frac{I_{M2}}{K_4}}, \qquad (16)$$

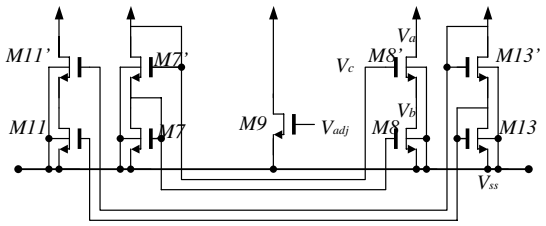

Fig. 6. Cascode current mirrors composed of $M7$, $M7'$, $M8$, $M8'$, $M11$, $M11'$, $M13$, and $M13'$ replace the current mirrors composed of $M7$, $M8$, $M11$, and $M13$ in Figure 3.

TABLE II

RESISTANCE OF FLOATING RESISTOR AT DIFFERENT V_{adj}.

V_{adj}(V)	-2.4	-2.6	-2.8	-3.0	-3.2	-3.4
R ($M\Omega$)	2.6	2.8	3.2	3.6	4.2	5.1

$$V_+(or\ V_-) > V_{adj} - V_{tn1,2} - V_{tn9} + \sqrt{\frac{I_{adj}}{K_9}}, \qquad (17)$$

where $V_{tn1,2}$ is the threshold voltage of $M1$ and $M2$, and V_{tp3} and $V_{tp3'}$, and V_{tp4} and $V_{tp4'}$ are for the PMOS transistors that compose the 2-level PMOS cascode current mirrors and replace $M3$ and $M4$ in Figure 3.

V. CONCLUSIONS

A scheme of making a transconductance-based floating resistor has been proposed, and a floating resistor circuit using a differential pair has been presented. The introduced circuit has a simple topology and can be configured to work as either a positive or negative resistor. The simulation results of an example setup are provided to show that the proposed floating resistor can achieve a resistance of around 2.6 to 5.1 $M\Omega$, and can be adjusted with the gate voltage of a current source MOS transistor. The analysis of the body effect shows that the body effect has little influence on the proposed floating resistor circuit.

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