Phase Noise Optimization of A Symmetric CMOS LC VCO

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***Abstract*— A new approach to the design of CMOS LC-tank VCO with flicker noise upconversion optimization is proposed. The key idea is to get good phase noise performance using a symmetric and balanced circuit, which can be realized with equal transconductance and approximately equal parasitic capacitance of PMOS and NMOS transistors in the complementary cross-coupled LC VCO. The linear-time variant mode is used for prediction of the phase noise performance in the $1/f^3$ region. The impact on the phase noise of employing the equal transconductance and approximately equal parasitic capacitance of PMOS and NMOS transistors is analyzed. Moreover, the effect of the tail current for the reduction of phase noise is addressed. Simulated phase noise of -95.16 dBc/Hz at 100 kHz offset for the modified VCO, is compared with the simulated phase of -93.68 dBc/Hz at 100 kHz for the normal complementary cross-coupled VCO. The two LC VCOs are realized in 0.18 μm CMOS process with a 3 V power supply.**

I. Introduction

LC voltage-controlled oscillators (VCOs) play a very important role in radio frequency transceivers. A number of research efforts have been made to develop the fully integrated CMOS LC VCOs [1]–[3]. It is still a challenge to improve phase noise performance and reduce power consumption. The $1/f^3$ phase noise, which is close in to the carrier, is mainly the upconverted flicker noise of MOS transistors. Without a good design structure, the phase noise performance is severely affected by the flicker noise.

This paper focuses on the trade-offs involved in the design of a symmetric CMOS LC VCO for flicker noise optimization. The impact on the phase noise of employing the equal transconductance and parasitic capacitance of PMOS and NMOS transistors in the complementary cross-coupled LC VCO is investigated. The linear-time variant model [2] is used for prediction of the phase noise performance in the $1/f^3$ region. Analysis on the effect of phase noise due to the symmetry and balance properties of the circuit is carried out. Based on these results the circuit is optimized for low phase noise performance. The simulation results are in agreement with the theoretical analysis. The technique of using the symmetric circuit to reduce the flicker noise upconversion around the carrier is reported in LC VCOs [2]. But no investigation on using the equal transconductance and approximately equal parasitic capacitance together was reported.

II. Phase noise in $1/f^3$ region

Since MOSFETs are surface devices, they generate flicker noise to a much greater degree than bipolar transistors [4]. In oscillators, flicker noise is upconverted to $1/f^3$ phase noise close to the carrier. In this section, we concentrate on $1/f^3$ phase noise of a VCO.

To understand the phase noise mechanism, an appropriate phase noise model is very important in the design and optimization of LC VCOs. Some models are based on a linear time invariant feedback system [5], [6]. But the VCO system is fundamentally time-varying. Here, we adopt Hajimiri's model [2], which treats the generation of phase noise in an oscillator as a linear, time-varying (LTV) process, to predict phase noise of a VCO.

The LTV model defines the impulse sensitivity function (ISF), a periodic function that describes the sensitivity of an oscillator to phase perturbation due to fluctuations produced by noise in an oscillator system. For a n node system, the ISF of the ith node is defined as [2]:

$$\Gamma_i(\omega t) = \frac{f_i'(\omega t)}{\sum_{j=0}^{n} f_j'(\omega t)} \tag{1}$$

Where $f_i'(\omega t)$ is the first derivative with respect to phase of the voltage waveform on node i. And ISF also can be expanded in a Fourier series :

$$\Gamma_i(\omega t) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 t) \tag{2}$$

Where c_0 and c_n are fourier series coefficients. c_0 is the average value of the ISF, which controls the transformation of $1/f$ and other low frequency noise sources into the oscillator's spectrum. The ISF output waveform is extracted from Spice simulation. Then c_0 can be calculated from the simulated ISF.

Given c_0, the $1/f^3$ single sideband phase noise power spectral density, at an offset frequency of $\Delta\omega$ from the carrier, is described as [2] :

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log\left(\frac{c_0^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{8\Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right) \tag{3}$$

Where q_{max} is the maximum charge displacement across the capacitor on the node i, $\omega_{1/f}$ is the $1/f$ corner frequency, $\overline{i_n^2}/\Delta f$ is the total mean square noise power spectral density.

The main noise contribution in $1/f^3$ region is dominated by the upconverted flicker noise of the tail current source when using a complementary cross-coupled structure with tail current. In practice, a small amount of the PMOS and NMOS switch transistor flicker noise is also upconverted to $1/f^3$ phase noise by phase modulation.

According to [7], $L\{\Delta\omega\}$ can be rewritten as a noise-to-signal ratio :

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log\left(\frac{N_{\mathcal{L}}}{V_0^2/2}\right) \tag{4}$$

Where V_0 is the tank output amplitude, and $N_{\mathcal{L}}$ is the noise power. Since spectreRF expresses the phase noise data in term of $N_{\mathcal{L}}$ and signal power, Eq. (4) is very useful in practice. By using $q_{max} = CV_0$, C is the node i capacitance, and combing Eq. (3) and (4), we get

$$\mathcal{L}\{\Delta\omega\} = \frac{c_0^2 \cdot \overline{i_n^2}/\Delta f}{4C^2\Delta\omega^2} \tag{5}$$

Form Eq. (3) and (5), decreasing the square of the average value of ISF reduces the phase noise power spectral density in the $1/f^3$ region proportionally. Since the height of the positive and negative lobes of the ISF are determined by the slope of rising and falling edges, maintaining the symmetry in the ISF waveform rise and fall time can reduce c_0 and attenuate the transformation of $1/f$ noise into the phase noise spectrum [2]. Moreover, the elimination of low-frequency noise sidebands for waveforms with half-wave symmetry, i.e., $f(t) = -f(t \pm T/2)$ (T is the waveform period), was observed in [8]. And it is further confirmed by [9].

Therefore, the waveform symmetry properties are very important for reducing the flicker noise upconversion. In our LC VCO design, not only the tranceconductance of PMOS and NMOS are set equal, but also the parasitic capacitance of PMOS and NMOS are as equal as possible.

III. CMOS Voltage-Controlled Oscillator Design

The VCO topology for our design is shown in Fig. 1(a). Compared with NMOS transistors only cross-coupled topology, the complementary cross-coupled VCO has two main advantages. First, with the additional PMOS pair, the complementary topology offers higher transconductance to compensate for the loss of the tank with less current consumption. It is more power efficient. Second, matching the PMOS and NMOS transistors, the complementary topology provides better symmetry properties of the oscillating waveform, which decreases the upconversion of $1/f$ noise of devices to the $1/f^3$ noise region.

The basic complementary cross-coupled VCO concept is shown in Fig. 1(b). The PMOS and NMOS transistor pairs in positive feedback provide negative resistance $-R_{pmos}$ and $-R_{nmos}$ respectively, as shown in Fig. 1(a). The negative resistance $-R_{pmos}$ and $-R_{nmos}$ are designed to compensate for the loss associated with the LC tank, which is denoted as R_{eq} in Fig. 1(b). C_{pmos} and C_{nmos} are parasitic capacitance of PMOS and NMOS transistors, respectively. Fig. 1(b) also

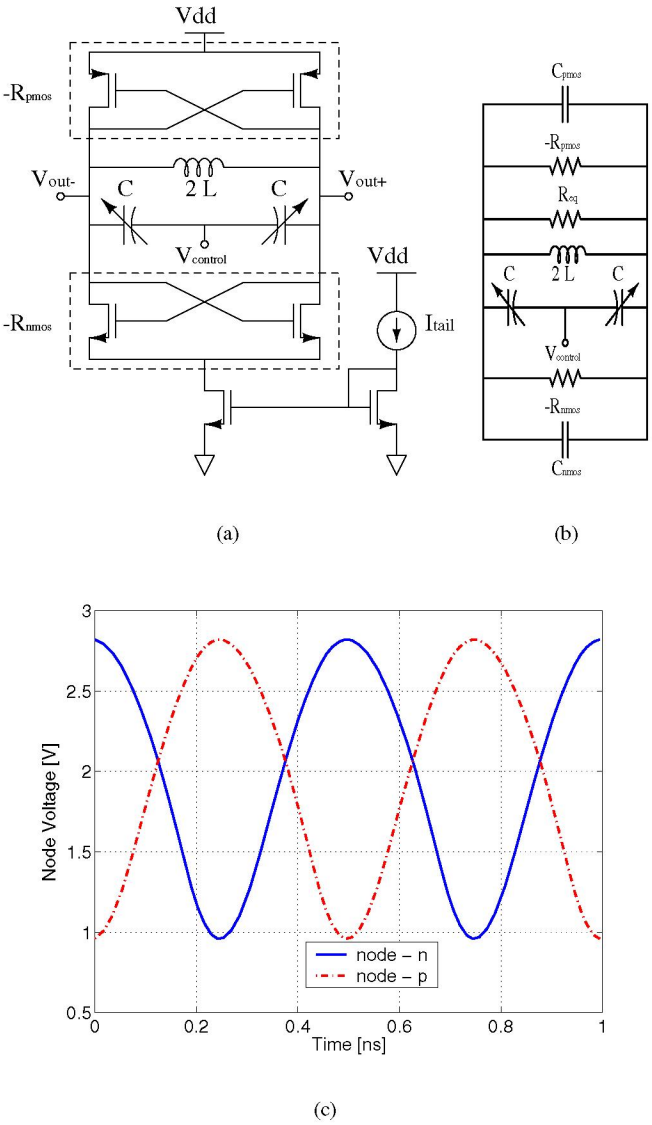


Fig. 1. CMOS LC VCO: (a)Topology, (b) Concept, (c) Output node voltages

shows us that the complementary cross-coupled topology is a more symmetric circuit than one of only PMOS or NMOS transistors in a cross-coupled circuit. Fig. 1(c) shows the simulated node voltage waveform when Vdd is 3 V. The values of L and C are such that the circuit oscillates at 2 GHz. We see that the shape of a rising edge is controlled by the PMOS transistors, which switch the output node voltage to the power voltage. And the shape of the falling edge is controlled by NMOS transistors, which switch the output node voltage to approach the V_{DS} of the tail transistor. We know the rising time of the waveform is affected by C_{pmos}/g_{mp} and the falling time of the voltage waveform is affected by the C_{nmos}/g_{mn}, as seen in Fig. 1(b). So, in order to maintain single-ended symmetry of each half circuit, we design the PMOS and NMOS transistors with the same transconductance ($g_{mp} = g_{mn}$), and the PMOS and NMOS transistors with

approximately equal parasitic capacitance ($C_{pmos} \approx C_{nmos}$).

Equation (1) shows that the ISF function $\Gamma(\omega t)$ is proportional to the first derivative of the VCO output voltage. Further, we see that the more symmetric the output voltage waveform, the better the symmetry in the ISF waveform. With more symmetric ISF waveform, the average value of ISF, i.e., c_0, is minimized, and then less $1/f$ flicker noise is upconverted.

Based on the VCO circuit symmetry properties, two integrated VCO circuits are designed in the 0.18 μm TSMC CMOS process, following Fig. 1(a), for 2 GHz operation. A symmetric octagonal inductor with the quality factor 8.5 at 2 GHz and the inductance of 4.5 nH, as well as two n+ accumulation MOS varactors and the capacitance tuning range from 1.2 pF to 2.6 pF consist of the resonate tank. A simple current mirror is used for setting the bias current in the resonator. According to the traditional symmetry properties, when designing VCO1, we match the PMOS and NMOS transistor transconductances ($g_{mp} = g_{mn}$) with the minimum length for each transistor, respectively, i.e., the PMOS transistor length is 0.3 μm and the NMOS transistor length is 0.35 μm. On the other hand, when designing VCO2, we not only match the transconductances of the PMOS and NMOS transistors, we also design equal areas of PMOS and NMOS to make the parasitic capacitances of the PMOS and the NMOS transistors as equal as possible. The length chosen for the PMOS is 0.30 μm, and the length for the NMOS is 0.5 μm.

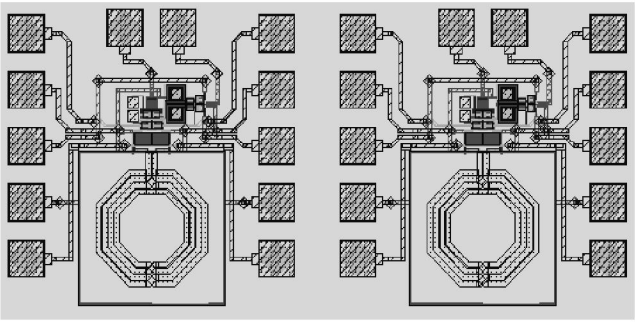
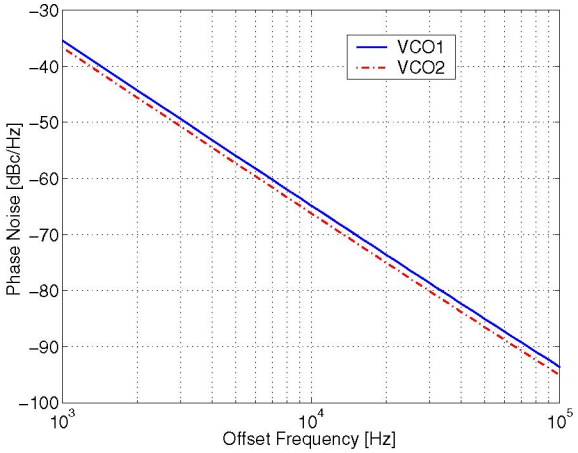


Fig. 2. The layout of VCO1 (left) and VCO2 (right).

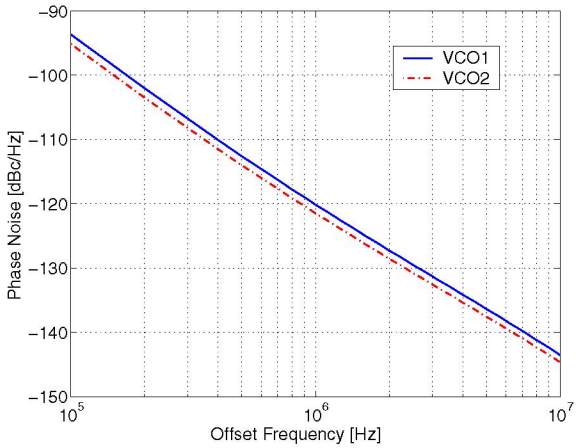
IV. Simulation Results and Layout

The physical layout implementation of VCO1 and VCO2 is shown in Fig. 2. The area is approximately 1.7x0.8 mm^2. The two different VCO structures are simulated through SpectreRF with a 3 V power supply. Verification of phase noise performance improvement of the proposed technique was done on the transistor level.

Figure 3(a) and 3(b) show the phase noise at low offset frequencies and large offset frequencies, respectively, from the carrier frequency 2 GHz. The phase noise of VCO1 is -93.68 dBc/Hz and VCO2 is -95.16 dBc/Hz at 100 kHz. And VCO1 is -131.28 dBc/Hz, VCO2 is -132.53 dBC/Hz at 3 MHz. A significant improvement is observed at close-in phase noise in Fig. 3(a) due to the reduction of the upconverted flicker noise of transistors with the matched transconductance and parasitic capacitance; as the offset from the carrier gets larger, the contribution from the upconverted thermal noise of transistors becomes more pronounced. The phase noise performance of VCO2 is still better than that of VCO1 at larger offsets due to the smaller γ for longer-channel NMOS transistors in VCO2, seen in Fig. 3(b).



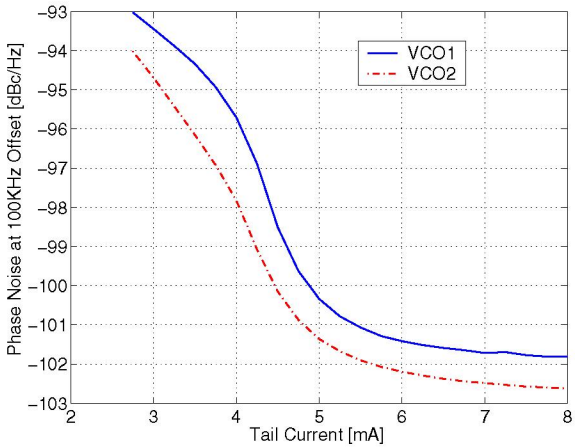
(a)



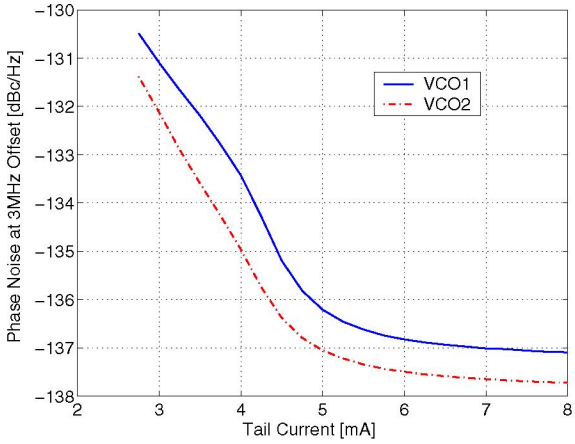
(b)

Fig. 3. (a) Simulated the close-in phase noise of CMOS VCO, (b) Simulated phase noise at larger offsets from carrier

We know the main upconverted flicker noise of a VCO is from the tail current source. To get more insight about the better phase noise of the proposed technique, phase noise of both VCOs is simulated at 100 kHz and 3 MHz offset for different tail current, as shown in Fig. 4(a) and 4(b). As can be seen from these graphs, VCO2 has better phase noise performance than that of VCO1. Also, we can see the improvement is smaller as the offset from carrier gets larger. Moreover, increasing the tail current will improve the phase noise due to the increase in oscillation amplitude. But the larger tail current means more power consumption.



(a)



(b)

Fig. 4. (a) Simulated 100 kHz offset versus Itail, (b) Simulated 3 MHz offset versus Itail, f_0=2 GHz and Vdd=3 V

Figure 5 shows the tuning characteristics of VCO1 and VCO2 tuned from 0.5 V to 2.5 V. From Fig. 5, we can see the frequency of VCO2 is a little lower than that of VCO1 due to the slightly bigger parasitic capacitance caused by a slightly bigger size NMOS transistors used in VCO2. But we also can see the tuning range of VCO1 is almost the same as the tuning range of VCO2. So, the effect of the slightly bigger parasitic capacitance of NMOS transistors in VCO2 on tuning range can be negligible. But, as the area of NMOS transistors gets larger, the parasitic capacitance will severely deteriorate the VCO tuning range.

V. Conclusions

A new approach to the design of an LC-tank VCO with flicker noise upconversion minimization is proposed. The key idea is to get good phase noise performance using a symmetric and balanced circuit, which can be realized with

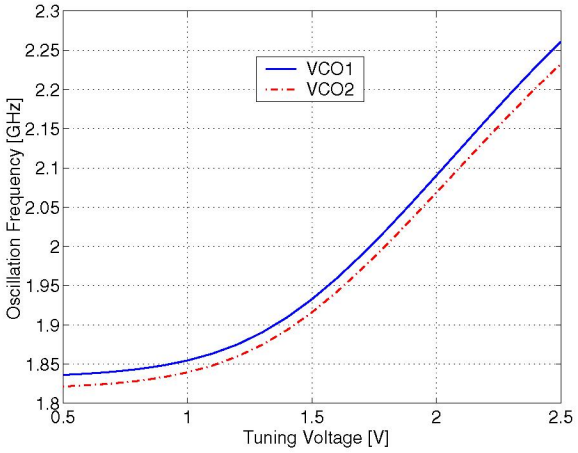


Fig. 5. The simulated tuning range of two VCOs.

equal transconductances and approximately equal parasitic capacitances of the PMOS and NMOS transistors. The impact of parasitic capacitance on phase noise was analyzed and simulated in Fig. 3. It highlights the design trade-offs involved in the symmetric LC VCO architecture. Moreover, the effect of the tail current for the reduction of phase noise has been addressed. Simulated phase noise results within the offset frequency range of 100 kHz to 3 MHz from the carrier are in good agreement.

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