SESSION TA3:

Radio Frequency and Optical Circuits

Chair: Mark Schrader, *Harris Corporation*
Co-chair: Dong Ha, *Virginia Tech*

CMOS PASSIVE RFID TRANSPONDER WITH READ-ONLY MEMORY FOR LOW COST FABRCIATION

W. Jeon*, J. Melngailis, and R. W. Newcomb

Department of Electrical and Computer Engineering
University of Maryland, College Park, MD 20742, USA
Email: wcjeon@glue.umd.edu Phone: 301-405-0030 Fax: 301-314-9437

ABSTRACT

A novel fully integrated CMOS passive RFID transponder without EEPROM and control logic was designed and simulated. 1.5V of the operation voltage was generated by the charge pump and the average power required for operation was 62.9μW at 910MHz. 0.41x0.64mm^2 of die area was required for fabricating the suggested RFID chip.

I. INTRODUCTION

The applications of Radio Frequency Identification (RFID) can be found in the supply chain for inventory control, product tracking, and counterfeit control [1] and aviation for airline passenger and baggage tags. [2] These are a few RFID applications and their applications are expanding rapidly. However, up to now, RFID tags are used for only high price merchandise and applications because of the high manufacturing cost. In other words, reducing the manufacturing cost is the main concern and inexpensive CMOS technology is one of the most promising solutions due to its low-cost, and low-power operation.

Several CMOS passive RFID tags were suggested [3-4], and they used EEPROM using floating gate memory for reading and writing data in RFID transponder tags. EEPROM and its logic circuitry require many transistors and are difficult to be fabricated in the standard CMOS process which increase the manufacturing cost and may be vulnerable to tampering.

Here, we report a design of a simple RFID tag, which does not have EEPROM and logic control circuits and occupies only 0.41 x 0.64 mm^2 of die area. An inverter train, which has a series of 128 inverters, was designed to read 64-bit data sequentially and a modified ring oscillator was designed to generate a short pulse train with long period. The pulse generated in the oscillator travels from the first inverter to the 128th inverter with enough time delay to read one bit of data where traveling through two inverters. An external printed dipole antenna is connected to the input of the charge pump. Even though our design is a read only RFID tag and does not ally reprogramming, the manufacturing cost can be significantly reduced over currently used RFID tags.

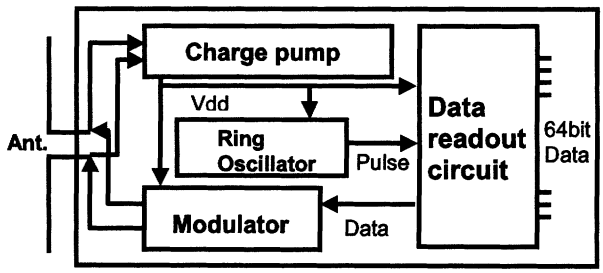

Figure 1: Block diagram of the RFID transponder chip

II. SYSTEM ARCHITECTURE

The RFID chip consists of four parts, a charge pump for generating 1.5V of DC operating voltage, a ring oscillator for clock generation, a data readout circuit with inverter train, and a modulator to modify the input impedance. (Fig. 1)

A. Charge Pump with voltage regulator

For generating a DC supply voltage, the incident RF signal needs to be multiplied after rectification. A charge pump circuit with Schottky diodes was used for multiplying the operating voltage. Two diodes and two capacitors consist of one stage. For the multiple stages, the maximum possible DC bias voltage can be calculated by the following equation.

$$V_{DC} = 2N\left(V_{PP\_RF} - V_{on}\right) \quad (1)$$

Where V_{PP_RF} is the positive peak voltage of the incident RF signal, V_{on} is the turn-on voltage of a

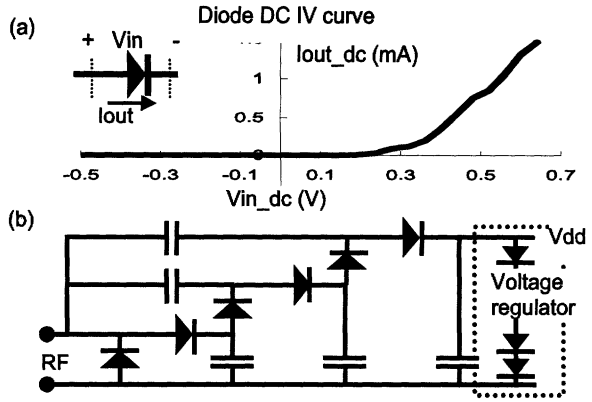

Figure 2: (a) Measured DC current(A) vs. DC voltage input(V) curve of a Schottky diode with 10x10μm^2 contact area (b) Three stage Charge pump with voltage regulating diodes

Schottky diode, and N is the number of stages in the charge pump. [4] Fig. 2(b) shows a three-stage charge pump with voltage regulating diodes. The number of diodes can be decided by the peak-to-peak voltage, $V_{p\text{-}p}$, of the incident RF signal. For the case of the small RF signal input, such as $0.7V_{p\_p}$, the 13-stage charge pump was enough to generate the operating voltage of 1.5V.

The main parameters for designing a charge pump are the series resistance and the junction capacitance of the Schottky diodes and load capacitors. After fabricating and testing several diodes with various contact areas through the AMI 0.5μ process, a Schottky diode with 10x10μm^2 contact area was selected due to its DC IV characteristics, 7.2μA at 0.2V turn-on voltage and 215Ω of the series resistance as shown in Fig. 2(a). From this measured result, seven Schottky diodes were used for limiting the DC output to below 1.5V, which can be calculated by the following equation.

$$V_{dd} = k(V_{on} + R_s I_d) \qquad (2)$$

Where k is the number of regulating diodes, Rs is the series resistance, and I_d is the diode current. If the voltage generated by the charge pump was lower than the limit, 1.5V, the voltage applied to each regulating diode was lower than V_{on}.

B. Ring Oscillator with modified pulse train

To generate a short pulse for stimulating the first inverter in the inverter train, a modified ring oscillator was designed by adding a capacitor, "C" in Fig. 3. A normal ring oscillator generates a pulse train with the pulse width of a half of its period. If a capacitor is added between the first and the

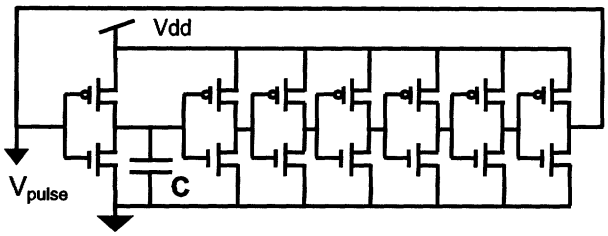

Figure 3: Ring oscillator with pulse width modification

second inverters, the second inverter waits until the capacitor is charged up to the threshold voltage. The gate width and length ratios of all transistors were chosen to set the pulse width to 200ns.

C. Data readout with an Inverter Train circuit

The main idea of the inverter train circuit is modifying the delay between two inverters. The delay time of an inverter was intentionally increased to a half of the pulse width of the oscillator output by changing the width and length ratios of the pFET and nFET of the inverter. Fig. 4 shows the inverter train and switches. D1 through D64 represent the 64bit fixed data, which is already coded during the fabrication. All inputs connected to switching nFET's, which is connected to on-or-off nFET's (M_2, M_4, M_6,..., M_{128}). Focused Ion Beam (FIB) can be used for implanting Ga+ ions to permanently turn some of nFET's off. For fabricating a 200mm wafer with 80,000 chips, 5.6min implantation time, after thinning the glass layer, is required. [5] When a pulse, Vpulse, with 200ns of pulse width comes in, the first switch, M_1, is turned on and the first inverter, In_1, begins to be turned on. In_2 begins to be turned on at 100nsec. After 200ns, In_2 is fully turned on and M_1 is turned off and M_3 is turned on. The third inverter, In_3, begins to operate at 200ns. At 300ns, In_2 and M_3 are turned off and M_5 is turned on. As time goes by, this single pulse travels to the last inverter, In_{128}, and turn on M_{127}. After turning off the last switch

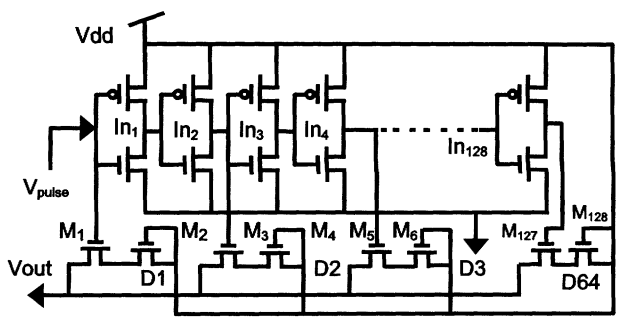

Figure 4: Inverter Train with nFET switches between data and output to the modulator and on-or-off nFET's

M_{127}, the pulse vanishes. Since Vpulse was periodic, a periodic pulse travels through the inverter train and the output data is repeated with the same period as that of the ring oscillator.

C. Modulator

Backscattered modulation was used for designing the modulator. When the periodic data sequence arrives from the readout circuit, the modulator changes the input impedance of the RFID chip. As a result, the reflected RF signal varies with a specific pattern, which is repeated at the same frequency as the ring oscillator. By detecting this pattern, the RFID data receiver can recognize the target.

Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), and Phase Shift Keying (PSK) are dominant digital modulation methods for RFID applications. ASK is common in 13.35MHz load modulation. PSK is the most common in 915MHz backscattered modulation due to the better power efficiency. [4] Since ASK could give a loading effect on the operation of the charge pump and the variation of the capacitance of the charge pump was negligible in PSK mode, PSK was considered to be implemented. Fig. 5 shows the modulator circuits for both ASK and PSK cases, where the data pulse train changes the capacitance of the input impedance.

III. Simulations

0.5μ CMOS process transistor models were used for the Spice simulation. The Schottky diodes with 0.2V as the turn-on voltage, 215Ω for the series resistance, 16fF as the junction capacitance, and 2pF capacitor loads were used in the charge pump circuit. Table 1 shows the design specification for the RFID transponder chip. An RF signal at 915MHz, which is within the standard operating frequency range in Auto-ID class 0 &1 and ISO 18000-6 A & B [3], and 0.7V V_{p-p} was the

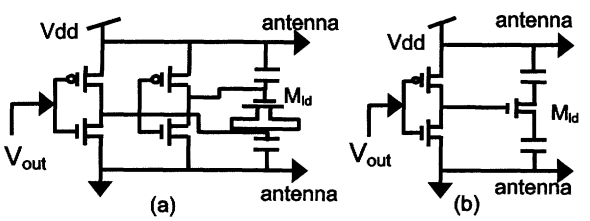

Figure 5: (a) PSK circuit and (b) ASK circuit, output impedance varies by the data train (V_{out}).

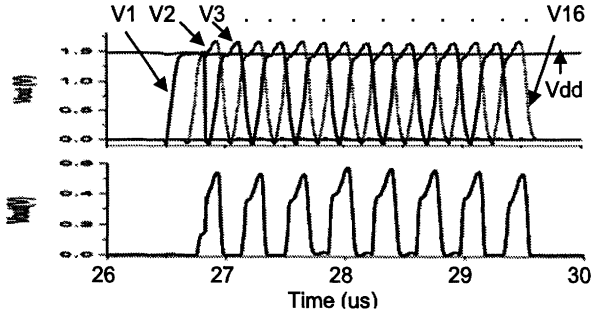

Figure 6: (a) 1.5V Vdd and 16 outputs (V) of the inverter train: Outputs of In1 to In16 in Fig. 4. The first pulse turns the second inverter on and the second pulse turns the third inverter on, and so on. A pulse travels through the inverters in the readout circuit. Each pulse turns one switch on to transfer the input data to the output (b) Scanned output voltage: Vout of Fig. 4. The input data was "0101010101010101"

incident RF signal. The ring oscillator consists of high W/L ratio (20/1) nFET's for generating a short pulse with 200ns pulse width. The inverters in the readout circuit consist of low W/L ratio (3/10) nFET's for 100ns delayed switching and the switches are all nFET's with fast switching. Fig. 6 shows the simulation result of the 16bit inverter train with switch circuit. 16 outputs of 16 inverters are shown in Fig. 6(a). The output of switches (Fig. 6(b)) showed the same sequence as the input data. For the PSK modulation circuit, the nFET capacitor had a large gate area for a wide variation of the input impedance.

The power was mainly consumed in the charge pump and the oscillator circuit, since only up to two inverters and one nFET were in the operation of the readout circuit. For $0.7V_{p-p}$ and 910MHz of incident RF signal, the average powers consumed were 0.2uW, 2.5μW, and 60.2μW for the readout, the oscillator, and the charge pump, respectively.

The average power consumption was 62.9μW. If 0dBm transponder antenna gain and free space propagation loss are assumed, the operating distance can be calculated by the following Friis free space transmission equation. [6]

$$d \le \sqrt{\frac{P_{Tx} G_{Tx} \lambda^2 G_{Rx}}{16\pi^2 P_{Rx} L}} \qquad (3)$$

Where d is the distance between transmitter and transponder, P_{Tx} is the transmitted power, P_{Rx} is the received power, G_{Tx} is the transmitter gain, G_{Rx} is the receiver gain which is the antenna gain, λ is the wave length of the incident RF signal, and L is the system loss factor. If an RF signal with the frequency of 915MHz and 4W of Effective Isotropic

Radiated Power (EIRP) was transmitted, the working distance was calculated to be 6.39m.

Fig. 7 shows the simulation result of the inverter train for 64bit input data with a ring oscillator circuit. The 0.5V pulse train represents the output signal transferred from the input through the readout circuit. The 1.5V pulse train with 200ns of the pulse width and 15μs of the period was generated by the oscillator circuit. One bit data can be read in 200ns and the data rate is 10Mb/s. As long as the operation voltage of 1.5V is maintained, there was no effect on the pulse width and the data rate. When we changed the frequency of incident RF signal, the pulse width varied due to the operation voltage change. However, in the frequency range between 800MHz and 2.5GHz, negligible Vdd change was observed.

The modulator changed the capacitance of the load transistor M_{ld} in Fig. 5 by changing the voltage between gate and source. The threshold voltage of the inverter needed to be low to 0.4V due to the low output voltage from the readout circuit.

Table 1: Design specification for RFID chip

Part	W/L		Capacitance
	pFET	nFET	
Charge pump	N/A		2pF
Ring Oscillator	3μ/4μ	10μ/1μ	20pF
Readout Inverters	1μ/2μ	3μ/10μ	N/A
Switches	N/A	2μ/1μ, 10μ/3μ	N/A
Modulator	1μ/10μ	20μ/1μ, 30μ/10μ	5pF

IV. Layout

The charge pump circuit in 0.119mm^2 area, the readout circuit in 0.076mm^2 area, the ring oscillator circuit in 0.041mm^2 area, the modulator circuit in 0.023mm^2 area, and the pads in 0.02 mm^2 area were used. Total 0.261mm^2 (0.408mm x 0.639mm) of die space was required for fabricating the designed RFID chip.

V. Conclusions

An RFID transponder chip with read-only memory was designed and simulated. By omitting EEPROM and logic circuitry, the chip size is minimized and the suggested RFID chip can be fully fabricated through the inexpensive CMOS process. As a result, significant cost reduction is expected. The data transfer rate was 10Mb/s, which is much faster than other RFID circuits. The

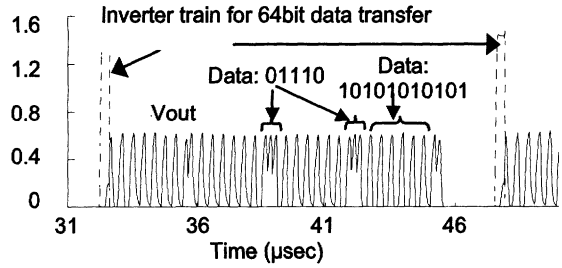

Figure 7: Simulation result of inverter train for 64Bit data. Solid line is the output (Vout in Fig. 4) and dashed line is a pulse train (Vpulse in Fig. 3 and 4) generated by the ring oscillator.

power required for operation was 62.9μW and the working distance between transmitter and transponder was calculated to be 6.58m. For numbering codes, FIB implantation of transistor gates can be used to permanently turn some of on-or-off transistors off. Actual RFID chip is being fabricated through a 0.5μ CMOS process and will be tested in an anechoic chamber with RF radiation.

REFERENCES

[1] N. Raza, V. Bradshaw, M. Hague, " Applications of RFID technology," Proc. of the IEE Coll. on RFID Tech., London, pp. 1/1 - 1/5, October, 1999

[2] A. Cerino and W. P. Walsh, "Research and application of radio frequency identification (RFID) technology to enhance aviation security." Proc. of IEEE Natl Aero & Elec Conf., Dayton OH, USA, pp. 127 – 135, October, 2000

[3] R. Glidden, C. Bockorick, S. Cooper, C. Diorio, D. Dressler, V. Gutnik, C. Hagen, D. Hara, T. Hass, T. Humes, J. Hyde, R. Oliver, O.Onen, A. Pesavento, K. Sundstrom, and M. Thomas, " Design of ultra-low-cost UHF RFID tags for supply chain applications," IEEE Comm. Mag., Vol. 42, Iss. 8, pp.140 – 151, August, 2004

[4] U. Karthaus and M. Fisher, "Fully integrated passive UHF RFID transponder IC with 16.7-μW Minimum RF input power," IEEE Trans. Solid State Circuits, vol. 38, no. 10, pp. 1602-1608, October, 2003

[5] A. DeMarco, W. Bandy, S. Parsa, H. Kaufmann, and J. Melngailis, "Writing the identity in RFID tags with focused ion beam implantation of transistor gates," J. of Vac. Sci. Tech. B Nov/Dec, 2005

[6] H.T. Friss, " A note on a simple transmission formula," Proc. of the IRE, Vol. 41, pp. 254-256, May, 1946