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Digital Integrated Circuits Analysis and Design

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This is a well-written solid engineering oriented book covering the transistor circuits associated with digital electronic systems. From the Preface the background knowledge assumed is of “calculus, differential equations, physics, and chemistry as well as courses in circuits, electronics, and digital logic” with the book intended to “fit into the junior or senior year.” The stated goals of the book are:

1. To present an interdisciplinary approach that will remain relevant for years to come
2. To provide broad coverage of the field that is relevant for engineers designing integrated circuits or designing with integrated circuits
3. To focus on the underlying principles rather than on details of current technology that will soon be obsolete.”

Chapter 1 “Introduction to Digital Integrated Circuits,” pages 1-43, is, as stated, a short overview; the emphasis is upon logic gates and includes a good summary of transistor IC fabrication steps (for which I would have liked to see substrate contacts for CMOS and EBC labels for NPN).

Chapter 2 “Semiconductor Materials,” pages 45-60, Chapter 3: “Diodes,” pages 61 – 87, and Chapter 4 “Bipolar Junction Transistors,” pages 89-114, lead into Chapter 5, “Transistor-Transistor Logic,” pages 115-206, and Chapter 6, “Emitter-Coupled Logic,” pages 207-254. These cover material as found in most basic electronics books with, however a very good set of Laboratory Exercises and (homework) Problems, especially for the TTL material.

The book then turns to FET device characterizations in Chapter 7, “Field-Effect Transistors,” pages 155-286, which are then used in the next five chapters (Chapter 8, “NMOS Logic,” pp. 287-319; Chapter 9, “CMOS Logic,” pp. 321-389; Chapter 10, “Low-Power CMOS Logic,” pp. 391-421; Chapter 11, “BiCMOS Logic;” pp. 423-447; Chapter 12, “GaAs Direct-Coupled FET Logic,” pp. 449-480).

Six more chapters and two appendices close out the book: Chapter 13, “Interfacing between Digital Logic Circuits,” pp. 481-508. Chapter 14, “Interconnect,” pp. 509-541; Chapter 15, “Bistable Circuits,” pp. 543-576; Chapter 16, “Digital Memories,” pp. 577-606; Chapter 17, “Design and Layout,” pp. 607-634; Chapter 18, “Integrated Circuit Packages,” pp. 635-661. The appendices give some Si and GaAs constants and a large number of symbols used (over four pages worth). The index I also find to be quite complete (covering 26 pages).

As can be inferred from the chapter titles the material is essentially what is being taught from the digital portion of Sedra and Smith, “Microelectronic Circuits,” [1], what I would call classical IC circuits. For this reason, and as the book has the essential basic material, it is not clear that electronics should be a prerequisite to using this book. Indeed one of the advantages of this book is that it has the basic background material needed for understanding the transistorized digital circuits covered. Another significant advantage is that each chapter has an excellent one-half to two (in the case of TTL) page “Quick Reference” set of tables at the end of each chapter. There is also a good use of figures and of tables within the chapters, such as Table 7.1 “MOSFET Symbols” (for which I would have liked to see the arrows placed on the three terminal MOSFETs, as well as the reason for their direction, since there is considerable trouble for students to understand why they are not in the “same” direction as those on the four terminal representations). The inclusion of Spice techniques used throughout is also a definite plus (though it would have been best to use Spice parameters in the device equations, for example KP to escape confusion with the KP of p. 269).

Concerning the stated goals listed above, for goal one the chapter headings more or less tell the story. Note though that it is weak on things of importance for the future of digital circuits, missing for example organic, DNA, quantum, and single electron transistor circuits, among others. For goal two, it is reasonably met but some items of importance are missing, among these I would mention multivibrators, digital filtering, digital PLLs, High Definition Languages, fabrication means for resistors and capacitors (in Chapter 1) and more than one line on FPGAs (p. 621). Since a means of getting PSpice from the web is given, it would be most useful to also give a web

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O

Optical resolving power; cf. Image resolution
Optimization; cf. Circuit optimization

P

Packet switching
 gigascale SoC, xpipes, net.-on-chip archit. Bertozzi, D., + , CAS-M
Second Qtr 2004 18-31

Parallel architectures
 gigascale SoC, xpipes, net.-on-chip archit. Bertozzi, D., + , CAS-M
Second Qtr 2004 18-31

Parallel processing; cf. Parallel architectures

Pipeline processing
 gigascale SoC, xpipes, net.-on-chip archit. Bertozzi, D., + , CAS-M
Second Qtr 2004 18-31

Power demand
 charge pump ccts., power consumption optim., summary. Palumbo,
 G., + , CAS-M *Third Qtr 2004* 26-29

PROM; cf. EPROM

S

Signal processing
 genomics and proteomics, a signal processor's tour. Vaidyanathan,
 P.P., CAS-M *Fourth Qtr 2004* 6-29.
Signal resolution; cf. Image resolution

T

Telecommunication; cf. Data communication
Time division multiplexing; cf. Packet switching

Transducers; cf. Biomedical transducers

Transform coding
 video coding, H.264/AVC, tools, perform., complexity. Ostermann,
 J., + , CAS-M *First Qtr 2004* 7-28

V

Video coding
 H.264/AVC, tools, perform., complexity. Ostermann, J., + , CAS-M
First Qtr 2004 7-28

reduced spatial resolu. transcoding, summary, drift compensation.
 Yin, P., + , CAS-M *Second Qtr 2004* 32-36

Video signal processing; cf. Video coding

+ Check author entry for co-authors

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page where one can find the layout for standard digital cells, to go with Chapter 17. And, in spite of the third goal, which is reasonably met, since any student in the US can fabricate an IC chip through MOSIS, with students in Europe and Asia having similar alternatives, it would be appropriate to have oriented Chapter 17 toward this possibility. A weakness which I find in similar texts is the omission of the substrate terminal and its connection for CMOS transistors, especially those where the substrate potential is critical (such as the mid-potential transistor Mno of the dynamic CMOS inverter, p. 357).

As mentioned above, this book could serve as an alternative to the digital portion of Sedra and Smith [1], though the latter has a lot more circuits with more emphasis upon analog concepts. Ayers' book could serve as an excellent background for more advanced works such as that of Baker, et al [2], which concentrates almost exclusively on CMOS circuits, Rabaey, et al [3], which

concentrates more on layout and again is primarily CMOS oriented, Geiger, et al [4], which gives a much broader in depth coverage including analog as well as digital circuits, and Gray & Meyer [5] which emphasizes almost exclusively analog topics.

In summary, this is an excellent book for a first course which concentrates on digital electronics at the transistor level. Any shortcomings can easily be handled by supplementary material supplied by an instructor.

References

- [1] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Fifth Edition, Oxford University Press, New York, NY, 2004.
- [2] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. IEEE Press, New York, NY, 1998.
- [3] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits, A Design Perspective*, Second Edition, Prentice-Hall, Upper Saddle River, NJ, 2003.
- [4] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*. McGraw-Hill Publishing Co., New York, NY, 1990.
- [5] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Third Edition. John Wiley & Sons, Inc., New York, NY, 1993.

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