System Architecture for Multi-Technology Testbench-on-a-Chip

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Abstract

The Architecture for a multi-technology testbench on a chip is presented for functional testing of mixed signal devices. The technologies tested by this System-on-a-Chip (SoC) include Op Amps, biosensors, and smart signal processing of Analog/Digital Multiplexers. This paper focuses on describing the architecture of the testbench on a chip as well as the results obtained from testing integral components of the fabricated device. The objective of this research is to uncover key metrology infrastructure issues needed for developing the design reuse approach for multi-technology System-on-a-Chip (SoC) devices.

1. Introduction

The driving force in today's semiconductor industry is the need to maintain a rate of improvement in speed and size reduction of 2x every eighteen months in high-performance components. Currently, these improvements rely exclusively on advances made in semiconductor miniaturization technology. The 1999 ITRS (International Technology Roadmap for Semiconductors) suggests that, "innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement" [1]. Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple silicon technologies on the same chip. The devices that result from these integrations are commonly referred to as System-on-a-Chip (SoC) devices.

Design is paramount for all categories of the ITRS roadmap. This is especially true for the SoC category where time-to-market for an Application Specific Integrated Circuit (ASIC) is a key attribute for new product delivery. Design is additionally important for SoC devices because of increasing system complexity. The growth of system complexity is due to the diversity of SoC design styles, integrated passive components, and the increased need to incorporate embedded software. Design for SoC devices will become increasingly difficult with the growing interaction among design levels, the difficulties of converging multiple designs onto a single chip, design process predictability, and the growing size and dispersion of design teams.

These challenges are overcome with the use of block-based design approaches that emphasize design reuse. System blocks often contain a layout file that is used for the fabrication process and an Analog Hardware Description Language (AHDL) behavioral model used to describe the interaction of system components during the design process. Each system block should have features that allow for the implementation of Built-in Self-Test (BIST). The emergence of the SoC paradigm imposes various metrology and standardization challenges. These include metrology for multi-technology process monitoring, BIST calibrations, validation of behavioral model representations, and benchmarking simulation of on-chip systems interactions.

Another significant challenge involves ensuring the testability of an IC design. This is a formidable task, as testability within the context of mixed technology integrated circuits is not well defined. Testability is defined as controllability and observability of significant waveforms within a circuit [4]. For most IC designers, significant waveforms are input/output signals that can be obtained at every stage of the circuit. The first stage of the circuit input is assumed to be controllable; while during the last stage, output is observable.

Some have proposed methods of assuring testability that involve the use of oscillatory BIST techniques [5,6]. The BIST method using an oscillation-based test circuit has been shown to have the potential of overcoming common problems associated with conventional test methods [6]. This BIST method has also been shown to be effective for any type of mixed analog/digital circuitry used as system blocks [7].

2. Multi-Sensor System Architecture

The architecture of the Multi-Sensor Smart System is given in Fig. 1 where there are multiple inputs, sensors, and outputs. A built-in self-test (BIST) element is included between each signal processing element. In this system there may be many classes of input signals (for example, material [as a fluid] and user [as indicator of what

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to measure]). Each inputs may be directed to many sensors (for example, one material may go to several sensors each of which senses a different property [as dielectric constant in one and resistivity in another]).

The sensor signals are treated as an N-vector and combined as necessary to obtain the desired outputs, of which there may be many (such as an alarm for danger and indicators for different properties). For example, a patient with kidney disease may desire a system on a chip that gives an indication of when to report to the hospital. In this case, an indication of deviation of dielectric constant from normal and spectral properties of peritoneal fluid may be sensed. Once combined they indicate the presence of creatinine (a protein produced by the muscles and released in the blood) in the fluid. Here, the signal output is recognized as the percent of creatinine in the fluid and an alarm when at a dangerous level.

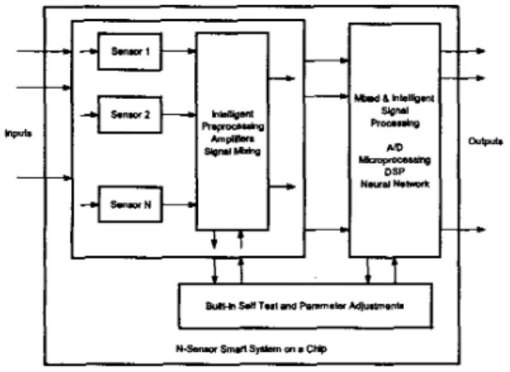

Figure 1. Architecture for Multi-Sensor Smart System on a Chip.

To design multi-technology SoCs such as in Fig.1, a block-based design approaches that emphasize design reuse is preferred to reduce overall design time and cost of testing the new device. System blocks often contain a layout file that is used for the fabrication process and an Analog Hardware Description Language (AHDL) behavioral model used to describe the interaction of system components during the design. To validate the interaction between various sensor, signal processing, and BIST sub-blocks a unique Testbench-on-a-Chip methodology has been developed.

3. TESTBENCH-ON-A-CHIP METHODOLOGY

The Testbench-on-a-Chip evaluates the interactions between key sub-blocks of the multi-sensor smart system. Figure 2 shows the block diagram of the Testbench-on-a-Chip. The most important aspect of the Testbench-on-a-Chip methodology is to be able to multiplex input signals from different sensor system blocks or reference signals to different BIST system blocks. The outputs of the BIST system blocks are then multiplexed to the digital output of the ToC. This enables the use of a computer controlled test system to select and analyze the interaction between different system blocks for a wide range of computer controlled test vectors.

The following sections describe the electronic circuitry used for the Testbench-on-a-Chip in more detail. Included in this circuitry description are biosensors, ring oscillators, test op amps, and smart signal processing in the form of a MUX/DeMUX pair. The test system and computer controlled instrument interface will be described in the final paper.

4. BIOSENSOR SYSTEM BLOCKS

The class of biosensors studied in this work is designed to analyze physical properties of fluids [8]. These sensors are capable of deciphering various characteristics associated with fluids including: color, odor, pH, resistivity, and dielectric constant. The sensors can also discern inorganic and organic chemical properties. Such sensors are implemented using micro-electro-mechanical systems (MEMS) technology. The sensor circuit can be fabricated on a semiconductor substrate that allows for the integration of additional signal processing circuitry onto the chip. An array of such sensors can be used to determine multiple properties of a fluid, using a single chip.

Figure 3 is a schematic of the type of sensor used to detect fluid properties. This example sensor circuit operates as a dielectric constant measurement device. This sensor can be provided as part of an integrated micro-system designed to determine the properties of a fluid. The fluid-sensing transistor in this sensor is a VLSI adaptation of the CHEMFET [9]. The sensor operates as a capacitive-type bridge such that a balance can be set for a normal dielectric constant. In the presence of a fluid, the unbalance that occurs within this sensor bridge is used to evaluate the fluid's dielectric constant.

The four CMOS transistors form the bridge: M1, M6, M7, and the fluid-sensing transistor comprised of transistors M2 through M5. The fluid-sensing transistor and transistor M1 are PMOS (p-type MOSFETs) transistors in the diode connected configuration (gate connected to drain) while the lower two, M6 and M7, are NMOS type (one diode connected and the other with a gate voltage control). The output, Vout, of the sensor circuit is taken between the junction of the fluid-sensing transistor and the diode-connected transistor, M7.

The transistors, M2 through M5, have openings in their gates to allow fluid to flow between the silicon substrate and the polysilicon gate where the gate oxide has been removed. This allows the fluid to

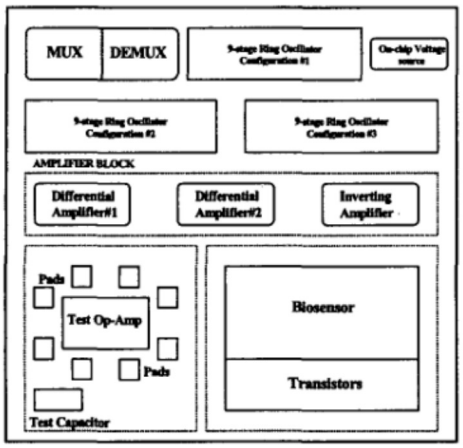

Figure 2. Block Diagram of Testbench-on-a-chip.

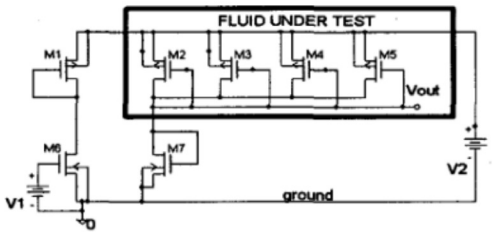

Figure 3. Schematic of biosensor circuit under test. Each transistor has a W/L ratio of 10μ/10μ. The overall W/L ratio of the fluid-sensing transistor is therefore 40μ/40μ.

behave as the gate dielectric for that transistor. The fluid-sensing transistor is constructed out of four transistors with all terminals connected in parallel to increase the gain constant parameter KP that is proportional to the dielectric constant.

Fabrication of the sensor is based on a sacrificial etch process, where the silicon dioxide gate dielectric in the fluid-sensing transistor is removed by chemical etch [10]. This activity is accomplished by opening holes in protective layers using the over-glass cut method available in the MOSIS-MEMS fabrication process.

5. Ring Oscillators and Level Crossing Detectors

Converting the output of the analog CUT into a digital signal involves transferring the signal through an ADC comprised of a Voltage Controlled Oscillator (VCO), Level Crossing Detector (LCD), and Frequency Counter (FC). The LCD and FC make up the frequency-to-number converter (FNC) that passes a number to a frequency counter for processing. A block diagram of this ADC conversion process is shown in figure 4. The frequency counter output, that appears at the output of this diagram can be expressed as a function of the CUT's components or parameters [7]. Changes in various component characteristics (i.e., transistor W/L ratios) will give rise to deviations in the CUT's expected output. The test for a fault is therefore denoted by any deviation of an oscillation frequency from its expected nominal value.

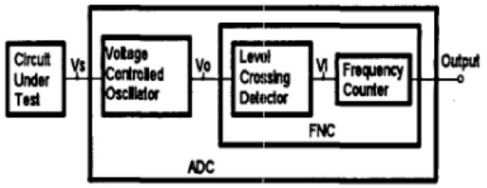

Figure 4. Block Diagram of ADC Conversion.

The question then arises as to how to transform the CUT signal to an oscillating signal. For the case of a steady-state voltage output, oscillations are created with the aide of a voltage-controlled ring oscillator. An example of a VCO is provided in figure 5.

The VCO is a structure made up of three unique parts including: the control input stage, the propagation delay controlled ring oscillator, and the output buffer. The input control voltage (Vin) that originates from the circuit under test controls the overall oscillation frequency of the VCO. This voltage is capable of "current starving" the inverter stages of the ring oscillator and thus changing the propagation delay. The input sets the current in the current sources M5 and M20 of figure 5, which in turn set the current in the delay control elements. The ON resistance of the pull-up (upper transistors of ring oscillator) and pull-down (lower transistors of ring oscillator) transistors is modulated according to the input voltage, Vin. These variable resistances control the current available to charge and discharge the load capacitance of each inverter stage in the ring oscillator. When the control voltage is large, a large current will flow, producing a small resistance and thus a small propagation delay.

Each of the inverters appearing in the VCO ring oscillator consists of two complimentary transistors (an NMOS and a PMOS). A ring oscillator consists of an odd number of inverters. The output of the last inverter is connected to the input of the first. The minimum number of

inverters needed to produce oscillations is three. The oscillation frequency (f_{osc}) is inversely proportional to the gate propagated delay time and the number of gates n, $f_{osc} = 1/(2\pi\tau_{osc})$.

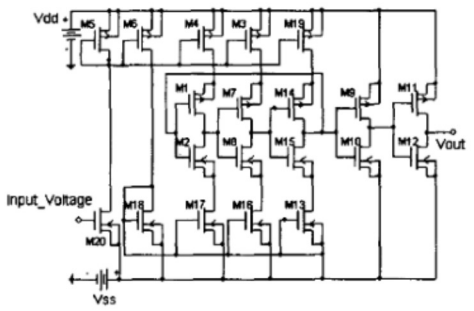

Figure 5. Voltage Controlled Oscillator.

In this analysis, various VCO configurations were considered. The key variables in the design study were those that affected the ring oscillator stage. A number of inverters and drain voltages were considered prior to selecting the configuration for the BIST method studied here. The 9-inverter ring oscillator with a drain (source) voltage of 0.25V (-0.25V) was chosen as most suitable for the BIST ADC.

6. Test Operational Amplifiers

The ring oscillator configurations require the use of unique amplification at several stages. The overall layout of the Op-Amp is 178um x 287um. The op-amp is used along with several resistors to design the necessary amplifier stages for the ring oscillator configurations. The amplifier block in the layout consists of two differential amplifiers and one inverting amplifier designed with this op-amp. Since the op-amp has been used at several stages of the design, a standalone op-amp along with the compensation capacitance was placed in the layout in order to characterize this important core block of the chip. The evaluation of this test Op-Amp will appear in the final publication.

7. Smart Signal Processing

The objective of the MUX-DEMUX pair is to manage the inputs to the Testbench-on-a-Chip. The outputs of the MUX-DEMUX pair are connected to ring oscillator 1, ring oscillator 2, ring oscillator 3 and an external pad. The external pad connection is used to analyze on-chip losses.

8. Device Fabrication

The Testbench-on-a-Chip was fabricated using the MOSIS foundation's AMI 1.6 technology. Due to the incorporation of biosensor circuitry the chip underwent post-processing via an HF etch. Various tests have been conducted on the biosensors and signal processing aspects of the chip. The biosensors were etched in increments of 1,3,and 15 minutes to ascertain the point at which chip bio-transistor collapse would occur. The HF etch process has not affected circuitry components not directly tied into the biosensor circuit. The biosensor circuit was evaluated in the presence of air and liquid. Results of testing the biosensors and associated BIST system blocks for various test vectors will be given in the final paper.

9. Conclusion

A novel Test-bench-on-a-Chip methodology has been introduced to analyze the interaction of various biosensors and BIST circuits. The ToC serves a precursor to the development of an integrated multi-biosensor system using block-based design. The overall system is designed to perform functional testing of mixed signal devices. The technologies tested by this System-on-a-Chip (SoC) include Op Amps, biosensors, and smart signal processing of Analog/Digital Multiplexers. This paper describes the architecture of the Testbench-on-a-Chip.

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