Semistate Theory and Analog VLSI Design

by Angela M. Hodge and Robert W. Newcomb

***Abstract*—Semistate theory as applied to electronic circuits is reviewed in a tutorial fashion. The resulting theory is applied to the design of linear vlsi circuits using an admittance framework for which the main components are CMOS capacitors, differential pairs and current mirrors. The results are extended to nonlinear designs through the use of CMOS multipliers.**

1531-636X/$10.00©2002IEEE

Introduction

Over the recent years, since the 1960's, state variable theory has had a prominent place in the theory of systems [1]. However some artifacts are needed to handle systems with differentiators or even purely algebraic ones, such as resistive circuits. Thus, by the late 1970's the mathematicians had extended the concept [2] as summarized in the books by [3] though one can find similar ideas in much earlier works, for example in the canonical forms of matrix differential equations as treated by Gantmacher [4, p. 45]. These systems actually now go under a number of different names, for example in the mathematical literature as differential-algebraic equations [5–6]. Because of the generality the ideas were quickly taken over to various fields using other names, such as singular systems in control [7, 8], descriptor systems in economics [9], and semi-state systems in circuit theory [10]. Here we illustrate that this theory has some value for the theory of analog VLSI circuit design.

In essence the theory modifies the state variable equations, by placing a possibly singular matrix in front of the derivative of the state, in which the state now becomes something different, which Dziurla [11] suggested be called the semi-state. A useful canonical form for these equations, which we will here call semistate equations, is [12, p. 238]

$$\mathrm{E}\frac{dx}{dt} = \mathcal{A}(x, t) + Bu \qquad (1a)$$

$$y = Cx \qquad (1b)$$

in which $x = x(t)$ = semistate [a k-vector], $u = u(t)$ = input [an m-vector], $y = y(t)$ = output [an n-vector], and B, C, and E are constant matrices. For linear time-invariant circuits the nonlinear time varying operator satisfies

$$\mathcal{A}(x, t) = Ax \qquad (1c)$$

with A also a constant matrix. In this linear time-invariant case the transfer function matrix, $T(s)$ for $y = T(s)u$ with $s = d/dt$, is given by

$$T(s) = C(sE - A)^{-1}B \qquad (1d)$$

It is convenient to call $[A, B, C, E]$ a semistate realization of $T(s)$. It is clear that the realization is not unique since we may premultiply (1a) by a nonsingular matrix P and replace x by $x = Q\underline{x}$ with Q nonsingular so that the same transfer function results. Also of importance to our method will be the fact that both the input u and the output y can be scaled by the same nonzero (scalar) factor g. Thus the same transfer function results from

$$PE\frac{dQ\underline{x}}{dt} = PAQ\underline{x} + QBgu \qquad (2a)$$

$$y = gCQ\underline{x} \qquad (2b)$$

Example 1:

As a simple example, the system which gives the second derivative can be described by

$$\begin{bmatrix}0 & 1 & 0\\ 0 & 0 & 1\\ 0 & 0 & 0\end{bmatrix}\frac{d}{dt}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix} = \begin{bmatrix}-1 & 0 & 0\\ 0 & -1 & 0\\ 0 & 0 & -1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix} + \begin{bmatrix}0\\ 0\\ 1\end{bmatrix}u \qquad (3a)$$

$$y = \begin{bmatrix}1 & 0 & 0\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix} \qquad (3b)$$

These equations give the transfer function via the following calculation.

Angela Hodge and Robert Newcomb are with Microsystems Laboratory, ECE Department, University of Maryland, College Park, MD 20742 USA. Emails: amhodge@eng.umd.edu, newcomb@eng.umd.edu

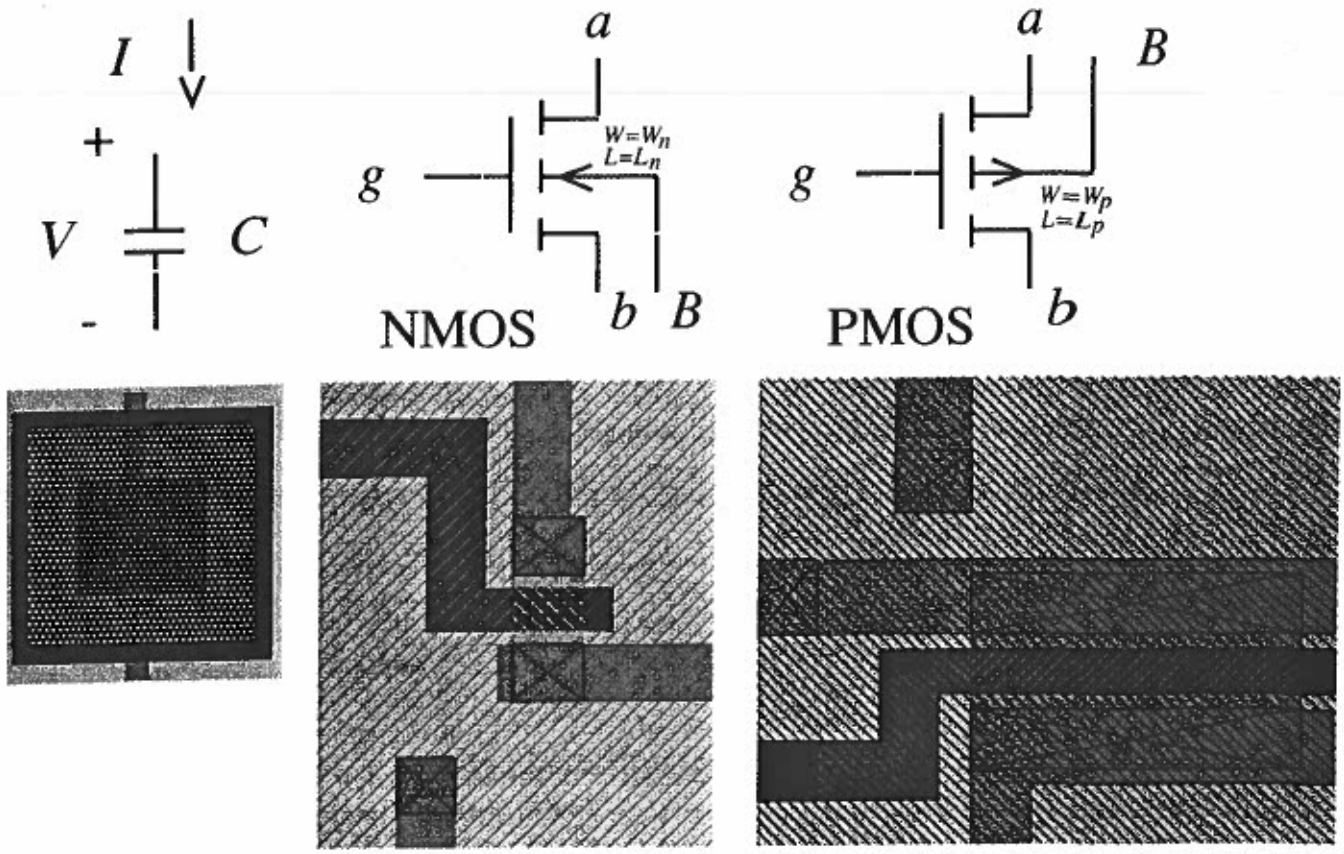


Figure 1. Basic analog VLSI devices and their corresponding VLSI layouts.

$$T(s) = \begin{bmatrix}1 & 0 & 0\end{bmatrix}\begin{bmatrix}1 & s & 0\\ 0 & 1 & s\\ 0 & 0 & 1\end{bmatrix}^{-1}\begin{bmatrix}0\\0\\1\end{bmatrix} = \begin{bmatrix}1 & 0 & 0\end{bmatrix}\begin{bmatrix}1 & -s & s^2\\ 0 & 1 & -s\\ 0 & 0 & 1\end{bmatrix}\begin{bmatrix}0\\0\\1\end{bmatrix}$$

$$= s^2 \qquad (3c)$$

In the case of interest here, that is of VLSI circuits, the vectors u, x,and y are currents and/or voltages. However, since transistors are generally nonlinear components key to vlsi, (1c) will hold only when linearization occurs. As we will see in the section *Circuit Semistate Equations*, one possible choice for x is as the tree branch voltages along with the link branch currents though in designs we will primarily use node to ground voltages.

In the next section we discuss the types of components of interest for vlsi design and show how they fit in the scheme of things. In the section *Circuit Semistate Equations*, we show how the semistate equations result from analysis while following that we will use them for design of linear circuits through the use of an admittance matrix.

VLSI Components

In the present VLSI technologies the primary circuit components of interest are shown in Fig. 1, these being capacitors and MOS transistors both of which are most conveniently described as voltage controlled current devices.

We will assume linear capacitors described by

$$i = c\frac{dv}{dt} \qquad (4)$$

though nonlinear ones can be handled as linear ones seen through a nonlinear resistive circuit [13].

Concerning the MOS transistors, for our purposes we will assume a

slight modification (to include the Early effect) of the Schichman-Hodges [14] description of their DC characteristics. For the transistors shown in Fig. 1 we will take positive currents entering a node, voltages measured with respect to ground and assume that the Bulk, B, does not affect the operation by being properly biased. For the characterization we use the notation: $1(x)$ is the unit step function in x; $KP(=\mu C_{ox})$, V_{th}, and λ are Spice parameters [respectively the conductive gain, threshold voltage and Early effect]; W and L are transistor width and lengths, these latter two being the main design parameters. Generally we will assume enhancement mode devices for which the threshold voltage, V_{th}, is positive for the N channel (= NMOS) devices and negative for P channel (= PMOS) ones. Define

$$f(x) = \beta x^2 1(x), \quad \beta = \frac{KP}{2}\frac{W}{L} \qquad (5)$$

For an NMOS transistor this model for the current from a to b is

$$i_{a2b} = [f(v_a - v_g - V_{th}) - f(V_b - v_g - V_{th})] \cdot (1 + \lambda \mid v_a - v_b \mid) \qquad (6)$$

When, as in the normal case, $v_a > v_b$ this is the drain current (a = drain, b = source), otherwise it is the source current; in all cases g is the gate. For PMOS devices all quantities, except β and λ, are replaced by their negatives. In most cases λ is small and for design purposes can initially be ignored. Since $(x+y)^2 - (x-y)^2 = 4xy$ these transistors can conveniently be used to obtain multipliers and, for constant y, linear circuits. For dynamic behavior, the transistors exhibit gate to source and drain capacitance, in which case they can also be used to realize VLSI capacitors by connecting the source to the drain as shown in Fig. 2. For Fig. 2 the capacitance is given by

$$C = C_{ox}WL; \quad C_{ox} = \varepsilon e_{ox}/TOX,$$
$$\varepsilon_{ox} = \varepsilon_{si}\,\varepsilon_o; \quad \varepsilon_{si} = 3.97,$$
$$\varepsilon_o = 8.85 \text{ atoFarad/micron} \qquad (7)$$

for which again the transistor width and length serve as design parameters, since the oxide thickness, TOX, and dielectric constant are fixed by the process.

For hand and initial design calculations we will use here the 1.2 micron process Spice parameters of MOSIS

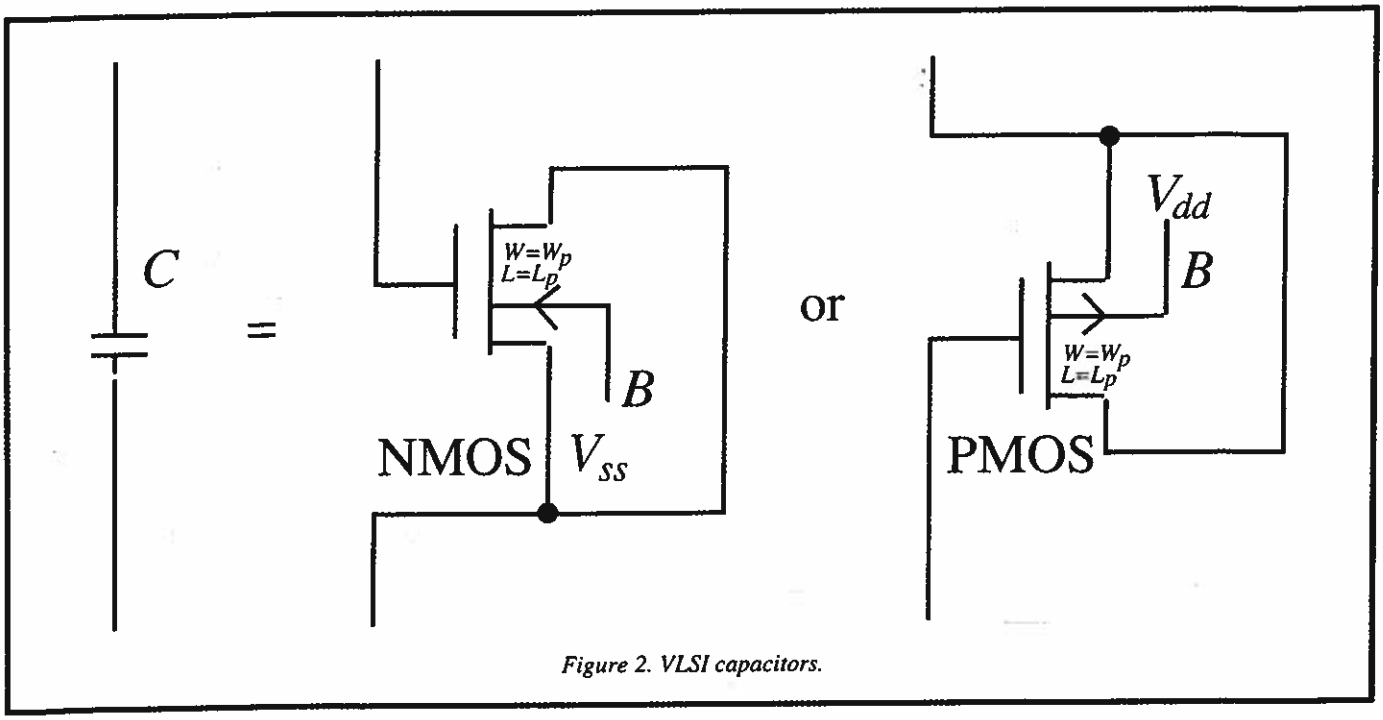


Figure 2. VLSI capacitors.

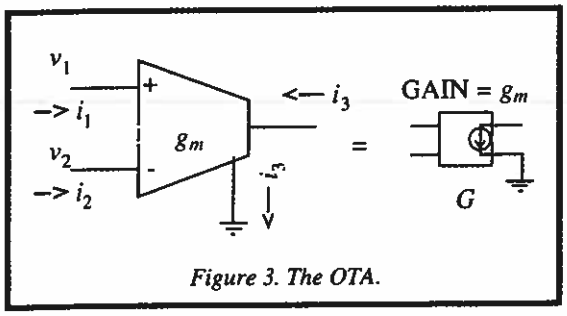


Figure 3. The OTA.

Table 1: Transistor Spice Parameters of Interest

	KP, amp / volt^2	VTO = V_{th}, volt	LAMBDA = λ,volt^{-1} (curve calculated)	TOX, microns
NMOS	7.768×10^{-5}	0.567	1.568×10^{-6}	3.06×10^{-8}
PMOS	1.889×10^{-5}	–0.800	0.0918×10^{-6}	3.06×10^{-8}
Poly to Poly2 capacitance = 611 atoFarads/micron^2; ato = 10^{-18}, micron = $u = \mu = 10^{-6}$				

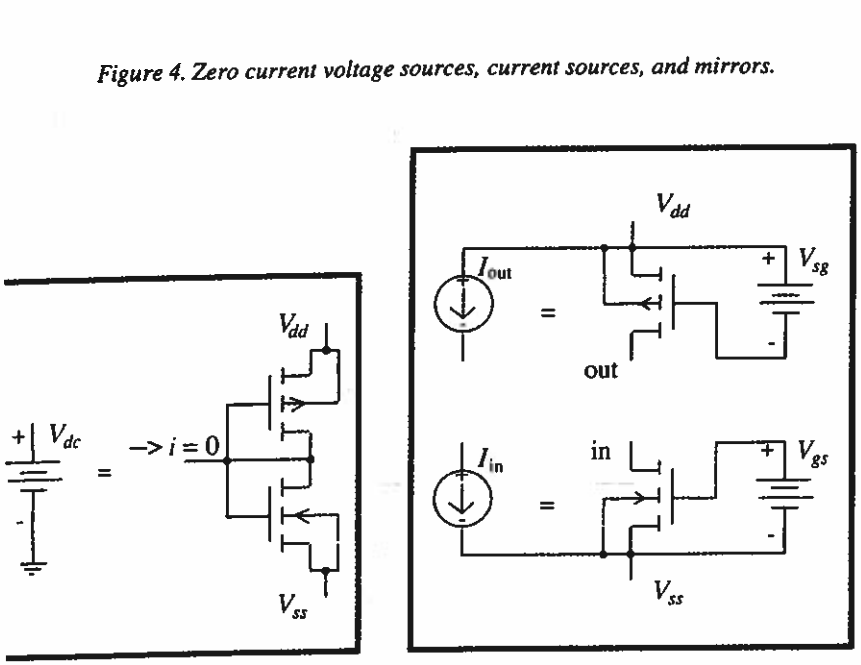
AMI run N7AB which are given in Table 1; for a full set and/or updated parameters one can consult the web for the fabricator of interest, for example [http://www.mosis.org/vendors/ami-abn/n7ab].

One of the most convenient linear time-invariant circuits is the differential voltage controlled current source, DVCCS, alternatively called a (operational) transconductance amplifier, OTA, since it is known that all linear time-invariant circuits can be constructed from them in the presence of capacitors [15]. Figure 3 shows the symbol we will use for the OTA, which is the linear *G* component in Spice, the PSpice symbol also being given in the figure. Its voltage controlled current law is

$$i_1 = i_2 = 0 \qquad \text{(8a, b)}$$

$$i_3 = g_m(v_1 - v_2) \qquad \text{(8c)}$$

Figure 4. Zero current voltage sources, current sources, and mirrors.



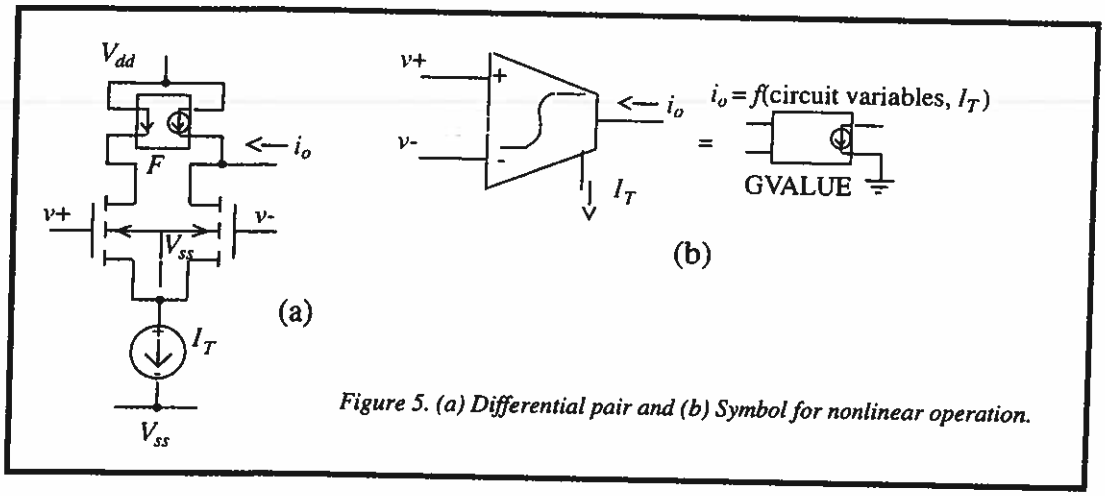
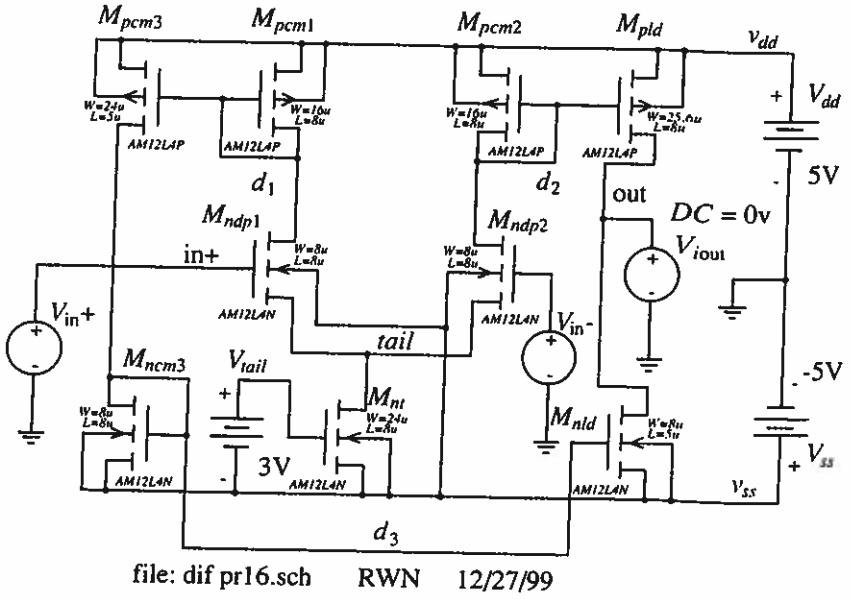
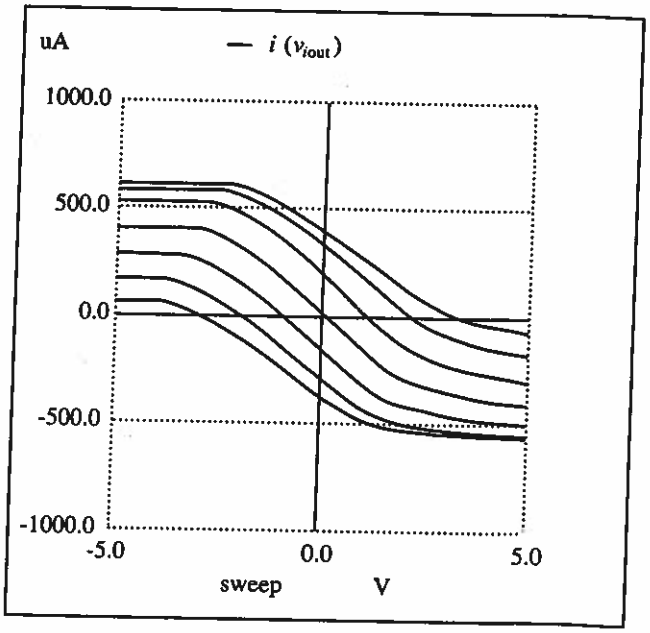


Figure 5. (a) Differential pair and (b) Symbol for nonlinear operation.

Figure 6. (a) CMOS transistorized differential pair (b) Characteristics.



Differential Pair for 1.6u technology & layout
DC analysis: V_{in}+ -5 to +5, 0.1v steps;
nest: V_{in}- -5 to +5, 1v steps



We note that the output current return path to ground shown in Fig. 3 is often omitted but necessary for satisfying Kirchhoff's current law by denoting the current path when setting up a circuit graph as we will do in the next section. In Spice the OTA is equivalent to the *G* device, the symbol for which we also show in Fig. 3. Since current sources, current mirrors, and internal bias voltages are important components of analog VLSI we also show in Fig. 4 their simplest constructions with the Spice *F* component equivalent of the current mirror.

The OTA can be realized in VLSI by operating a differential pair in its linear range with a typical differential pair circuit shown in Fig. 5. In Fig. 5 the Spice current controlled current source, *F*, is readily made in VLSI by current mirrors. The key design parameter of a differential pair is the tail current, I_T, with the full voltage controlled current characteristic being derived by using (6) for the transistor pair being in saturation ($v_a - v_b > v_g - v_b - V_{th}$) assuming $\lambda = 0$. In terms of the differential input voltage, $v_d = v_1 - v_2$, by [16,

Semistate Theory and Analog VLSI Design

p. 432] the output current $I_{out}(v_d)$ is given by

$$\begin{cases} I_T & \sqrt{I_T/\beta} < v_d \\ \sqrt{\beta(2I_T)}v_d \cdot \sqrt{1-\beta(v_d^2/(2I_T))} & -\sqrt{I_T/\beta} \le v_d \le \sqrt{I_T/\beta} \\ -I_T & v_d < -\sqrt{I_T/\beta} \end{cases} \quad (9)$$

From this it is seen that this differential pair acts like the OTA when $|v_d| << \sqrt{2\beta I_T}$. For these small $|v_d|$ we have

$$I_{out}(v_d) = g_m v_d \quad \text{with } g_m = \sqrt{(2I_T)\beta}. \quad (10)$$

In the literature there are many variations and improvements upon this basic circuit [17–19]. But one variation which is important to us is that the upper and lower saturation currents may be changed by inserting a current source at the output to shift the current up or down as may be desired.

The differential pairs can give the nonlinear saturating activation functions of artificial neural networks as well as hysteresis but are most often designed to behave linearly over their range of operation in which case they can be connected as positive or negative resistors (by connecting the output to the unused input). By appropriate combinations squaring devices make available polynomial nonlinearities while exponentials become available when MOS transistors are operated in their subthreshold regime. And although inductors and transformers can be directly fabricated [20] they can also be obtained through gyrator equivalences by the use of capacitors.

Circuit Semistate Equations

In this part we set up semistate equations for a given circuit via circuit analysis using graph theory. To a large degree a precursor to these ideas was set out by Desoer for describing the adjoint circuit [21]. The graph theory material follows to some degree that in texts [22] while some of the synthesis ideas stem from previous techniques [23].

As numbers let t, ℓ, and b be the number of tree branches, link (= cotree) branches and total branches and as subscripts let them indicate tree and

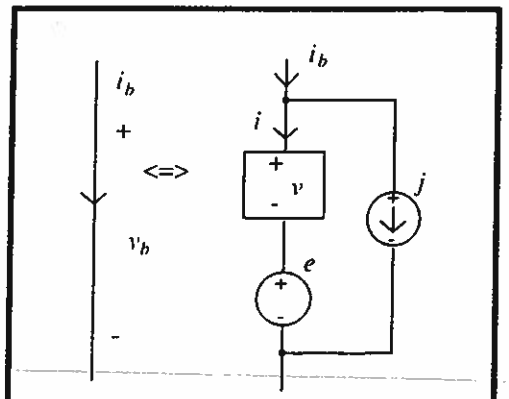


Figure 7. Matrix graph components.

link variables. Assuming a common ground, that is one separate part, the total number of branches is $b = t + \ell$ so that all voltages and currents in the circuit can be found once the tree branch voltages, v_t, and link branch currents, i_ℓ, are known via the Kirchhoff voltage and current laws. In terms of the graph's cut set $t\times b$ matrix $\mathcal{C}$ and $\ell\times b$ tie set matrix $\mathcal{T}$, these laws are

$$0_t = \mathcal{C} i_b, \quad 0 = \mathcal{T} v_b \quad (11a, b)$$

where (11a) is found by summing cur-

rents into closed surfaces each cut and directed by only one tree branch and (11b) by summing voltages around closed loops with one cotree branch in and directing each loop. For a finite graph, by encircling with a large sphere into which no power can enter, we have zero for the total power in, $P_{in} = v_b^T i_b = 0$, where the superscript T denotes matrix transpose. This shows that the Kirchhoff laws are equivalent to

$$v_b = \begin{bmatrix} v_t \\ v_\ell \end{bmatrix} = \mathcal{C}^T v_t, \quad i_b = \begin{bmatrix} i_t \\ i_\ell \end{bmatrix} = \mathcal{I}^T i_\ell,$$

$$\mathcal{C}\mathcal{I}^T = 0_{t\times\ell} \qquad \text{(11c, d, e)}$$

This leads us to one possible choice of the semistate as

$$x = \begin{bmatrix} v_t \\ i_\ell \end{bmatrix} \qquad (12)$$

Equations (11a, b) give the laws of connections of the circuit, so in order to get the circuit description we need the laws of the components being connected. By placing driving sources outside of the transistor-capacitor branches we take the generic, matrix, branch as shown in Fig. 7 where

$$i_b = i + j, \qquad v_b = v + e \qquad \text{(13a, b)}$$

Considering first the linear time-invariant case with components described by admittances with all dynamics in capacitors placed in the first c branches of the tree

$$i = (sC_{ap} + Y_{alg})v \qquad (14)$$

where C_{ap} is a diagonal matrix of the nonzero capacitor values, $C_{ap} = \text{diag}(c_1, \ldots, c_c, 0, \ldots, 0)$ and Y_{alg} is a constant matrix in s with its first c rows and columns zero. Assuming also that no independent voltage sources are in a capacitor branch, substitutions of the connection laws (11, 13) into the component laws (14) gives

$$\mathcal{I}^T i_\ell - j = (sC_{ap} + Y_{alg})(\mathcal{C}^T v_t - e)$$

$$= sC_{ap}\mathcal{C}^T v_t + Y_{alg}\mathcal{C}^T v_t - Y_{alg}e \qquad (15)$$

Upon combining terms and noting that the source terms e and j are inputs in the linear case, we have, with 1_b the bxb identity matrix, the first portion of the semistate equations

$$Esx = [C_{ap}\mathcal{C}^T, 0]sx = [-Y_{alg}\mathcal{C}^T, \mathcal{I}^T]x$$

$$+ [-1_b, Y_{alg}]\begin{bmatrix} j \\ e \end{bmatrix} = Ax + Bu \qquad (16)$$

Noting also that any voltages or currents, including output ones, will be a linear combination of the tree branch voltages and link currents, there is some matrix C such that $y = Cx$.

Example 2:

For the circuit of Fig. 8 the directed graph is chosen as shown on the right with branches 1 and 2 for the tree and

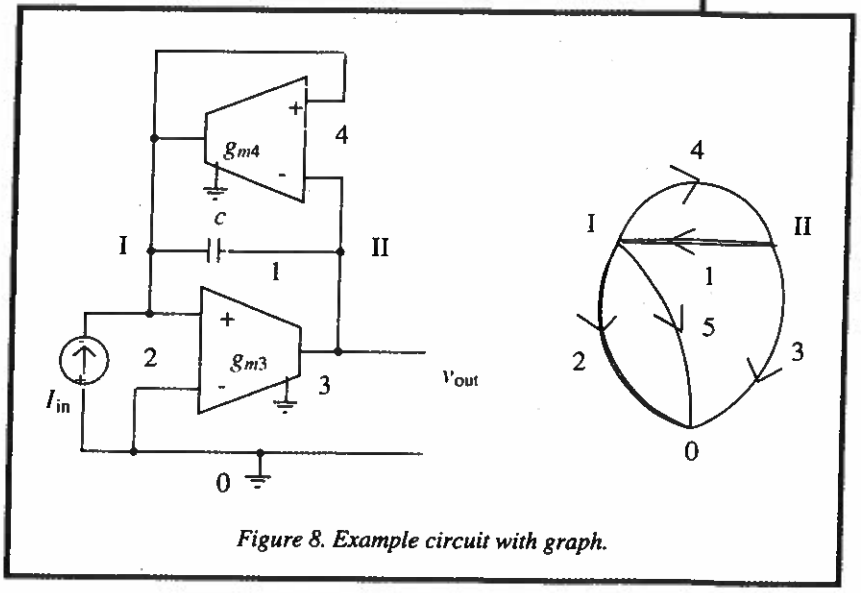


Figure 8. Example circuit with graph.

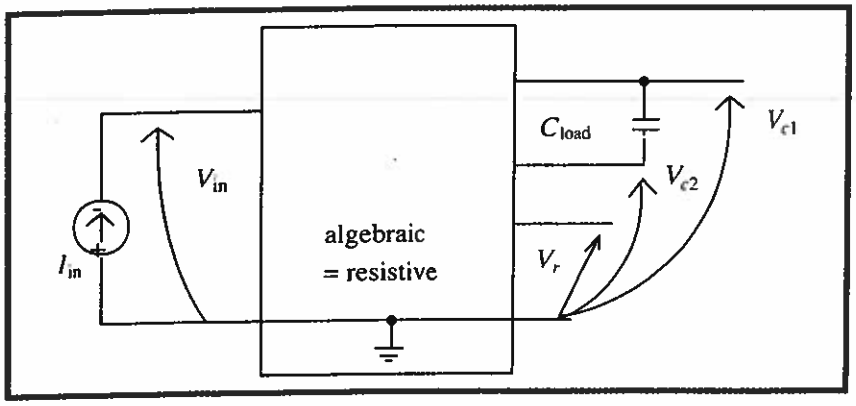


Figure 9. Capacitor and node extraction.

3, 4, 5 for the links. In the graph branch 2 combines i_{in} with the input for g_{m3}, branches 3 and 5 are for the current outputs of the two differential amplifiers.

We find

$$\begin{bmatrix}\text{cut set for branch 1}\\ \text{cut set for branch 2}\end{bmatrix} \Rightarrow \begin{bmatrix}0\\0\end{bmatrix} = \begin{bmatrix}1 & 0 & 1 & -1 & 0\\ 0 & 1 & 1 & 0 & 1\end{bmatrix} i_b \quad (17a)$$

$$\begin{bmatrix}\text{tie set for branch 3}\\ \text{tie set for branch 4}\\ \text{tie set for branch 5}\end{bmatrix} \Rightarrow \begin{bmatrix}0\\0\\0\end{bmatrix} = \begin{bmatrix}-1 & -1 & 1 & 0 & 0\\ 1 & 0 & 0 & 1 & 0\\ 0 & -1 & 0 & 0 & 1\end{bmatrix} v_b \quad (17b)$$

$$e = 0,\quad j = \begin{bmatrix}0\\-i_{in}\\0\\0\\0\end{bmatrix},\quad i = \begin{bmatrix}sc & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\\ 0 & g_{m3} & 0 & 0 & 0\\ 0 & 0 & 0 & g_{m4} & 0\\ 0 & 0 & 0 & 0 & 0\end{bmatrix} v \quad (17c, d, e)$$

giving for Eq. (16)

$$\begin{bmatrix}c & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0 & 0\end{bmatrix} sx = \begin{bmatrix}0 & 0 & -1 & 1 & 0\\ 0 & 0 & -1 & 0 & -1\\ 0 & -g_{m3} & 1 & 0 & 0\\ 0 & 0 & 0 & 1 & 0\\ g_{m4} & 0 & 0 & 0 & 1\end{bmatrix} x + \begin{bmatrix}0\\1\\0\\0\\0\end{bmatrix} i_{in} \quad (17f)$$

$$v_{out} = [1 \quad 1 \quad 0 \quad 0 \quad 0]x \quad (17g)$$

As a different output vector we can take y to consist of the two external voltages giving

$$y = \begin{bmatrix}v_{in}\\ v_{out}\end{bmatrix} = \begin{bmatrix}0 & 1 & 0 & 0 & 0\\ 1 & 1 & 0 & 0 & 0\end{bmatrix} x \quad (17h)$$

Using this latter output and solving the equations by eliminating semistate variables yields for the transfer function matrix

$$\begin{bmatrix}v_{in}\\ v_{out}\end{bmatrix} = T(s) i_{in} \quad (17i)$$

$$T(s) = \begin{bmatrix}z_{in}(s)\\ z_{21}(s)\end{bmatrix} = \begin{bmatrix}\dfrac{sc}{g_{m3}(sc+g_{m4})}\\ \dfrac{sc-g_{m3}}{g_{m3}(sc+g_{m4})}\end{bmatrix} \quad (17j)$$

The inverse of the first entry of this transfer function, that is $y_{in} = 1/z_{in}$, can also be obtained by using the same semistate but modifying the second row of the A matrix to read [0 −1 0 0 0], the input to be v_{in}, and the output equation to be $i_{in} = [0\ 0\ 1\ 0\ 1]x$.

An alternate procedure which will prove of more value when we turn to synthesis is to extract the capacitors and attach external leads to all internal nodes, as shown in Fig. 9. Possibly considering virtual branches (open circuit branches of zero admittance) from every node to ground, and taking node to ground branches as tree branches, allows node equations to be written for the circuit.

Example 3:

This procedure is illustrated by the circuit of the previous example where, after the capacitor and input source extraction, we are left with the algebraic circuit of Fig. 10.

By summing currents at the nodes I and II, with v_I, v_{II}, i_I, and i_{II} being node to ground voltages and externally entering node currents, we get the nodal admittance matrix description for Fig. 10.

Setting these currents to their values for the loading of Fig. 7 gives

$$\begin{bmatrix} -g_{m4} & g_{m4} \\ -g_{m3} & 0 \end{bmatrix} \begin{bmatrix} v_{\mathrm{I}} \\ v_{\mathrm{II}} \end{bmatrix} = \begin{bmatrix} i_{\mathrm{I}} \\ i_{\mathrm{II}} \end{bmatrix}$$

$$= \begin{bmatrix} sc(v_{\mathrm{I}} - v_{\mathrm{II}}) - i_{\mathrm{in}} \\ sc(v_{\mathrm{II}} - v_{\mathrm{I}}) \end{bmatrix} \qquad (18a)$$

Using the node voltages as the semistate, $x = [v_{\mathrm{I}}, v_{\mathrm{II}}]^T$, semistate equations are

$$\begin{bmatrix} c & -c \\ -c & c \end{bmatrix} sx$$

$$= \begin{bmatrix} -g_{m4} & g_{m4} \\ -g_{m3} & 0 \end{bmatrix} x + \begin{bmatrix} 1 \\ 0 \end{bmatrix} i_{\mathrm{in}} \qquad (18b)$$

$$y = v_{\mathrm{in}} = [1 \;\; 0]\, x \qquad (18c)$$

By direct calculation of $T(s) = C(sE - A)^{-1}B$ we check the transfer function, $z_{\mathrm{in}}(s) = sc/[g_{m3}(sc + g_{m4})]$, found in Example 2.

Example 4:

As preparation for the synthesis of the next section, here we replace the input current source in Fig. 8 by a voltage source v_{in} for the input and take the current from it as the output, i_{in}. The equations of Example 3 are still valid but need to be augmented to incorporate this input and output. For this we number the left terminal of node I as III and now take $x_3 = i_{\mathrm{III}} = i_{\mathrm{in}}$, $x_4 = v_{\mathrm{I}} = v_{\mathrm{III}} = v_{\mathrm{in}}$. The semistate equations for this case become

$$\begin{bmatrix} c & -c & 0 & 0 \\ -c & c & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} sx = \begin{bmatrix} -g_{m4} & g_{m4} & 1 & 0 \\ -g_{m3} & 0 & 0 & 0 \\ -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ 0 \\ -1 \end{bmatrix} v_{\mathrm{in}} \qquad (19a)$$

$$i_{\mathrm{in}} = [0 \quad 0 \quad 1 \quad 0]x \qquad (19b)$$

In this case the transfer function is

$$\frac{i_{\mathrm{in}}}{v_{\mathrm{in}}} = y_{\mathrm{in}}(s) = g_{m3}\left(\frac{sc + g_{m4}}{sc}\right) \qquad (19c)$$

which also checks the result from Example 2 since $y_{\mathrm{in}} = 1/z_{\mathrm{in}}$. We comment that although as a 2-terminal pair the circuit has an admittance matrix as used in Example 3, as a 3-terminal pair it does not have an admittance since $v_{\mathrm{I}} = v_{\mathrm{III}}$. Nevertheless, by the methods of the next section we can synthesize $y_{\mathrm{in}}(s)$ via an admittance matrix.

Turning to nonlinear circuits, we assume voltage controlled current devices, as we may through circuit equivalences [10]. Assuming, as we may by equivalences, that all capacitors are linear, time-invariant, and placed in the first c of the tree branches we can write

$$i = \mathcal{Y}(v, t) = [sCapv_t \oplus 0_t] + [0_c \oplus \mathcal{Y}_a(\mathcal{C}^T v_t - e, t)] \qquad (20)$$

where $\oplus$ denotes the direct sum and $Cap = \mathrm{diag}[c_1, \ldots, c_c \oplus 0_{b-c}]$ is a diagonal matrix of the c nonzero capacitance values; $\mathcal{Y}_a(\,,\,)$ is purely algebraic containing no derivatives since it describes the resistive elements, including the nonlinear DC transistor characteristics. Using (13a, b) and (20)

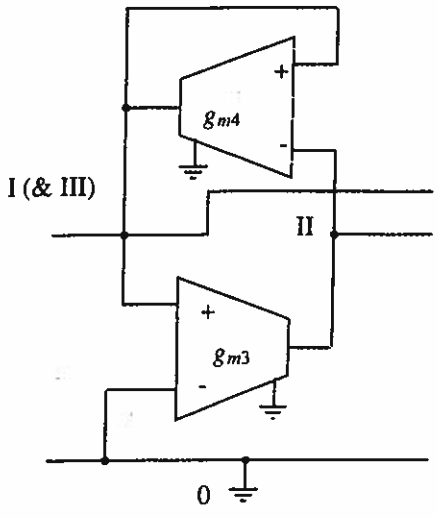


Figure 10. Algebraic circuit for Examples 3 and 4.

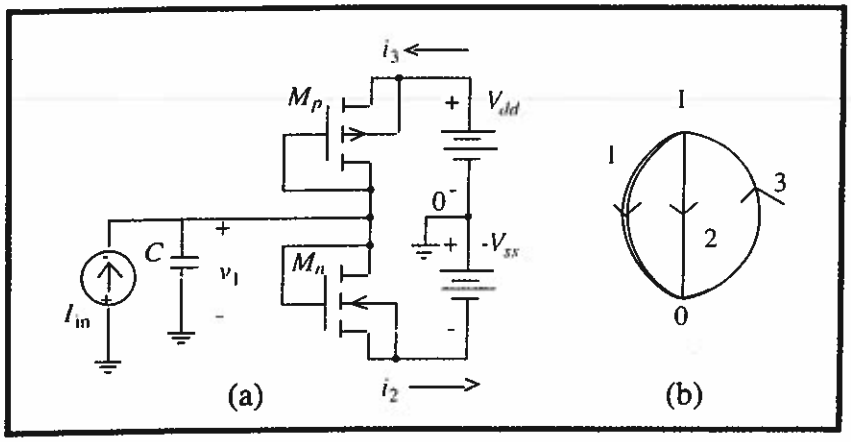


Figure 11. (a) Circuit, (b) Graph; $C - I_{in}$ *in 1,* $M_n - V_{ss}$ *in 2,* $M_p - V_{dd}$ *in 3.*

$$[sCap(v_t \oplus 0_t)] = \mathcal{A}^T i_t - [0_c \oplus \mathcal{Y}_a(\mathcal{C}^T v_t - e, t)] - j \qquad (21)$$

Example 5:

For the circuit of Fig. 11 we can take $x = [v_1, i_2, i_3]^T$ as the semistate. Then assuming the capacitor voltage as the output, Eq. (21) gives

$$\begin{bmatrix} c & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} sx = \begin{bmatrix} 0 & -1 & 1 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix} x + \qquad (22a)$$

$$\begin{bmatrix} 0 \\ \beta_n(v_1 - V_{ss} - V_{thn})^2 1(v_1 - V_{ss} - V_{thn}) \\ \beta_p(V_{dd} - v_1 - V_{thp})^2 1(V_{dd} - v_1 - V_{thp}) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} I_{in}$$

$$y = [1 \quad 0 \quad 0]x \qquad (22b)$$

Equations (22a) are readily reduced to one equation in v_1 by subtracting the second row from the first and adding the third to the first. Normally the bias voltages V_{dd} and V_{ss} would be chosen such that $V_{ss} + V_{thp} < v_1 < V_{dd} - V_{thn}$, in which case both of the transistors are always on in saturation and we obtain

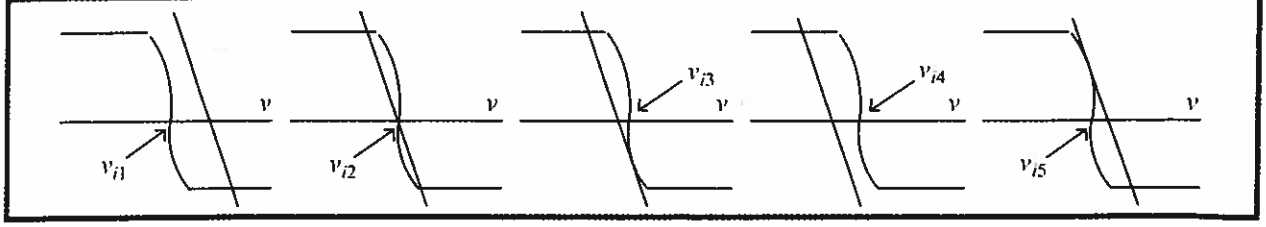
$$c\frac{dv_1}{dt} = (\beta_p - \beta_n)v_1^2 + 2(\beta_n(V_{ss} + V_{thn}) - \beta_p(V_{dd} - V_{thp}))v_1 + (\beta_p(V_{dd} - V_{thp})^2 - \beta_n(V_{ss} + V_{thn})^2) + I_{in} \qquad (22c)$$

From this we see that if $\beta_p = \beta_n$, which is easily accomplished by choice of (W/L) ratios, then the transistor portion of the circuit acts like a linear resistor with a voltage offset; more is said about this circuit later at Fig. 18.

Example 6:

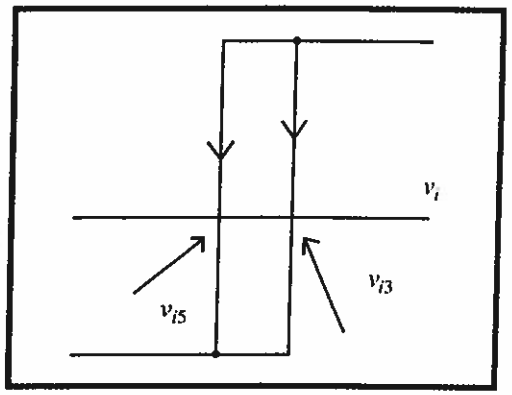
Hysteresis is a very nonlinear phenomena for which a class of CMOS circuits yielding hysteresis can be described nicely by the semistate equations as we discuss here. Consider Fig. 12 where a nonlinear curve, as results for a differential pair, slides by a linear curve, as can result from the right of Fig. 11 when $\beta_p = \beta_n$. The sliding first goes from left to right as v_i increases up to v_{i4} and afterwards slides back left. At first there is one intersection, as for $v_i = v_{i1}$ in (a), then three intersections as for $v_i = v_{i2}$ in (b), next a jump to the upper curve as v_i increases above v_{i3} of (c). As v_i continues to increase the common intersection remains at the upper value of the nonlinear curve but when v_i decreases below v_{i4} to v_{i5} there is a jump to the lower value of the differential pair curve, re-

Figure 12. Hysteresis process.



$$\begin{bmatrix} c_{par} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} sx = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 0 & -1 & 0 & 0 \\ -b & 0 & -1 & 0 \\ 0 & 0 & 0 & -1 \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ a \\ i(x_1, x_2) \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix} v_i \quad (24a)$$

Figure 13. Resulting hysteresis.



peating the situation at v_{i1}. If $v_{i5} < v_{i3}$ there will be hysteresis with actually a triple valued curve between the two jump values of v_i. However, the middle point is unstable while parasitic capacitance will hold the hysteresis to the branch it is on prior to a jump. The result is a hysteresis curve as seen in Fig. 13.

This hysteresis can be well described by semistate equations. Let the linear portion be described by the constant negative slope, $-b$, and constant v axis intersect, a, via

$$i_1(v) = a - bv \quad (23a)$$

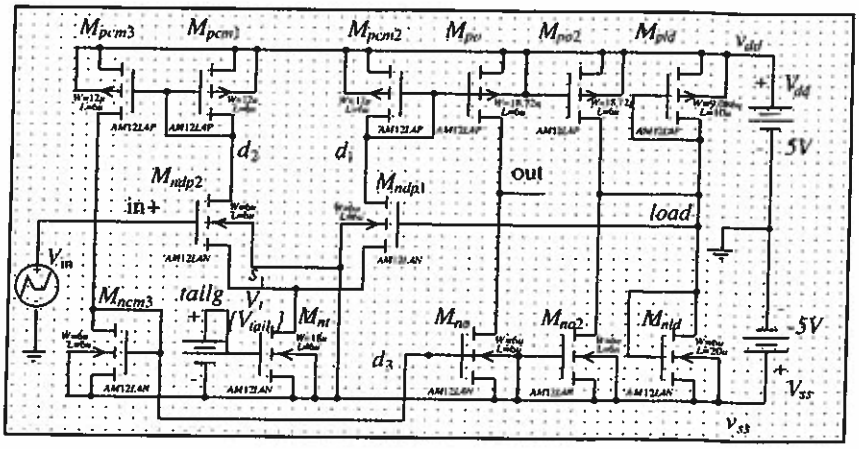
and then the nonlinear portion by

$$i_2 = i(v, v_1) = \begin{cases} I_{hi} & -V_{dl} \le v \\ f(v_i - v) & -V_{dl} < v < V_{d2} \\ I_{lo} & v \le V_{d2} \end{cases} \quad (23b)$$

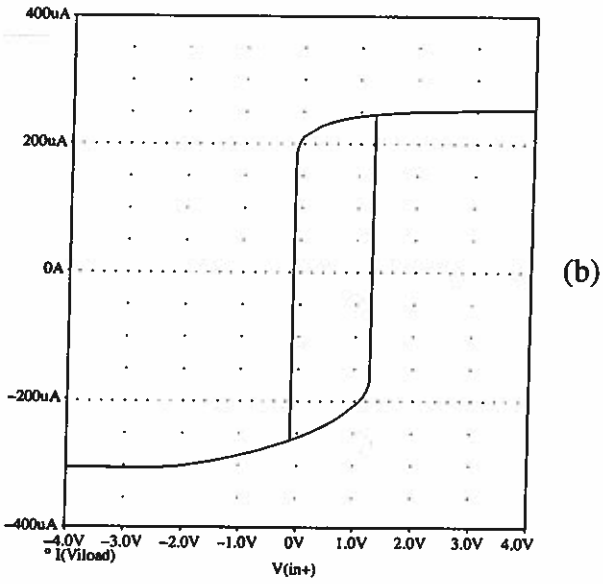
Inserting the parasitic capacitance, c_{par}, at the connection of the devices giving Eqs. (23a, b) allows the semistate equations to be written using $x = [v, v_i, i_1, i_2]^T$, $u = v_i$, $y = i_{out} = i_2$ (most likely by use of a current mirror), as

$$i_{out} = [0 \quad 0 \quad 1 \quad 0]x \quad (24b)$$

From these equations it is to be noted that transistorized hysteresis results from multivalued solutions of the two single valued functions of (23) with this hysteresis being described via the single valued semistate equations for very small parasitic capacitance (in the limit as $c_{par} \to 0$).



(a)



(b)

Figure 14. (a) CMOS hysteresis circuit, (b) Resulting hysteresis.

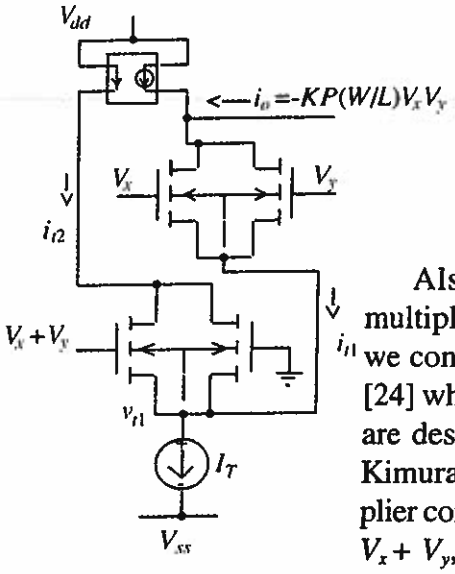


Figure 15. Multiplier core.

Also of considerable interest is multiplication of two signals. For this we consider the multiplier of Kimura [24] while a number of similar circuits are described in [25]. This circuit of Kimura contains two parts: the multiplier core takes three inputs, V_x, V_y, and $V_x + V_y$, as shown in Fig. 15, and another part to obtain $V_x + V_y$ from the other two inputs, as shown in Fig. 16.

Assume that all the transistors are identical and of the same W/L ratio and that the current mirrors have unity gain. Turning first to the multiplier core, one can set up full semistate equations but in this case we note that the output current is the difference of the two currents

$$i_{t1} = \beta\{[V_x - (v_{t1} + V_{th})]^2 + [V_y - (v_{t1} + V_{th})]^2\} \quad (25a)$$

$$i_{t2} = \beta\{[V_x + V_y - (v_{t1} + V_{th})]^2 + [0 - (v_{t1} + V_{th})]^2\} \quad (25b)$$

On subtracting it is seen that the square terms and terms with $v_{t1} + V_{th}$ all cancel with the result

$$i_o = -KP(\frac{W}{L})V_xV_y \quad (26)$$

It is to be noted that this is independent of the tail current and can be adjusted by the transistor width to length ratios.

For the adder we have

$$v_o - (v_{t3} + V_{th}) = \sqrt{i_o/\beta}, \quad V_y - (v_{t3} + V_{th}) = \sqrt{(I_T - i_o)/\beta},$$

$$V_x - (v_{t2} + V_{th}) = \sqrt{i_o/\beta}, \quad 0 - (v_{t2} + V_{th}) = \sqrt{(I_T - i_o)/\beta}$$

(27a, b)

On subtracting the last three expressions from the first we get, again independent of the (equal) tail currents

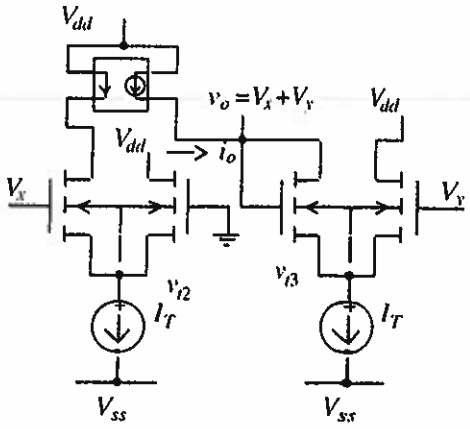


Figure 16. Voltage adder.

$$v_o = V_y + V_x \quad (28)$$

Consequently connecting the voltage adder to the multiplier core yields an excellent four quadrant multiplier. The fully transistorized circuit is shown in Fig. 17 with its response in Fig. 18 where it is seen that, as naturally expected, multiplication is valid over about one-fifth of the bias voltage range.

In some cases it is necessary to convert an output current into a voltage, as could occur with this multiplier or with an OTA. For this conversion the circuit of Fig. 19 is very convenient. As already seen in Example 5 this can determine a linear conductance law. Determination of the law results by summing currents at the input node to obtain

$$I_{in} = I_{Dn} - I_{Sp} = \beta_n(\alpha_1)^2 1(\alpha_1)$$

$$- \beta_p(\alpha_2)^2 1(\alpha_2)$$

where

$$\alpha_1 = V_{in} - V_{ss} - V_{thn}$$

$$\alpha_2 = V_{dd} - V_{in} + V_{thp} \quad (29)$$

When both transistors are turned on, by expanding we can cancel the V_{in}^2 term if we set $\beta_n = \beta_p$ in which case a linear resistive curve with some offset

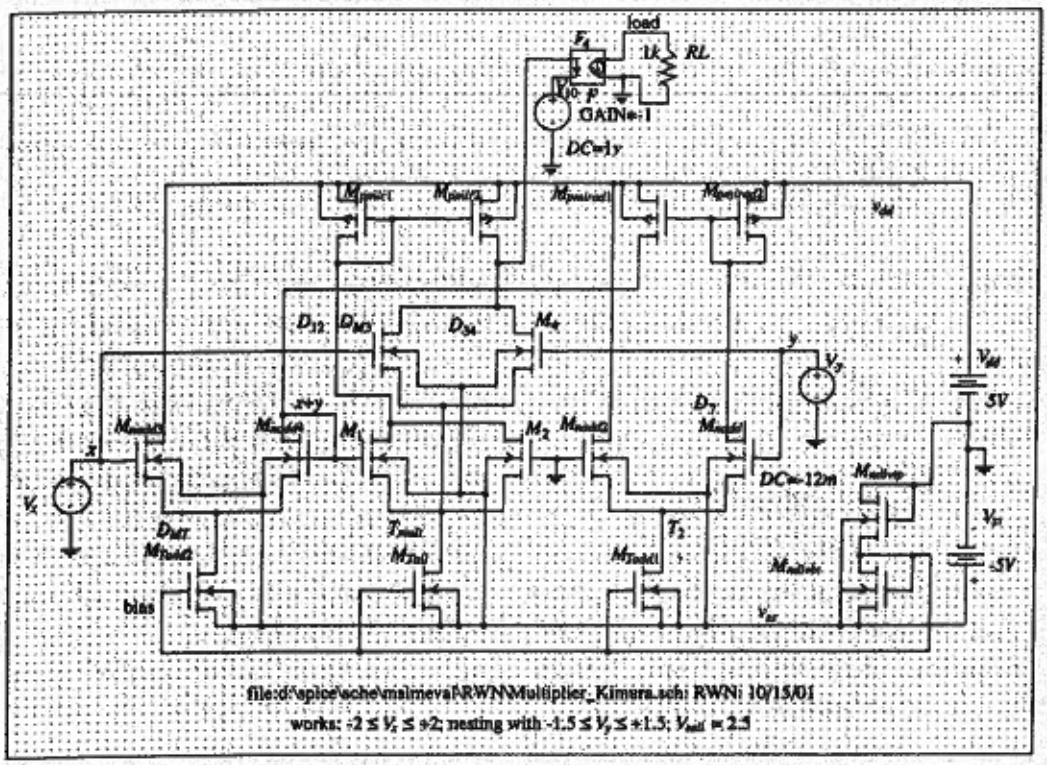


Figure 17. Transistorized multiplier.

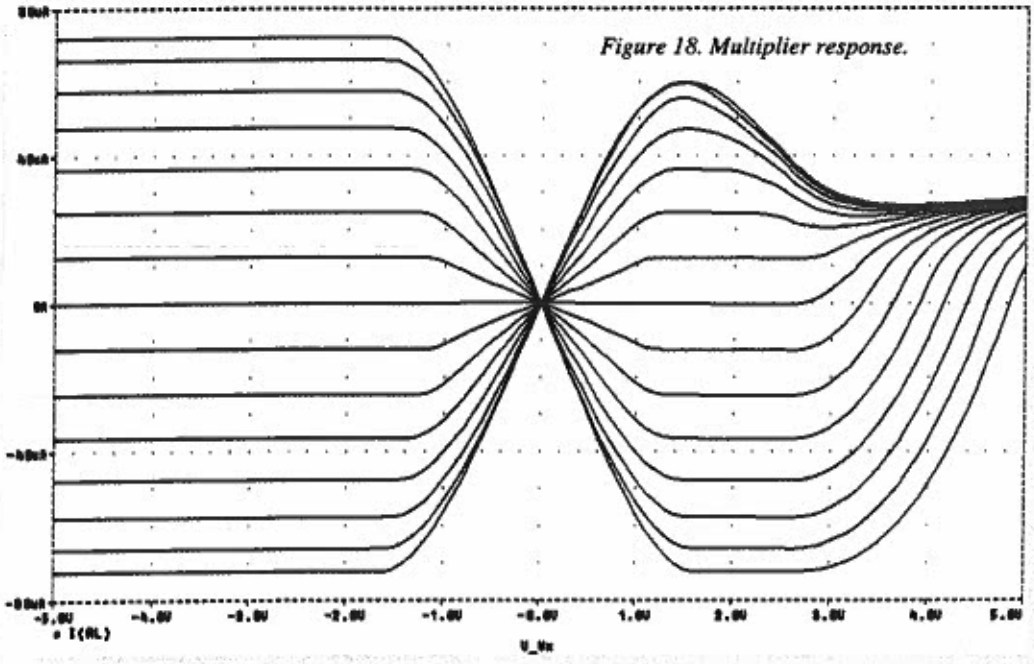


Figure 18. Multiplier response.

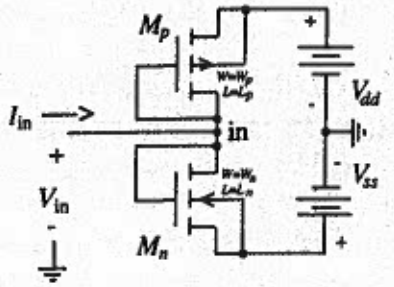


Figure 19. Load for I to V conversion.

is obtained over a mid range of V_{in}. If $V_{ss} = -V_{dd}$ this offset is small and readily cancelled by a compensating current source. Thus if $\beta = \beta_n = \beta_p$

$$I_{\text{in}} = \begin{cases} -\beta(V_{\text{in}} - V_{ss} - V_{thn}) & V_{dd} + V_{thp} \le V_{\text{in}} \\ G_{\text{in}} V_{\text{in}} + I_{\text{off}} & V_{ss} + V_{thn} \le V_{\text{in}} \le V_{dd} + V_{thp} \\ \beta(V_{dd} - V_{\text{in}} + V_{thp}) & V_{\text{in}} \le V_{ss} + V_{thn} \end{cases} \quad (30a)$$

where

$$G_{in} = 2\beta(V_{dd} - V_{ss} + V_{thp} - V_{thn}) \quad (30b)$$

$$I_{off} = \beta([V_{ss} + V_{thn}]^2 - [V_{dd} + V_{thp}]^2) \quad (30c)$$

Synthesis of Linear Semistate Equations

At this point for synthesis we assume linear time-invariant semistate equations are given to us and we desire to synthesize by a vlsi circuit. Given a transfer function the semistate equations can be set up as shown elsewhere [12] and summarized in the Appendix.

For identification with a circuit we write the semistate equations in the form

$$\begin{bmatrix} sEx \\ y \end{bmatrix} = \begin{bmatrix} A & B \\ C & 0 \end{bmatrix} \begin{bmatrix} x \\ u \end{bmatrix} \quad (31)$$

Here the zero is the zero nxm matrix, E and A are kxk, B is kxm and C is nxk.

We initially take the structure of Fig. 20 as the basis of the synthesis. In Fig. 20 all terminals' voltages and currents are taken to be vectors and we assume that there are c capacitors all of which are grounded and serve as a load on a portion of a resistive subcircuit. Initially we also take $u = V_{in}$ and $y = I_{in}$ as input and output quantities. Assuming the existence of an admittance matrix under linearity and time-invariance for the resistive subcircuit we have

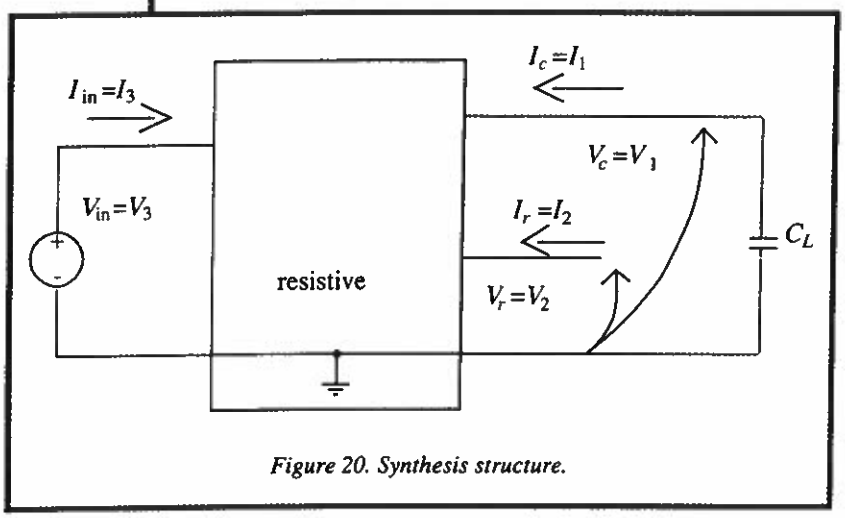


Figure 20. Synthesis structure.

$$\mathrm{i} = \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} -i_c = -C_L \dfrac{dv_c}{dt} \\ 0 \\ i_{in} = y \end{bmatrix} \quad (32)$$

$$= \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 = v_c \\ v_2 = v_r \\ v_3 = v_{in} = u \end{bmatrix}$$

From this equation we see that we may take the semistate as the voltages on the right side of Fig. 20, that is

$$x = \begin{bmatrix} v_c \\ v_r \end{bmatrix} \quad (33a)$$

If v_c is a c-vector then the remaining semistate r-vector has $r = k - c$. We can now read off from (4.1)

$$\begin{bmatrix} C_L & 0 \\ 0 & 0 \end{bmatrix} sx = \begin{bmatrix} -Y_{11} & -Y_{12} \\ -Y_{21} & -Y_{22} \end{bmatrix} x + \begin{bmatrix} -Y_{13} \\ -Y_{23} \end{bmatrix} u \quad (33b)$$

$$\mathrm{y} = \begin{bmatrix} Y_{31} & Y_{32} \end{bmatrix} x + [Y_{33}] u \quad (33c)$$

On identifying (33b, c) with (31) we see we can choose the admittance matrix in terms of the semistate real-

ization as

$$\begin{bmatrix} C_L & 0_{crx} \\ 0_{rxc} & 0_{rxr} \end{bmatrix} = E, \begin{bmatrix} -Y_{11} & -Y_{12} \\ -Y_{21} & -Y_{22} \end{bmatrix} = A,$$

$$\begin{bmatrix} -Y_{13} \\ -Y_{23} \end{bmatrix} = B, \begin{bmatrix} Y_{31} & Y_{32} \end{bmatrix} = C,$$

$$[Y_{33}] = 0_{mxm} \qquad (34a, b, c, d, e)$$

where the sizes of the zero matrices are indicated by their subscripts which also designate the sizes of the other submatrices. Consequently we have the nodal admittance matrix

$$Y_{\text{nodal}_1} = \begin{bmatrix} -A & -B \\ C & 0 \end{bmatrix} \qquad (35a)$$

which can be realized by OTAs with the first c terminals terminated by capacitors C_L connected to ground, the next r terminals terminated by open circuits and the final terminals fed by current sources, $u = i_{in}$, with the output being the voltages, $y = v_{in}$, across the current sources. Of considerable importance for practical realizations are the transformations of (2) which allow us to replace the admittance of Eq. (35a) by

$$Y_{\text{nodal}} = \begin{bmatrix} -PAQ & -gPB \\ gCQ & 0 \end{bmatrix} \qquad (35b)$$

Since E is to be realized by the capacitance matrix, C_L, along with open circuits, we desire that C_L be diagonal with positive entries. By the use of the P and Q of (2) this can be assured. However, the admittance matrix of the resistive circuit is to be realized by OTAs and, consequently, can be arbitrary, though one would like it to be as close to skew and/or positive semidefinite as possible for sensitivity and stability reasons.

Example 7:

Let us realize the input admittance $y_{in}(s) = sc / [g_{m3}(sc + g_{m4})]$, which is the dual of the first entry of Eq. (17i), by this method. We already have a semistate realization in Eqs. (18a, b) except that we need to change the input and output variable to their duals. This gives the realization

$$\begin{bmatrix} c & -c \\ -c & c \end{bmatrix} sx = \begin{bmatrix} -g_{m4} & g_{m4} \\ -g_{m3} & 0 \end{bmatrix} x + \begin{bmatrix} 1 \\ 0 \end{bmatrix} v_{in} \qquad (36a)$$

$$y = i_{in} = [1 \quad 0]x \qquad (36b)$$

We note that the E matrix is positive semidefinite if $c > 0$ but not diagonal. Consequently we desire to use the matrices P and Q of Eq. (2). We can choose these so that E becomes $c \oplus 0$ by the use of (these add the first row of E and A to the second and then the first columns to the second)

$$P = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}, \quad Q = P^T = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix} \qquad (37a, b)$$

Then inserting the common input-output scaling by g, the transformed semistate equations become

$$\begin{bmatrix} c & 0 \\ 0 & 0 \end{bmatrix} sx = \begin{bmatrix} -g_{m4} & 0 \\ -(g_{m3} + g_{m4}) & -g_{m3} \end{bmatrix} x + \begin{bmatrix} g \\ g \end{bmatrix} v_{in} \qquad (38a)$$

$$y = i_{in} = [g \quad g]x \qquad (38b)$$

giving, from Eq. (35), the nodal admittance

$$Y_{\text{nodal}} = \begin{bmatrix} g_{m4} & 0 & -g \\ g_{m3} + g_{m4} & g_{m3} & -g \\ g & g & 0 \end{bmatrix} \qquad (38c)$$

This nodal admittance can be realized by seven OTAs, one for each term. However, by using suitable transformations we can reduce the number of OTAs required. For example by subtracting the second row and column from the first, without changing the E matrix, we can reduce the number of OTAs to five via

$$Y_{\text{nodal}_2} = (P \oplus 1) Y_{\text{nodal}} (Q \oplus 1)$$

$$= \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} g_{m4} & 0 & -g \\ g_{m3}+g_{m4} & g_{m3} & -g \\ g & g & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 \\ -1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} 0 & -g_{m3} & 0 \\ g_{m4} & g_{m3} & -g \\ 0 & g & 0 \end{bmatrix} \tag{38d}$$

A circuit is as shown in Fig. 21 (which follows Fig. 20). Terminating terminal one in the capacitor c and terminal 2 in an open circuit gives the desired $y_{\text{in}}(s) = sc / [g_{m3}(sc + g_{m4})]$ at terminal 3.

we would have $1 >> g_m$ leading to OTAs out of range for the last row and column terms.

Several things are worth noting. First, the transfer function is a positive real driving point admittance and hence realizable by standard techniques [22, p. 336] by passive elements. But Y_{nodal} is not a positive real matrix and, hence, not realizable by passive elements. Since we are interested in realization by vlsi circuits, which rely heavily upon active transistors, this is not of serious concern though passive circuit realizations may have some advantage in other regards, such as sensitivity to element changes. The realization of Fig. 21 is not far off from being positive real since the two OTAs on the left form a gyrator and the two on the upper right are close to being a gyrator; the OTA on the lower right forms a positive, and hence passive, resistor.

Nevertheless, the nodal admittance can be made positive real by insertion

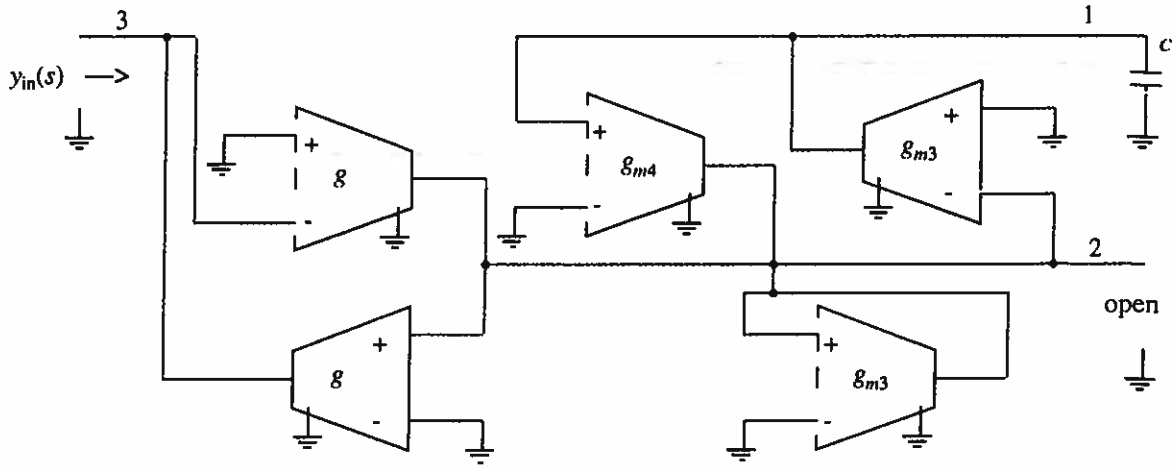
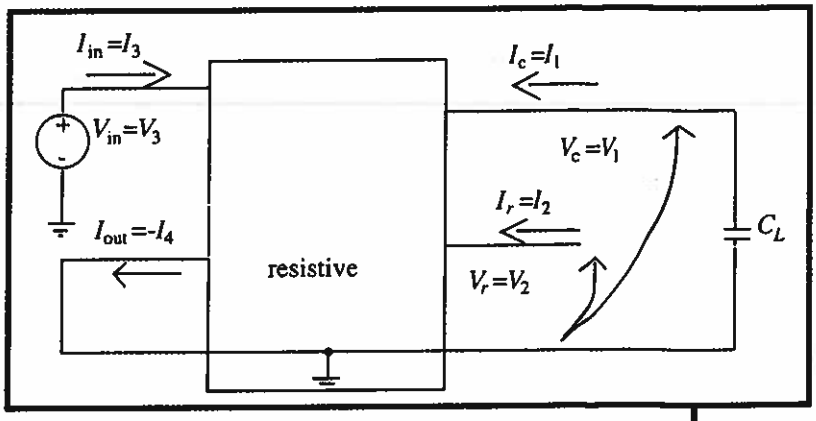


Figure 21. OTA realization for Example 7.

Note that g is used to bring the unity terms in B and C within the conductance range of practical OTAs, since without this scaling away from unity, of a dummy semistate, x_3, which we force to zero by the semistate equations. Multiplying it by the conductance g_1 gives

Figure 22. Transfer admittance structure.



$$Y_{\text{nodal}_3} = \begin{bmatrix} g_{m4} & 0 & 0 & -g \\ g_{m3}+g_{m4} & g_{m3} & 0 & -g \\ 0 & 0 & g_1 & 0 \\ g & g & 0 & 0 \end{bmatrix} \quad (38e)$$

This can be made positive real by a P and Q which do not destroy the E matrix. Thus adding multiples of the third column to the first two and then adding a multiple of the third row to the first two allows us to obtain

$$Y_{\text{nodal}_4} = \begin{bmatrix} g_{m4}+g_1 & -\left(\frac{g_{m3}+g_{m4}}{2}\right) & g_1 & -g \\ \left(\frac{g_{m3}+g_{m4}}{2}\right) & g_{m3}+\frac{(g_{m3}+g_{m4})^2}{4g_1} & -\left(\frac{g_{m3}+g_{m4}}{2}\right) & -g \\ -g_1 & \left(\frac{g_{m3}+g_{m4}}{2}\right) & g_1 & 0 \\ g & g & 0 & 0 \end{bmatrix} \quad (38f)$$

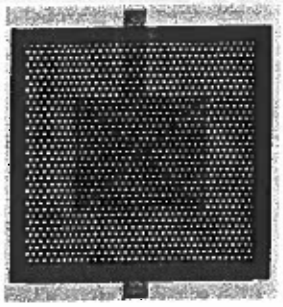
When g_{m3}, g_{m4}, and g_1 are positive this is a positive real matrix (being the sum of a diagonal matrix with non-negative entries and a skew-symmetric matrix). The reader may be interested in constructing the P and Q matrices which go from (38c) to (38d).

In many cases the transfer functions are not driving point ones but transfer admittances or voltage out versus voltage in. Such cases can all be transformed to the transfer admittance form so we first consider that via Fig. 22. For the case of Fig. 22 we have

$$i = \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} -i_c = -C_L \dfrac{dv_c}{dt} \\ 0 \\ I_{in} = \text{dont\_care} \\ -I_{out} = y \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} v_1 = v_c \\ v_2 = v_r \\ v_3 = v_{in} = u \\ v_4 = 0 \end{bmatrix} \quad (39)$$

We see that there are a number of entries with values that are of no importance, that is about which we don't care, at least in the formal synthesis view point. Thus the whole last column and the whole third row of the admittance matrix are immaterial and can be used to obtain properties of interest, such as skew symmetry. Using X for don't care entries we identify a semistate realization with

$$Y_{\text{nodal}} = \begin{bmatrix} -PAQ & -gPB & X \\ X & X & X \\ gCQ & 0 & X \end{bmatrix} \quad (40)$$



After inserting any desirable entries (for example 0) in the don't care positions and a desirable choice of P, Q, and g, a synthesis of this nodal admittance yields the required transfer function matrix, $y = I_{out} = -y_{21}xv_{in}$.

In the case where the input is a current and/or the output is a voltage, we use a gyrator equivalent to convert to the design via y_{21}. For example, for voltage to voltage the structure is as shown in Fig. 23.

The design of nonlinear circuits for VLSI can conveniently begin by conversion to semistate equations and realization of the derivatives through the currents flowing in capacitors, as for the above linear circuits. Conveniently, this can be setup via PSpice using the *G*value components to simulate the mathematical equations. Since the *G*value components of PSpice are OTAs for which mathematical functions can be specified, the simulated circuits can realize in the abstract almost any nonlinear semistate equations. Once these simulations give suitable results, scaling into ranges suitable for VLSI can take place followed by the replacement of the *G*value components by OTAs, multipliers, and so forth. Since the van der Pol oscillator is somewhat a universal second order system, we illustrate setting up the equations for it as an example.

Example 8:

Here we consider an extended van der Pol oscillator. We take the semistate equations to be

$$\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} sx = \begin{bmatrix} 0 & \omega_o & 1 \\ -\omega_o & 0 & 0 \\ 0 & 0 & -1 \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ i(x_1) \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} u \qquad (41a)$$

$$y = [0 \quad 1 \quad 0] \qquad (41b)$$

Here $i(x_1)$ is a nonlinear function which in the case of van der Pol is

$$i(x) = e\left(x - \frac{x^3}{3}\right) \qquad (41c)$$

which would be realizable in VLSI by using Kimura multipliers. However other nonlinearities can be easily handled, for example the hysteresis developed above. Figure 24 shows the connections and means for an initial design simulation using Pspice, from which a VLSI realization becomes straightforward by replacement of the *G* and *G*value components by transistorized components readily realized by the OTAs and multipliers given above.

Discussion

Here we have presented some of the basic ideas behind a type of theory for analog VLSI circuit synthesis. Basic to this is the notion of the semistate for circuit descriptions. In essence the semistate encompasses those variables which are most convenient for a first description of a circuit, using KCL, KVL, and the laws of the circuit components (which in the case of analog MOS VLSI are NMOS and PMOS transistors). The description is a most natural generalization of the state variable one since it allows immediately for portions of the circuit that otherwise would need to be eliminated, such as loops of capacitors, or for terms that are outside of the normal state variable description, such as *n*th order differentiators. In order to express the ideas we have used somewhat simple examples but tried to emphasize the design oriented nature of a theory based upon the semistate. In this limited space we have not touched upon many things, such as BiCMOS circuits and subthreshold circuits for both of which one can obtain exponential behavior which is of practical importance for neural networks and electronic watches. Likewise various effects such

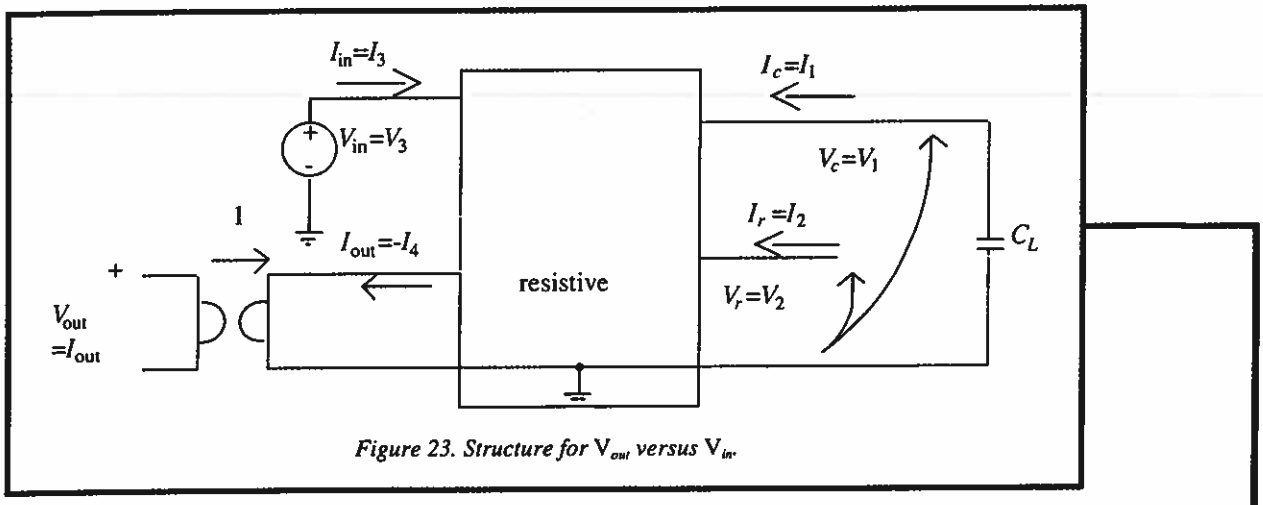


Figure 23. Structure for V_{out} versus V_{in}.

as the body effect have been ignored. In any event the techniques are general and once first order designs are made second order effects can be investigated via good computer simulations with corrections sought.

References

[1] L. A. Zadeh and C . A. Desoer, *Linear Systems Theory, the State Space Approach*. New York: McGraw-Hill, 1963.

[2] S. L. Campbell, C. D. Meyer, Jr., and N. J. Rose, "Applications of the Drazin Inverse to Linear Systems of Differential Equations with Singular Constant Coefficients", *SIAM Journal of Applied Mathematics*, vol. 31, no. 2, pp. 411–425, November 1976.

[3] S. L. Campbell, *Singular Systems of Differential Equations, I* and *II*. New York: Pitman, 1980 and 1982.

[4] F. R. Gantmacher, *The Theory of Matrices*, vol. 2. New York: Chelsea Publishing Co., 1959.

[5] C. W. Gear and L. R. Petzold, "ODE Methods for the Solution of Differential/ Algebraic Systems," *SIAM Journal of Numerical Analysis*, vol. 21, no. 4, pp. 715–728, August 1984.

[6] E. Griepentrog and R. Marz, "Differential Algebraic Equations and Their Numerical Treatment," *Teubner-Texte zur Mathematic*, Band 88, Teubner, Leipzig, 1986.

[7] F. L. Lewis, "A Survey of Linear Singular Systems," *Circuits, Systems, and Signal Processing*, vol. 5, no. 1, pp. 3–36, 1986.

[8] Z. Zhou, M. A. Shayman, and T.-J. Tarn, "Singular Systems: A New Approach in the Time Domain," *IEEE Transactions on Automatic Control*, vol. 32, no. 1, pp. 142–50, January 1987.

[9] D. G. Luenberger, "Non-Linear Descriptor Systems," *Journal of Economic Dynamics and Control*, vol. 1, pp. 212–242, 1979.

[10] R. W. Newcomb, "The Semistate Description of Nonlinear Time-Variable Circuits," *IEEE Transactions on Circuits and Systems*, vol. 28, no. 1, pp. 622–71, January 1981.

[11] B. Dziurla and R. W. Newcomb, "The Drazin Inverse and Semi-State Equations," *Proceedings of the International Symposium on Mathematical Theory of Networks and Systems*, Delft, pp. 283–289, July 1979.

[12] R. W. Newcomb and B. Dziurla, "Some Circuits and Systems Applications of Semistate Theory," *Circuits, Systems, and Signal Processing*, vol. 8, no. 3, pp. 235–260, 1989.

[13] R. W. Newcomb and O. A. Seriki, "Nonlinear-Capacitor Simulation," *Electronics Letters*, vol. 7, pp. 452–454, August 12, 1971.

[14] H. Schichman and D. A. Hodges, "Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Cir-

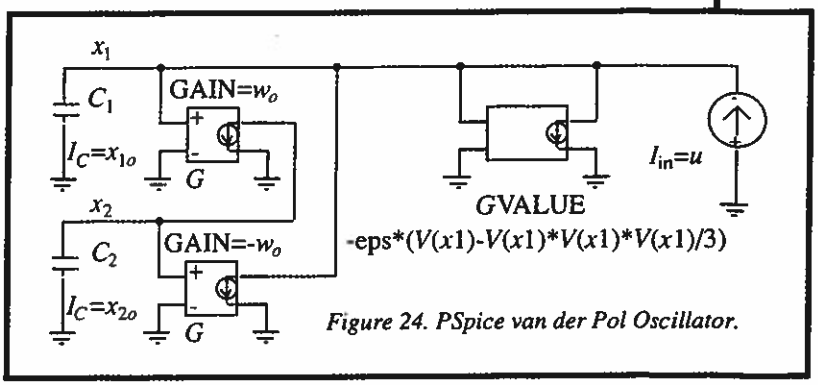


Figure 24. PSpice van der Pol Oscillator.

cuits," *IEEE Journal of Solid-State Circuits*, vol. SC-3, no. 3, pp. 285–289, September 1968.

[15] M. Bialko and R. W. Newcomb, "Generation of All Finite Linear Circuits Using the Integrated DVCCS," *IEEE Transactions on Circuit Theory*, vol. CT-18, no. 11, pp. 733–736, November 1971.

[16] R. L. Geiger. P. E. Allen, and N. R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*. New York: McGraw-Hill Publishing Co., 1990.

[17] D. V. Morozov and A. S. Korotkov, "A Realization of Low-Distortion CMOS Transconductance Amplifier," *IEEE Transactions on Circuits and Systems—I*, vol. 48, no. 9, pp. 1138–1141, September 2001.

[18] A. Motamed, C. Hwang, and M. Ismail, "A Low-Voltage Low-Power Wide-Range CMOS Variable Gain Amplifier," *IEEE Transactions on Circuits and Systems—II*, vol. 45, no. 7, pp. 800–811, July 1998.

[19] K.-C. Kuo and A. Leuciuc, "A Linear MOS Transconductor Using Source Degeneration and Adaptive Biasing," *IEEE Transactions on Circuits and Systems—II*, vol. 48, no. 10, pp. 937–943, October 2001.

[20] J. R. Long, and M. A. Copeland, "The Modeling, Characterization, and Design of Monolithic Inductors for Silicon RF IC's" *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 357–369, March 1997.

[21] C. A. Desoer, "On the Description of Adjoint Networks," *IEEE Transactions on Circuits and Systems*, vol. 22, no. 7, pp. 585–587, July 1975.

[22] B. Peikari, *Fundamentals of Network Analysis and Synthesis*. Englewood Cliffs, New Jersey: Prentice-Hall, 1974.

[23] R. W. Newcomb, *Active Integrated Circuit Synthesis*. Englewood Cliffs, New Jersey: Prentice-Hall, 1968.

[24] K. Kimura, "An MOS Four-Quadrant Analog Multiplier Based on the Multitail Technique Using a Quadritail Cell as a Multiplier Core," *IEEE Transactions on Circuits and Systems—I*, vol. 42, no. 8, pp. 448–454, August 1995.

[25] G. Han and E. Sanchez-Sinencio, "CMOS Transconductance Multipliers: A Tutorial," *IEEE Transactions on Circuits and Systems*, vol. 45, no. 12, pp. 1550–1563, December 1998.

Appendix—From Transfer Function to Semistate

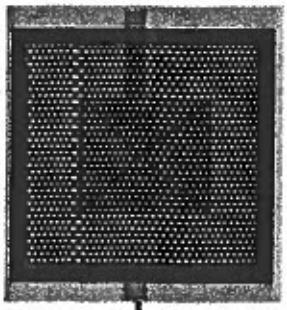
Given a transfer function matrix, $T(s)$, we give a method to get a minimal semistate realization, that is one with the rank of E equal to the degree of the transfer function. For this we follow the technique of [12, p. 243] and make a partial fraction expansion.

$$T(s) = T_\infty(s) + T_o(s) \qquad (42)$$

where $T_\infty(s)$ is the portion at infinity and $T_o(s)$ is zero at infinity, $T_o(\infty) = 0$. Then we move the poles at infinity to zero so that the realization theory for finite poles can be used. Finally, we follow [23, pp. 80–84] to get the two realizations

$$T_o(s) = C_o(sI - A_o)^{-1}B_o \qquad (43a)$$

Angela Hodge-Miller received the B.S.E.E. from the University of Maryland in 1996 and the M.S. in electrical engineering from Stanford University in 1998. She is currently research scientist for the United States Federal Government. She was formerly employed by the National Institute of Standards and Technology, Electronics and Electrical Engineering Laboratory where she researched methods of performing built-in self-tests for multi-technology systems-on-a-chip. She is now employed with the Naval Research Laboratory where her work focuses on developing multi-sensor systems for fluidic characterization. She has held membership in multiple societies including the IEEE, Sigma Xi (The Scientific Research Society), and NSBE.



$$T_\infty(\frac{1}{s}) = D_\infty + C_\infty(sI - E_\infty)^{-1}B_\infty \Longrightarrow T_\infty(s) = D_\infty + C_\infty((\frac{1}{s})I - E_\infty)^{-1}B_\infty \quad (43b)$$

The details are rather messy to give here but in the case of scalar transfer functions A_o and E_∞ can be chosen as companion matrices. This allows the minimal semistate realization

$$\begin{bmatrix} I & 0 & 0 & 0 \\ 0 & E_\infty & I & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} sx = \begin{bmatrix} A_o & 0 & 0 & 0 \\ 0 & I & 0 & 0 \\ 0 & 0 & I & 0 \\ 0 & 0 & 0 & I \end{bmatrix} x + \begin{bmatrix} B_o \\ 0 \\ -B_\infty \\ -D_\infty \end{bmatrix} u \quad (44a)$$

$$y = [C_o \;\; C_\infty \;\; 0 \;\; I]\, x \quad (44b)$$

Example a.1:

Assume that we desire to realize $T(s) = (3s4 + 2s + 1) / (s2 + 5s + 6)$. We first obtain the partial fraction expansion portion at infinity: $T(s) = 3s2 - 15s + 57 + [(193s - 341) / (s2 + 5s + 6)]$; thus,

$$T_\infty(\frac{1}{s}) = 57 + \frac{3 - 15s}{s^2},\; T_o(s) = \frac{193s - 341}{s^2 + 5s + 6},\; D_\infty = 57,\; E_\infty = \begin{bmatrix} 0 & 1 \\ 0 & -1 \end{bmatrix},\; B_\infty = \begin{bmatrix} 0 \\ 1 \end{bmatrix},$$

$$C_\infty = [3 \;\; -15],\; A_o = \begin{bmatrix} 0 & 1 \\ -6 & -5 \end{bmatrix},\; B_o = \begin{bmatrix} 0 \\ 1 \end{bmatrix},\; C_o = [-341 \;\; 193] \quad (45)$$

from which, by (44) we have

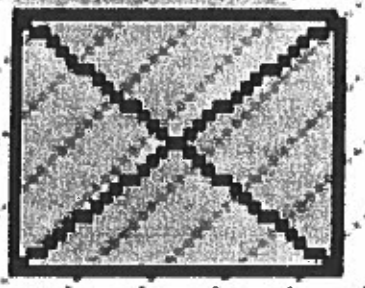
$$\begin{bmatrix} 1 & & & & & & & \\ & 1 & & & & & & \\ & & 0 & 1 & 1 & & & \\ & & 0 & -1 & & 1 & & \\ & & & & 0 & & & \\ & & & & & 0 & & \\ & & & & & & 0 & \\ & & & & & & & 0 \end{bmatrix} sx = \begin{bmatrix} 0 & 1 & & & & & & \\ -6 & -5 & & & & & & \\ & & 1 & & & & & \\ & & & 1 & & & & \\ & & & & 1 & & & \\ & & & & & 1 & & \\ & & & & & & 1 & \\ & & & & & & & 1 \end{bmatrix} x = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 0 \\ -1 \\ -57 \end{bmatrix} u \quad (46a)$$

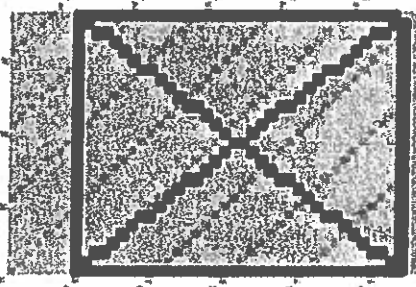
$$y = [-341 \;\; 193 \;\; 3 \;\; -15 \;\; 0 \;\; 0 \;\; 1]x \quad (46b)$$

Robert W. Newcomb received the B.S.E.E. from Purdue University in 1955, the M.S. from Stanford University in 1957, and the Ph.D. from Berkeley in 1960 while on the teaching faculty. He later joined the tenured faculty of Stanford and then the University of Maryland to establish the graduate program in electrical engineering, where he now directs the Microsystems Laboratory devoted to analog, biomedical, and VLSI electronic circuit theory. His research activities can be found listed on the web at http://www.ee.umd.edu/newcomb/mslab.html. These include the semistate theory of circuits, group theory based computers, pulse coded neural networks following the neurophysiological models of D. K. Hartline and a scattering theory for ear type systems following upon the use of Kemp echoes for noninvasive study of the inner ear.

IEEE Circuits and Systems MAGAZINE

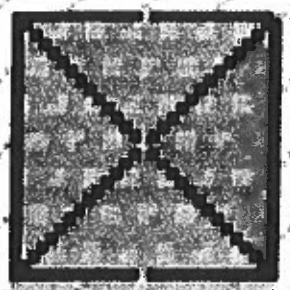
Volume [illegible] 2nd Quarter 2002 ISSN 1531-636X





Semistate Theory and Analog VLSI Design
30

Microelectromechanical Systems and System-on-Chip Connectivity
4



IEEE