

# A Digitally Implementable Ear-Type Lattice

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**Abstract**—The internal auditory system emits slightly detectable sounds (Kemp Echoes) as a response to the auditory input. This response is able to be mimicked via a cascade of two-port lattices and has been previously simulated with analog amplifiers. This paper presents a digital implementation scheme using fixed-point, two's complement arithmetic with the word-length and decimal precision based on generic parameters. The advantages are in accuracy and cancellation of initial cycle oscillations due to initial conditions normally present in both numerical and continuous implementations.

## I. INTRODUCTION

There have been several representations of lattice syntheses. Sellami and Newcomb, in [1], show that a cochlea model, viewed as a transmission line to correlate with the ear's outputted sound (upon an input 'click' or stimulation sound) [2], is best presented as a cascade of 2-port realizations, having degree-one real sections among these, which we give VHDL for in this paper. The corresponding complex degree one, and real degree two lattice however, is derived and implemented in analog current-mode by Moskowitz, Sellami, and Newcomb in [3] and [4].

The circuits in [3] and [4] take advantage of recently developed switched-current (SI) processing by Hughes, Macbeth, and Pattullo, in [5], for delay implementation, and bi-directional current mirrors, by Clark, in [6], for bias control. Some problems with these techniques include clock-feed-through, analyzed by Sheu and Hu in [7], and transistor size-mismatch error. As well, the transistor ratios that control the amplification coefficients can not be adjusted post-fabrication, which is not the case in the digital domain.

The purposes of mimicking the inner ear, aside from robotic application, is to build either a diagnostic device, that can adjust itself to the patient, or to build a more elegant cochlear implant than what commonly exists, [8]. Several applications can be exploited using the cochlear-type system, such as its use in conjunction with inner hair cell systems, as discussed by Rodellar *et al.* in [9].

Our model loosely bases itself on the lattice derived from cochlear fluid mechanics by Sellam and Newcomb, in [8], and is digital, but has more safeguard than analog by using *Design for Reusability* (DfR) and *Design with Reusability* (DwR) proposed by Romdhane, Maddisetti, and Hines in [10]. The functions required for the lattice are addition (positive and negative), multiplication, with an improved design by Sacristan *et al.* from [11], and delay.

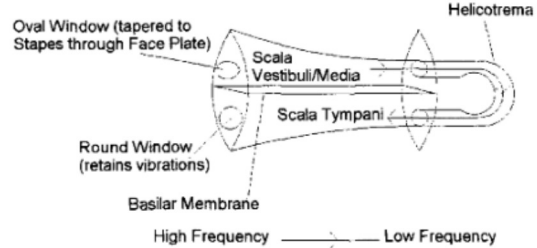


Fig. 1. Cochlea fluid propagation model from [3]. The distance away from the base along the basilar membrane is inversely proportional to the frequency the receptive hair cell at that point is resonant

## II. INNER EAR LATTICE BASICS

From [1], the transfer scattering matrix,  $\theta$ , that relates the left to right port scattering variables of a  $2n$ -port network for an ear type system is:

$$\begin{bmatrix} v_1^i \\ v_1^r \end{bmatrix} = \begin{bmatrix} \theta_{11} & \theta_{12} \\ \theta_{21} & \theta_{22} \end{bmatrix} \begin{bmatrix} v_2^i \\ v_2^r \end{bmatrix} \quad (1)$$

For a degree one complex lattice in standard form, this has

$$\theta(z) = I_2 + \frac{(z-1)}{(1-a^*)(z-a)} xx^{*T} J \quad (2)$$

where

$$I_2 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \quad J = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}, \quad (3)$$

(.)<sup>\*</sup> denotes complex conjugate, and (.)<sup>T</sup>, matrix transpose. The equations in [1] are simplified in [4] to appear as:

$$\theta(z) = I_2 + \frac{(z-1)}{(1-a^*)(z-a)} \frac{|a|^2 - 1}{1 - |a|^2} \begin{bmatrix} 1 & -k \\ -k^* & |k|^2 \end{bmatrix} \begin{matrix} |a| > 1 \\ |a| < 1 \end{matrix} \quad (4)$$

$$\theta_N(z) = \frac{1}{\sqrt{1-kk^*}} \begin{bmatrix} 1 & -k \\ -k^* & 1 \end{bmatrix} \begin{matrix} \begin{bmatrix} f(z) & 0 \\ 0 & 1 \end{bmatrix} |a| > 1 \\ \begin{bmatrix} 1 & 0 \\ 0 & f(z) \end{bmatrix} |a| < 1 \end{matrix} \quad (5)$$

$$\theta_N^{-1}(z) = \begin{matrix} \begin{bmatrix} 1/f(z) & 0 \\ 0 & 1 \end{bmatrix} |a| > 1 \\ \begin{bmatrix} 1 & 0 \\ 0 & 1/f(z) \end{bmatrix} |a| < 1 \end{matrix} \frac{1}{\sqrt{1-kk^*}} \begin{bmatrix} 1 & k \\ k^* & 1 \end{bmatrix} \quad (6)$$

so that:  $\theta(z) = \theta_N(z) \times \theta_N^{-1}(1)$  (7)

where  $a$  is a complex zero of transmission (which can not lie on the unit circle) and

$$f(z) = \frac{1 - a^* z}{z - a} \quad (11)$$

Furthermore, we mention here the rules from [1] to find cross-arm transmittances for the succeeding conjugate section to form an over-all real section, where  $x$  denotes the first section, and  $y$ , the second (also in simplified form from [4]):

$$a_y = a_x^*, k_y = -(v_2^i / v_1^i)^*, \quad (12), (13)$$

$$y = \frac{x^* - \mu^* x}{\sqrt{1 - |\mu|^2}}, x = \sqrt{\frac{|a|^2 - 1}{1 - |k_x|^2}} \begin{bmatrix} 1 \\ -k_x^* \end{bmatrix}, \mu = \frac{x^T J x}{|a|^2 - 1 - j2a_i} \quad (14), (15), (16)$$

### III. SIMPLIFIED IMPLEMENTED LATTICE

For this real implementation, we replace the transfer scattering matrix,  $\theta$ , for the case where  $|a| < 1$ , by  $\theta_M(z)$ , where  $k$  and  $a$  are both real, and we therefore ignore conjugate notation,  $k^*$  and  $a^*$ :

$$\theta_M(z) = \begin{bmatrix} 1 & -k \\ 1-k & 1-k \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & 1/z \end{bmatrix} = \begin{bmatrix} 1 & -k \\ k & z \\ 1-k & z \end{bmatrix} \quad (17)$$

We relate this however to the transfer scattering matrix of (7). First, rephrasing (6) without the constant multiplier gives:

$$\theta_N(z) = \begin{bmatrix} 1 & -kf(z) \\ -k & f(z) \end{bmatrix} \quad (18)$$

Now, surrounding  $\theta_M(z)$  on the left with  $J$  of (2), and on the right with  $K$ , where:

$$K = \begin{bmatrix} 1-k & 0 \\ 0 & \frac{1-az}{1-a/z} \end{bmatrix}, \quad (19)$$

gives:

$$J \times \theta_M(z) \times K = \begin{bmatrix} 1 & -kf(z) \\ -k & \underline{-(1-k)f(z)} \end{bmatrix} \quad (20)$$

where the underlined constant,  $-(1-k)$ , shows the difference in the two lattices, and is apparent between node (3) and node (4) in Fig. 2 (a). Figure 2(b) replaces this  $(1-k)$  with negative unity, which would match (18), and results in a new  $\theta_M(z)$ ,  $\theta_{M'}(z)$ , such that:

$$\theta_{M'}(z) = \begin{bmatrix} 1 & -k \\ 1-k & z \\ 1-k & z \end{bmatrix} \quad (21)$$

$$J \times \theta_{M'}(z) \times K = \begin{bmatrix} 1 & -kf(z) \\ -k & f(z) \end{bmatrix} = \theta_N(z) \quad (22)$$

To help explain the simulation section, we will load the lattice of Fig. 2 in a 1-port, so that we base our results on one input, namely,  $v_1^i$ . For this, we attach a load,  $S_L(z)$ , the load reflection coefficient, between  $v_2^r$  and  $v_2^i$ , such that:

$$v_2^r = v_2^i = S_L(z) \times v_2^r = S_L(z) \times v_2^i \quad (23)$$

Now, substituting (17) and (23) for  $\theta$ , in (1):

$$\begin{bmatrix} v_1^i \\ v_1^r \end{bmatrix} = \begin{bmatrix} 1 & -k \\ k & 1-k \\ 1-k & z \end{bmatrix} \begin{bmatrix} v_2^r \\ S_L(z) \times v_2^r \end{bmatrix} \quad (24)$$

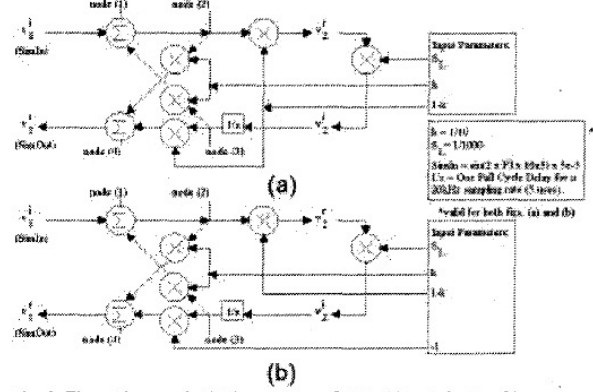


Fig. 2. Flow Diagram for lattice structure  $\theta_M(z)$ , (a) and  $\theta_{M'}(z)$ , (b).

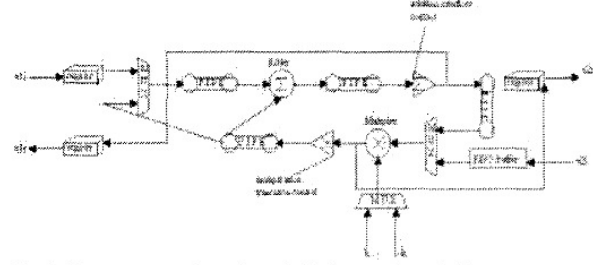


Fig. 3. Binary computation scheme for lattice structure  $\theta_M(z)$ .

$$\text{gives:} \quad \frac{v_1^r}{v_2^r} = \frac{1}{1-k} - kS_L(z) \quad (25)$$

$$\frac{v_1^r}{v_2^r} = \frac{k}{1-k} + \frac{(1-k)S_L(z)}{z} \quad (26)$$

The left reflection,  $v_1^r$ , in terms of the left incident,  $v_1^i$ , is denoted by  $S_I(z)$ , the input reflection coefficient:

$$v_1^r = S_I(z) \times v_1^i \quad (27)$$

$$S_I(z) = \frac{v_1^r}{v_1^i} = \frac{\frac{k}{1-k} + \frac{(1-k)S_L(z)}{z}}{\frac{1}{1-k} - kS_L(z)} \quad (28)$$

Let us substitute  $k = 1/10$ , and  $S_L(z) = 1/1000$  into (28):

$$v_1^r = (0.1 + 8.1007 \times 10^{-4} \times \frac{1}{z}) v_1^i, \quad (29)$$

or in discrete time (as  $1/z$  is the unit delay):

$$v_1^r[n] = 0.1 \times v_1^i[n] + 8.1007 \times 10^{-4} \times v_1^i[n-1], \quad (30)$$

which is how we numerically verify our results. Our test input, SimIn, or  $v_1^i$ , was a 10 kHz, 50  $\mu$ Amp signal, with a system sampling rate of 20 kHz corresponding to a 5  $\mu$ Sec unit delay.

## IV. DIGITAL MODEL

### A. Standard Delay Implementation

Switched current is used in the analog domain. Complementary switches, each working as half delays, form parallel and series full delays to form the poles/zeros, and higher degrees, respectively. Several problems with this technique include transistor mismatch error, clock feed-

through, and the extra half delay required for digitization. Moskowitz, Sellami, and Newcomb have presented a technique to eliminate clock-feed-through [12], but still, these problems, although minimized, are lingering, and although not noticeable in a single filter, they are noticeable in a higher degree cascade.

Digitally, a unit delay is accomplished by introducing a D flip-flop in the signal pathway. An arbitrary number of delays,  $n$ , is made with a FIFO register of length  $n$ . A variable valued delay can similarly be accomplished with DfR design techniques by parameterizing the length of the register. The product between the sampling period and the register length will give the effective delay endured for a sample. For instance, using a register of length three, will cause three unit delays. One of the advantages of working in the analog domain is that we can represent the standard delay in (10) with a standard filter structure from [5]. Incorporating the delays in the digital domain however is a non-standard digital procedure.

### B. Behavior

Let us interpret (17) to understand each row as a single linear equation, in order to partition our structure into operations, which will make implementation simpler and more organized (Table I). The desired outputs are the reflections, starting with the top row:

$$v_1^i = v_2^i / (1-k) - kv_2^i / z \quad (31)$$

becomes:

$$v_2^i = (v_1^i + kv_2^i / z) (1-k) \quad (32)$$

For the bottom row, we get:

$$v_1^i = v_2^i k / (1-k) + v_2^i (1-k) / z \quad (33)$$

and substituting (32) into this:

$$v_1^i = kv_1^i + (1-k+kk)v_2^i / z \quad (34)$$

Let us now describe the outputs, (32) and (34), in the discrete domain. For (32):

$$v_2^i[n] = (1-k)v_1^i[n] + k(1-k)v_2^i[n-1] \quad (35)$$

For (34):

$$v_1^i[n] = kv_1^i[n] + (1-k+kk)v_2^i[n-1] \quad (36)$$

Equations (32) and (34) are simplified in terms of signal groups, but we would like to obtain similar nodal analysis which is grouped in terms of the constants,  $k$  and  $(1-k)$ . Essentially our analysis is made simpler using graphical rather than mathematical philosophy, which is verified by tracing through the nodes (1-4) in Fig. 2(a). We calculate the respective nodal signal values, with  $n$  as node abbreviation:

$$n1 = v_1^i[n] + kv_2^i[n-1] \quad (37)$$

$$v_2^i[n] = n2(1-k) = n1(1-k) = (1-k)(v_1^i[n] + kv_2^i[n-1]) \quad (38)$$

$$n3 = (1-k)v_2^i[n-1] \quad (39)$$

$$v_1^i[n] = n4 = k \times n2 + (1-k) \times n3 = k(v_1^i[n] + kv_2^i[n-1]) + (1-k)v_2^i[n-1] \quad (40)$$

The advantage of using (38) and (40), over (35) and (36) is the reduction of the required parameters from three to two. Essentially, we eliminate the need for  $(1-k+kk)$  in (36). Now we can break the calculation procedure into two stages: addition and multiplication. However, to save space, we use one multiplier and one adder to correlate with Fig. 2(a) and equations (38) and (40).

Figure 3, like the lattice, is oriented flowing from left to right. Starting with the multiplier, the result of the multiplication is checked for a possible overflow and then it can be accumulated with a previous corrected multiplication result. The multiplier in [11] multiplies two numbers of  $n$  bits (each one with  $a$  integer bits and  $b$  decimal bits) and the result is a number of  $2n$  bits (with  $2n$  integer bits and  $2b$  decimal bits). We must return to the original format of  $n$  bits however, truncating  $a$  bits on the left and  $b$  bits on the right. The right bits are not problematic, but we must check the left bits, to find if we are eliminating sign or value bits. If they are sign bits, they are easily eliminated, otherwise, binary overflow occurs and a correction is necessary, the result of which will be the bigger positive or the smaller negative number represented by the chosen data format depending on the sign of the  $2n$  bits result.

In the second, addition, stage, correction is carried out in a manner similar to that of multiplication. Only same sign numbers may cause addition overflow, as a standard two's complement property such that the addition of two positively signed numbers will never yield a negative. When the sign of result is different than the operand's sign, this overflow will be corrected in the same way as the multiplier's.

Partitioning (38) and (40) in terms of operations, (38) gives us:

$$Op1 = k \times v_2^i[n-1] \quad (41)$$

$$Op2 = v_1^i[n] + Op1 \quad (42)$$

$$Op3 = (1-k) \times Op2 = v_2^i[n] \quad (43)$$

For equation (40):

$$Op4 = (1-k) \times v_2^i[n-1] \quad (44)$$

$$Op5 = k \times Op2 \quad (45)$$

$$Op6 = Op4 + Op5 = v_1^i[n] \quad (46)$$

An efficient schedule for these is shown in Table I.

TABLE I  
SMART SCHEDULING

Cycle						
Mult.	Op1	Op4		Op5	Op3	
Mult.		Op1	Op4		Op5	Op3
Mult.			Op1	Op4		Op5
Add				Op2		Op6
					Op2	
						Op6

### V. IMPLEMENTATION AND RESULTS

The functional units were previously designed following the ideas of DfR, [10], written in VHDL. They work in fixed-point arithmetic and two's complement. Operand size, delay, precision and constant values are generic parameters. Those

parameters may be particularized in the DwR stage according to the application performance requirements. This technique is advantageous for this type of lattice filter if it were to be used for cochlear applications, which would require adjustment to the ears of different patients.

We used Synopsys 0.6  $\mu\text{m}$  AMS technology for simulation. Table I shows the scheduling arrangement, while Table II shows accuracy and area variations with varying precision specifications.

The most influential parameter, in respect to the frequency, is the sample width. A sample width of 16 bits results in a working frequency of 156.49 MHz. Taking into account that 16 clock cycles are needed to perform all of the operations, we obtain the complete treatment of a sample in 9.78 MHz, instantaneous relative to the cochlear input range of 20 Hz to 20 kHz. In addition to VHDL simulations closely matching numerical simulations, we find that frequency range does not decrease proportionally to width increase, which is a benefit of the multiplier in [11].

Figure 4(a) shows accurate results for the right side's reflection,  $v_2^r$ , and fig. 4(b) does the same for the left side's,  $v_1^l$ . In both cases, the parameters are given in the asterisked text box of Fig. 2.

TABLE II

DESIGN CONSIDERATIONS FROM SIMULATION PARAMETERS				
WIDTH (BITS)	DECIMALS (BITS)	DELAY (SAMPLES)	CHIP AREA ( $\mu^2$ )	FREQUENCY (MHz)
*8	4	1	3099.58	216.00
16	10	1	9119.86	156.49
32	26	1	30429.71	134.77
64	58	1	118507.82	106.15
128	122	1	616240.67	81.23

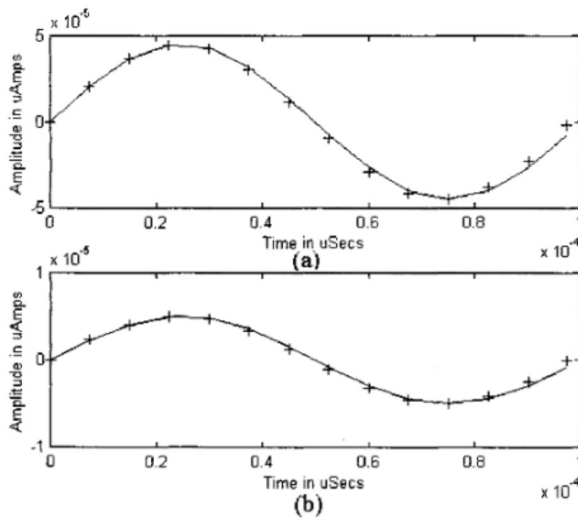


Fig. 4. (a) Right side's reflection,  $v_2^r$ , crosses are VHDL results, strait line is simulation. (b) Left side's reflection,  $v_1^l$ .

## VI. CONCLUSIONS

We have derived reflection and incidence relationships of an ear-type lattice graphically rather than mathematically to build a digital model for a programmable cochlear section. Our design accomplishment is based on the ideas of *Design with and for Reusability* by the authors of [10] and an improved multiplier by in [5]. These are with respect to programmability. With respect to cochlear fluid dynamics, our work is based on [1]. Even though more spacious, the digital circuit is more accurate than the analog model and therefore has a higher error threshold. A cascade of the design shown with the equations (2) and (19) are the first steps towards building an accurate external diagnostic or actuating device for those with inner-ear ailments.

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