An Adjustable CMOS Load Line for Nonlinear Circuits

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Abstract: **A five transistor nonlinear load line is presented for use in analog CMOS circuit design. The load line can be adjusted, possibly dynamically, by an external voltage to fit the situation. In this paper the load-line circuit is presented along with design equations and an example of its use in the realization of a neural type cell. Other uses are in relaxation oscillator and chaos generator design.**

1. Introduction

In active analog circuits load lines are critical to the behavior of the circuits since they serve to establish the operating points of the transistors [1, p.339]. The standard load lines covered in textbooks have linear current versus voltage characteristics that intersect the voltage axis at the bias supply voltage. But in situations where two or more operating points are needed, such as in relaxation oscillators, linear load lines may not be suitable while in the realization of vlsi analog circuits linear resistors are not the most convenient to fabricate. Consequently, diode connected MOS transistors become of interest but these again may not properly intersect the characteristics of the device being biased. In particular this occurs when we attempt to secure a wide range of operation of the neural type cell (NTC) [2]. For this reason Tsay [3] has introduced a CMOS load line which attains a desirable shape. Here we give design equations for Tsay's load line as well as make it voltage adjustable so that it can be used in situations where dynamic change of the load line is needed.

2. Nature of the Circuit

Figure 1(a) shows the load-line circuit under consideration while Fig 1(b) shows a typical characteristic that can be obtained from it. In Fig. 1(b) the DC i(v) characteristic, I(Vin) versus Vin, are measured in the upper left corner of Fig. 1(a) with the current direction chosen to coincide with that going to the left, into the device for which this is the load. An adjusting voltage can be applied to the lower right transistor Mn6. The left most transistor, Mp3, acts as a diode load while the two upper right and the lower left transistors act to give feedback to make the load line rise and fall in a desirable manner. Figure 2(a) shows sets of load line curves with various transistor W/L ratios, with Wp4 swept over $6um \le Wp4 \le 14um$ (from bottom to top), with each value of Wp4 having three values of Wp5 swept over $6um \le Wp5 \le 14um$ (top to bottom), in 4um steps and for various adjusting voltages, $-4V \le Vadap \le -2.5V$ stepped by 0.5V(from bottom to top) in Fig. 2(b).

3. Analytic Treatment

As seen in Fig. 1(b) there are four regions of interest. Here we develop the equations describing the i(v) curve in these four regions such that they can be used for design of the load line with various properties. However, due to space limitations we will make the development for the adaptive transistor turned off; its effect is already seen in Fig. 2(b). For this the hardest part is determining the boundaries of the regions in terms of the applied voltage. We use the standard MOS transistor equations:

$$Idn = Isp = \qquad \text{(1a,b,c)}$$

$$\beta \begin{cases} 0 & \text{for } |Vgs|-|Vth| \le 0; \text{cutoff} \\ (|Vgs|-|Vth|)^2 & \text{for } 0 \le |Vgs|-|Vth| \le |Vds|; \text{ saturation} \\ 2(|Vgs|-|Vth|)|Vds|-Vds^2 & \text{for } 0 \le |Vds| \le |Vgs|-|Vth|; \text{ Ohmic} \end{cases}$$

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where Idn is the drain current of an n-channel device, Isp is the source current of a p-channel transistor, Vth is the threshold voltage of the transistor and β=KpW/L with W & L the width and length of the channel and Kp the Spice gain parameter. Equation (1) is set up to hold for either an n or a p channel device for which n or p will be appended as subscripts when needed. By observing that Idn5=Isp5, Vgp4=Vdp5=Vdn5=Vgn5, Vdp3=Vgp3=Vdp4=Vgp5=Vin we can calculate the state of each transistor (cutoff, saturated, or Ohmic). The calculations are somewhat extensive so the results only are summarized here. First we note that Mp3 is in saturation for all Vin≤Vdd-|Vthp| and otherwise turned off. So we can calculate the states of the other transistors and add Isp3 to the resulting current. We also assume that Vin is limited to the range of Vss≤Vin≤Vdd. The current I is that flowing into the top of Vin and is Isp3+Isp4.

I. ViI=Vdd-|Vthp|≤Vin≤Vdd → Mn5, Mp3 & Mp5 cutoff, Mp4 Ohmic

Assuming Vinternal varies linearly with Vin(from Vss to Vss+Vthn),

$$I = Isp4 = \beta p4(2((1-\frac{Vthn}{|Vthp|})Vdd + \frac{Vthn}{|Vthp|}Vin - Vss - |Vthp|)(Vdd - Vin) - (Vdd - Vin)^2) \quad (2)$$

II. ViII≤Vin≤Vdd-|Vthp| → Mn5, Mp3 & Mp5 saturation, Mp4 Ohmic

The break point ViII is (found by setting Mp4 at Ohmic = saturation)

$$ViII = \frac{Vss + \sqrt{\frac{\beta p5}{\beta n5}}Vdd + Vthn + (1 - \sqrt{\frac{\beta p5}{\beta n5}})|Vthp|}{(1 + \sqrt{\frac{\beta p5}{\beta n5}})} \quad (3)$$

$$I = \beta p3(Vdd-|Vthp| - Vin)^2 + \beta p4(2(-(Vss + Vthn) + (1 - \sqrt{\frac{\beta p5}{\beta n5}})(Vdd-|Vthp|) + \sqrt{\frac{\beta p5}{\beta n5}}Vin)(Vdd - Vin) - (Vdd - Vin)^2) \quad (4)$$

III. ViII≤Vin≤ViII → Mn5, Mp3, Mp4 and Mp5 saturation

The break point ViII is (found by setting Mp5 at saturation = Ohmic)

$$ViII = \frac{Vss + \sqrt{\frac{\beta p5}{\beta n5}}Vdd + Vthn - (1 + \sqrt{\frac{\beta p5}{\beta n5}})|Vthp|}{(1 + \sqrt{\frac{\beta p5}{\beta n5}})} \quad (5)$$

$$I = \beta p3(Vdd-|Vthp| - Vin)^2 + \beta p4(-(Vss + Vthn)(1 - \sqrt{\frac{\beta p5}{\beta n5}})(Vdd-|Vthp|) + \sqrt{\frac{\beta p5}{\beta n5}}Vin)^2 \quad (6)$$

IV. Vss ≤Vin≤ ViIII → Mn5, Mp3 & Mp4 saturation, Mp5 Ohmic

$$I = \beta p3(Vdd-|Vthp| - Vin)^2 + \beta p4(x-|Vhtp|)^2 \quad (7a)$$

where x=Vdd-Vinternal is easily calculated from the quadratic equation

$$(\beta p5 + \beta n5)x^2 - 2[\beta n5(Vdd - Vss - Vthn) + \beta p5(Vdd - Vin-|Vthp|)]x + \beta n5(Vdd - Vss - Vthn)^2 = 0 \quad (7b)$$

The solution using the negative sign for the radical is the one desired (to match at ViIII).

From the region II equations above we can obtain the voltage at the peak, a useful design point, assuming that it is in region II:

$$Vin\_peak = Npeak/Dpeak \quad (8a)$$

$$Npeak = -\beta p3(Vdd-|Vthp|) + \beta p4[Vss + 2\sqrt{\frac{\beta p5}{\beta n5}}Vdd + Vthn + (1 - \sqrt{\frac{\beta p5}{\beta n5}})|Vthp|] \quad (8b)$$

$$Dpeak = -\beta p3 + \beta p4(1 + 2\sqrt{\frac{\beta p5}{\beta n5}}) \quad (8c)$$

Using (8) one can choose transistor W/L ratios to obtain desirable peak points.

4. Discussion

The above equations represent analytic determinations of the i(v) curve of the load line which are useful for design. In terms of actual transistors they give reasonably close answers, as we have checked by numerical evaluation for the transistors in the circuit of Fig. 1. But there are second order effects not taken into account which mean

that Spice runs should be made to incorporate the other effects, such as channel length modulation and channel undercutting. By differentiating the current in Region IV we can also determine the value of Vin needed to obtain the valley, but space limitations preclude its value being given here.

One use for this load line is illustrated in Fig. 3(a) where a voltage variable current hysteresis uses this load line, on the right, to generate neural-type pulses. Figure 3(b)&(c) illustrate that the load line cuts the hysteresis as the hysterisis moves, something which is generally not possible to achieve with a linear load line.

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References

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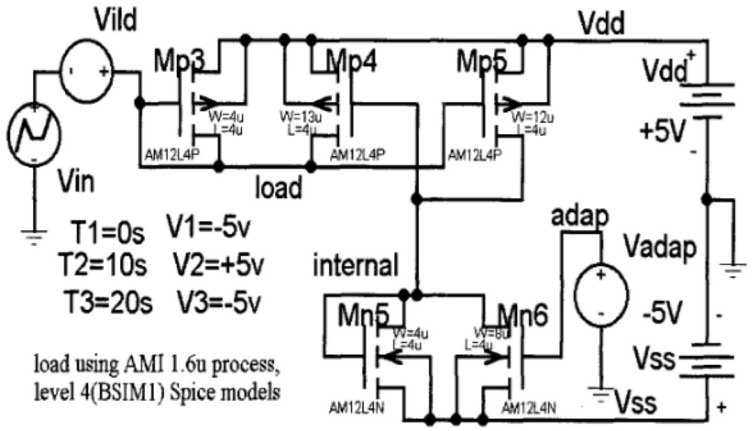

Figure 1(a) The load line circuit

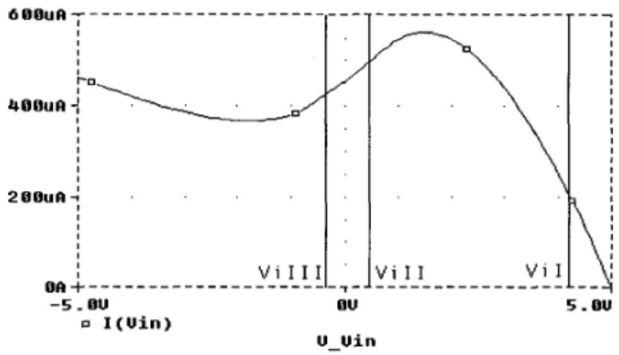

Figure 1(b) I-load versus Vin characteristics, Vadap=-5v

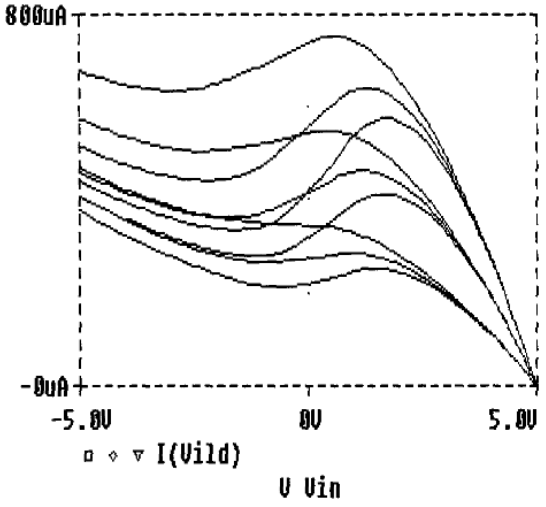

Figure 2(a) Load line with various transistor W/L ratios, Vadap=-5v

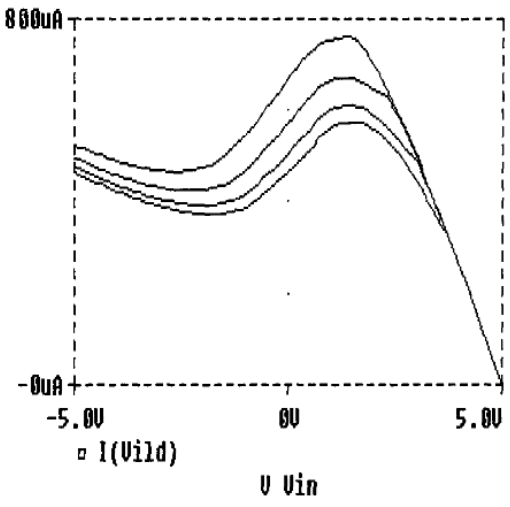

Figure 2(b) Load line with various adjusting voltage, -4.0v≤Vadap≤-2.5v

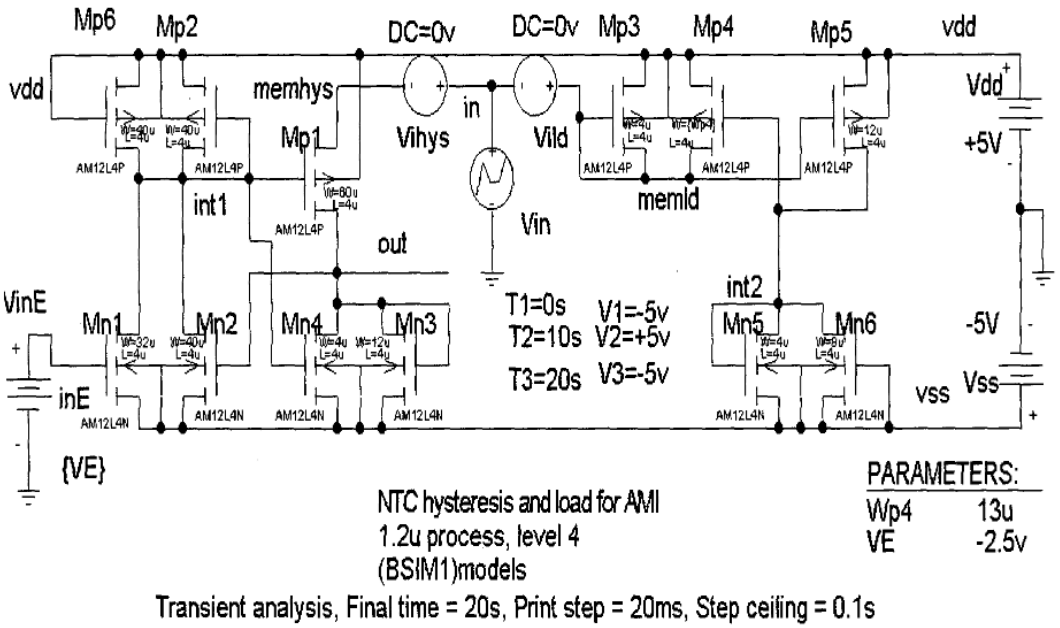

Figure 3(a) NTC circuit