Implementation of Hartline Pools and Neural-Type Cells by VLSI Circuits

Suan-Wei Tsay and Robert W. Newcomb

University of Maryland

Acknowledgements

The authors wish to acknowledge the assistance of and discussions with a number of people including especially D. Hartline, N. El-Leithy, G. Moon, R. Wh. Newcomb, M. de Savigny. G. Wolodkin and M. Zaghloul.

This research was supported in part by ONR Grant No. N00014-90-J-1114 and in part by NSF Grant MIP 89-21122.

1. Introduction

This article treats circuit realizations for the modules of the neural simulation program SYNETSIM created by D. Hartline (Ha2). In particular, discussion is given for VLSI hardware implementation of the chemical pools introduced by Hartline for chemical reactions and of tile Neural-Type Cells introduced by micro-systems researchers for signal transmission via the generation of trains of action potential pulses otherwise realized by table look up in SYNETSIM.

The chemical pools, as introduced by D. Hartline (Hal)(Ha3), are used to model chemical reactions, including enzymes and second messengers, in biological neurons (Be)(HaGr). There are four types of chemical pools introduced by Hartline and all of these have been implemented in electronic circuit form, as we discuss here, according to their describing equations which are based on the phenomenon of the synthesis and degradation of chemical materials. In VLSI realization, the pool itself (chemical material storage) is implemented by a capacitor, while the chemical materials are represented by charges on capacitors. The voltage on a capacitor, that is charge/capacitance, realizes the concentration of the chemical materials.

Repetitive firing modules are used in biological neural networks to transmit signals from one neuron to another. When the membrane potential is higher than a certain threshold value this module fires a train of pulses and in these trains information is transmitted. The primary repetitive firing module used in neurophysiological modeling was described by Hodgkin–Huxley in the 1950's (HoHu). However, the Hodgkin–Huxley equations are so complex that they are too difficult and costly to be realized in hardware. An alternate circuit is used here to avoid implementing the complex Hodgkin–Huxley equations. This alternative is the Neural-Type Cell (NTC) which was introduced in its basic form some time ago to generate neural-type pulses (Ne). The NTC uses hysteresis to generate its pulses when its input voltage is higher than a threshold value. One of the basic properties of the NTC is that its output frequency is a monotonic function of its input voltage.

This article is organized as follows. Section 2 gives an introduction to biological neurons including the chemical pools, transmitters, receptors and the synapses. Section 3 gives the hardware realization of four types of chemical pools, which are used to modulate the conductances of the membrane. Repetitive firing cells are discussed in section 4. Instead of direct implementation of the Hodgkin–Huxley equations which model the firing cells, we implement a neural-type cell which is much simpler and has a similar output form.

2 Generic Biological Neuron

In order to understand the tie of our circuits to biological neurons we review the latter with especial reference to SYNETSIM of D. Hartline (Hal)(Ha2). Although there are hundreds of different kinds of biological neurons and interaction means, each with their own features (Gu, chps. 45-59), we consider only a generic situation which captures most of the features we wish to emphasize. However, SYNETSIM and our resulting circuits can mimic the features of almost any neuron and its interactions.

A generic biological neuron basically consists of three parts: a cell body (soma), an axon and a number of dendrites. The dendrites form synapses with the branches of axons from other neurons. When a signal is transmitted from a neuron to another neuron through a synapse, the pre-synaptic membrane will release neuro-transmitters which can bind to special sites called receptors in the post-synaptic membrane. Once these sites are bound, ion channels may open and ions such as Sodium (Na+) or Potassium (K+) can then flow into or out of the post-

synaptic membrane in turn changing the membrane potential of the cell body of the neuron. When this membrane potential exceeds a threshold voltage, it will trigger a firing mechanism and issue a train of pulses. The axon then transmits these pulses to other neurons through synapses it forms with the dendrites of other neurons. Figure 1 shows the structure of this type of generic biological neuron

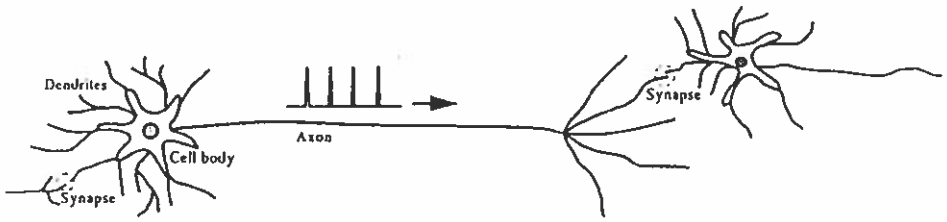


Figure 1. The structure of a biological neuron. The cell body fires a train of pulses when its potential exceeds a threshold voltage. This train of pulses transmits information to other neurons through the axon via synapses.

2.1 Neuron Membrane and Chemical Pools

The membrane potential depends to a large degree on the ionic currents that flow into or out of the membrane. A circuit model for the membrane itself consists of the membrane capacitance, C_M, in parallel with a leakage membrane resistance, R_L. To include the channels through which ions flow we add some parallel connected branches, with each branch constructed as a series connection of a resistor and a dc voltage source (HoHu). Figure 2 shows the circuit model to realize the membrane with ion channels of our generic biological neuron.

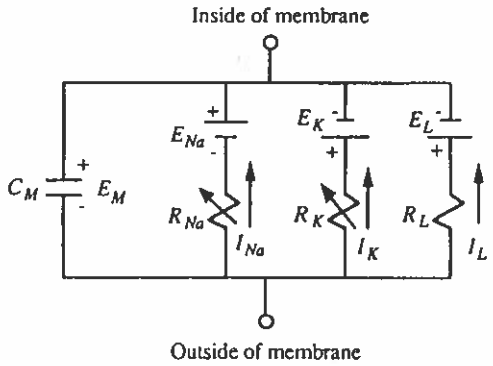


Figure 2. The circuit to realize the membrane of a biological neuron. Na *is for sodium,* K *is for potassium and* L *is for leakage.*

In Figure 2, all the conductance of the resistors are variable with their conductances being modulated by the concentration of chemical materials. In other words, the concentrations of chemical materials control the ionic currents that flow into or out of the cell. Thus, the chemical-electrical interaction is actually the key activity which determines the level of the membrane potential.

2.2. Neuron Synapse

The signal transmitted from one neuron to another is primarily through the axon and synapse receptor interactions. When the axon signal reaches the pre-synaptic membrane, the pre-synaptic membrane releases neurotransmitters and these neurotransmitters can be bound to receptor sites in the post-synaptic membrane, usually in the dendrites. These bound trasmitters then open the ion channels. The ions, such as Na^+ and K^+, can travel through the post-synaptic membrane via these ion channels. The operations between synapse and transmitters can be

demonstrated via Figure 3. In Figure 3, assume there are a total of C receptor sites on the post-synaptic membrane while x of them are bound with transmitters released by the pre-synaptic membrane. Assume the concentration of the transmitters is S and the unbinding rate for a bound transmitter is K. The increasing rate of the bound transmitters is linearly dependent on the concentration of the transmitters and the number of receptor sites which are not bound. The degradation rate, however, depends only on the concentration of bound transmitters by a constant factor K. Accordingly, the dynamic equation for the bound transmitters is

$$\frac{dx}{dt} = S(C - x) - Kx \tag{1}$$

where (C - x) is the number of unbound sites for receptors.

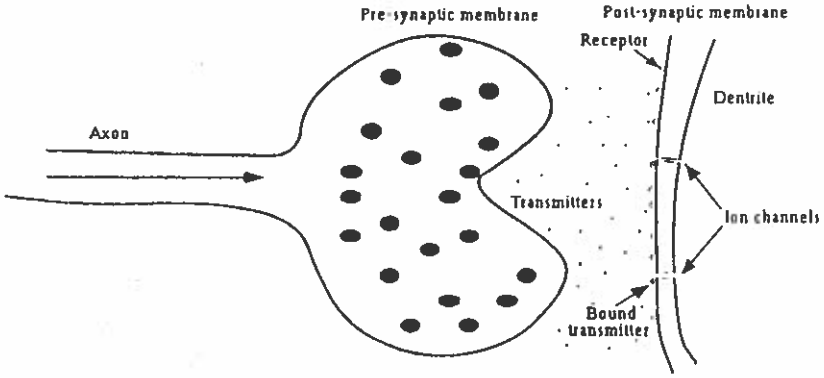


Figure 3. The transmitters and receptors in a synapse. The pre-synaptic membrane releases chemical transmitters. When these transmitters are bound by the receptors on the post-synaptic site, they will open ion channels on the post-synaptic membrane and thus change the membrane potential of the post-synaptic cell.

3 Chemical Pools

3.1 Introduction

The chemical components in a neuron which govern the chemical reactions and properties are modeled by a set of diffusionally connected compartments, called 'pools' in SYNETSIM. Therefore, the circuit realization of chemical pools is essential to the circuit implementation of the chemical reactions in a biological neuron.

According to experimental results from neurophysiology, the chemical pools can be categorized into four groups depending upon their different rules for filling and emptying the chemical material in the pools (Ha1)(Ha2). The pool levels, that is, the concentrations of the

chemical material in chemical pools, of the first two types of chemical pool are conditioned by the transmitter binding on the synapse. The third type has a filling rate proportional to the ionic current with first order decay and the fourth one is similar except that its filling rate is constant. Table 1 shows the pool kinetics for the four types of chemical pools.

Pool types	Describing equations
Pool type 1	$P = C \cdot S/(K_d + S)$
Pool type 2	$dP/dt = [C \cdot S/(K_d + S)] - C' \cdot P$
Pool type 3	$dP/dt = C \cdot I - C' P$
Pool type 4	$dP/dt = F - K \cdot P$

Where P: amount of 'material' in the pool
C & C': constants of proportionality
S: concentration of transmitter
Kd: dissociation constant for transmitter binding
I: ionic current flowing in a specified branch of the electrical branch
F: filling rate
K: rate constant for decay

Table 1. *Pool kinetics. All the constants in the describing equations can be modulated by the pool levels of other pools or by itself.*

The equations of Table 1 are interpreted in the next section.

3.2 Realization of Pools by VLSI Circuits

A goal for neural research is to build a biological-like neural network via VLSI circuits. As a first step towards this goal, we present a feasible way to realize the chemical pools using existing hardware components (TsEN).

As listed in Table 1, the four types of chemical pools are:

Type 1: Bound transmitter pool: The pool level (P/v, v is the pool volume) is proportional to the concentration of bound transmitters at a synapse. Because the pool level of a type one pool is assumed to change rapidly, there is no dynamic part in its describing equation. Its equation is

$$P = C \cdot S/(K_d + S) \tag{2}$$

where $CS/(K_d+S)$ is the concentration of bound transmitters that result as steady state solutions of Equation 1 described in section 2.2 and C is a constant. Because the pool volume v is a constant, it does not show up in the equation and is counted as part of the constant C.

Type 2. Filling rate of the pool material is proportional to bound transmitter: The filling rate is proportional to the bound transmitter at a synapse while its decay rate is linearly dependent on its own pool level. The chemical material in the pool can also 'diffuse to' or 'come from' other pools which phenomenon we represent by the inter-pool diffusion term I_{DT}.

$$dP/dt = C \cdot S/(K_d + S) - C' \cdot P + I_{DT} \tag{3}$$

where C and C' are constants and P is the amount of pool material.

Type 3: Filling rate of the pool material is proportional to ionic current: In this type of pool, the filling rate of pool material is linearly proportional to the ionic current which flows through a specific ion channel and its decay rate is also linearly dependent on the concentration of itself as for type 2. The inter-pool diffusion term also applies in which case the full describing equation is

$$dP/dt = C \cdot I - C' P + I_{DT} \tag{4}$$

where I represents ionic current and C & C' are constants.

Type 4: Filling rate of pool material is constant: This type of pool is the same as type 3 except that its filling rate is constant. Its describing Equation is shown as 5 and again F and K are constants, and pool volume does not show up because it has been counted as part of the constants.

$$\frac{dP}{dt} = F - K \cdot P + I_{DT} \tag{5}$$

The inter-pool diffusion term, I_{DT}, in Equations 3 to 5 describes the phenomenon that the chemical material can diffuse from one pool to another via a resistive path. The describing equation for inter-pool diffusion from the j^{th} pool into the k^{th} pool is

$$I_{DT} = \sum_{j \neq k} (K_{k,j}) \frac{P_j}{v_j} - \left(\sum_{j \neq k} K_{j,k} \right) \frac{P_k}{v_k} \tag{6}$$

where v_j is the volume of the j^{th} pool, P_j/vj is the j^{th} pool concentration and K_{ij} are the inter-pool volumetric decay rate constants. In fact, inter-pool diffusion can also take place with type 1 pools, but that is not treated here.

3.2.1 Pools of Types 3 and 4

Pools of types 3 and 4 are discussed together in this section because their describing equations are similar except that the filling of type 4 is constant, as described in Equation 4, while the filling of type 3 is controlled by another signal as seen in Equation 5. To realize these chemical pools by VLSI circuits, we can consider P to be analogous to charge with a pool itself being considered as a capacitor, since it stores the pool material. The volume v of the pool is analogous to the capacitance, in which case the concentration of the pool material P/v will be analogous to the voltage across the capacitor. Then F is a constant, bias, current source and C, C' and K can come from dependent current sources which can be easily modified by the other pools (TsEN). Table 2 shows the analogues between chemical pools and VLSI circuits.

Chemical Pools	Circuits
Pool	Capacitor
P Material in pool	Charges in capacitor
v Volume of pool	Capacitance
P/v Concentration of pool	Voltage across the capacitor
Filling rate	Inward current
Decay rate	Outward current

Table 2. Analogies between chemical pools and circuit realizations.

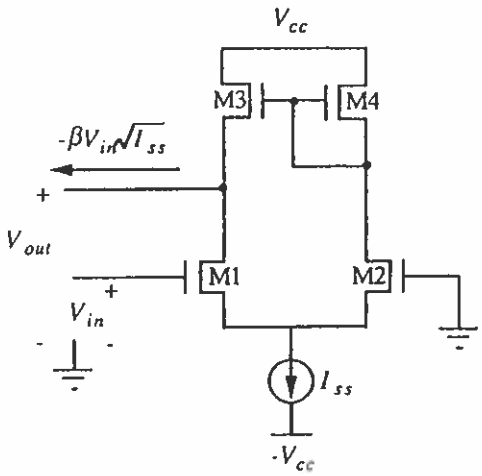


Figure 4 (above). Differential amplifier as an analog multiplier.

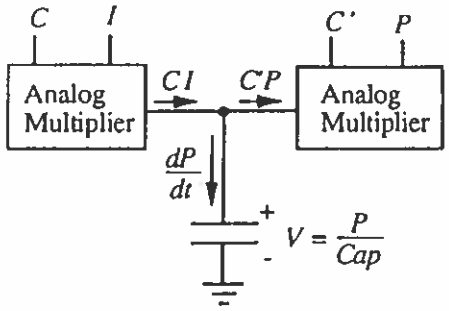
Figure 5 (below). (a) Structure of type 3 pool. (b) Structure of type 4 pool.

According to Equations 4, 5 and Table 2, we can view an isolated pool, that is, without inter-pool diffusion, as a capacitor with some current flowing in (CI for type 3 and F for type 4) and some self-concentration dependent current flowing out ($C'P$ for type 3 and KP for type four). The terms $C'P$ and KP can be formed by differential amplifiers used as multipliers, as shown in Figure 4; the basic structures of pool types 3 and 4 are shown in Figure 5.

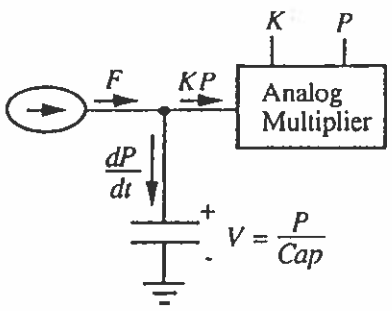
The differential amplifier (GrMe, p.705) in Figure 4, although simple, has two problems when used as an analog multiplier. They are:

(1) The load due to M3 and M4 on the drains of the two transistors M1 and M2 are different.

(2) The output current of the current source M3 can vary considerably due to variations of the output voltage, V_{out}.



(a)



(b)

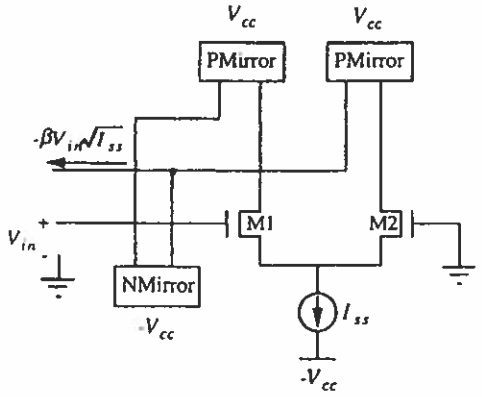


Figure 6. Improved differential amplifier (TsEN, Fig 3)

To remove the first problem, we can add an off-set voltage or change the W/L ratios but these are impractical solutions because the bias current Iss may be desired to be modulated by other pools or it may be different for different pools. Once Iss is changed, the loading problem occurs again. A better method to remove the first problem is to make the loads on the drains of M1 and M2 the same. This leads to the circuit shown in Figure 6.

To see the resulting improvement, in PSPICE simulations of both the original differential amplifier and the improved differential amplifier we made the input voltage, V_{in}, linearly vary from 0V to 1V then back to 0V again. When V_{in} = 0V, the drain currents of M1 and M2 should be equal because their gate-to-source voltages are the same. Figure 7(a) shows that the output of a regular differential amplifier for the circuit in Figure 4 is inaccurate. On the other hand Figure 7(b) shows that this inaccuracy has been improved by the circuit of Figure 6.

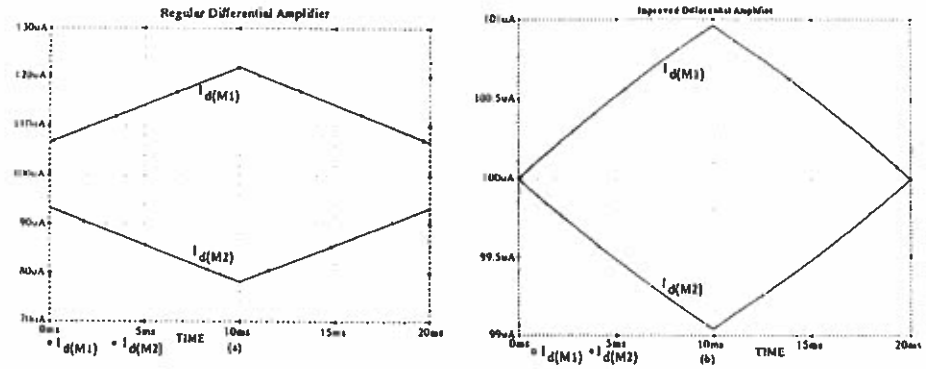


Figure 7. (a) Simulation output for the regular differential amplifier (b) Simulation result for the improved differential amplifier The input voltage is swept from OV to IV and back to OV.

The second problem can be solved by cascoding the regular current minors to increase their output resistance (GrMe, p.712). An example of the implementation of pools type 3 or 4 with triple cascoded current mirrors is shown in Figure 8. The pool level is measured as the voltage across the capacitor and goes to equilibrium when the inward current, *C . I* or *F* in Figure 8, equals the outward current, *C'.P*. Two PSPICE simulations of this pool with initial conditions 0 and 1 Volts for the capacitor voltage are shown in Figure 9. A physical layout for a 2 micron VLSI fabrication of the circuit in Figure 8 is shown in Figure 10 with a 5nf capacitor.

Three triple cascoded current mirrors are as indicated in the layout. Areas B2 and C2 locate the p-type current mirrors and area C1 the n-type one.

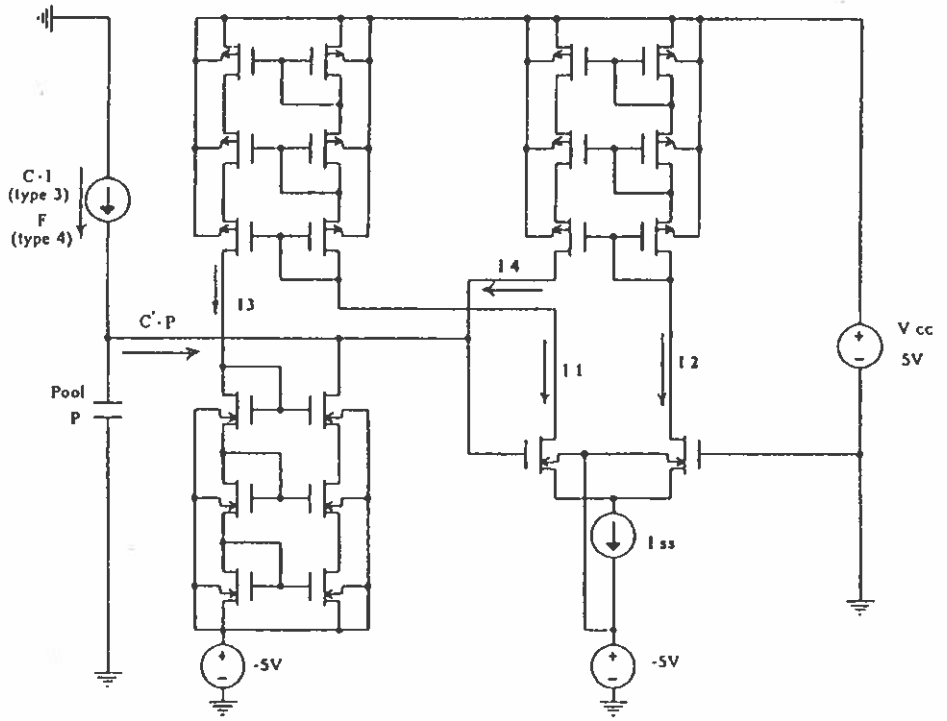
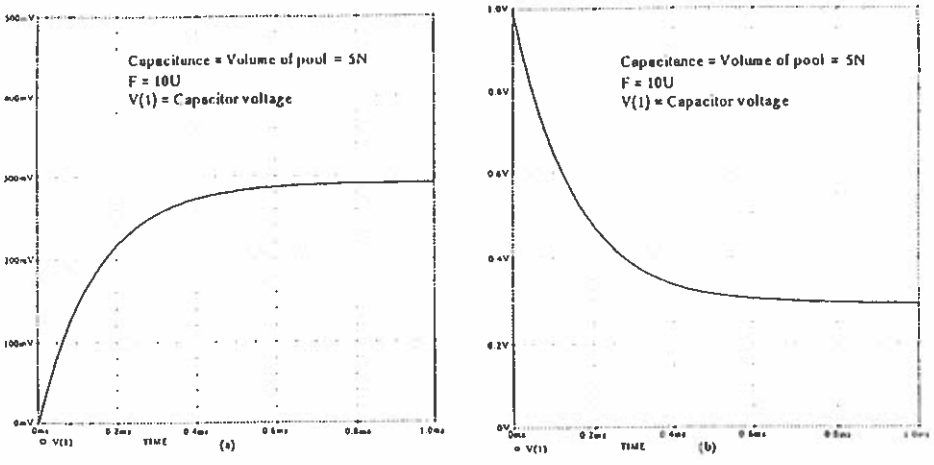


Figure 8 (above). Circuit implementation of type 3 or 4 chemical pools. The inward current is a constant current source for type 4 and is linearly proportional to I for type. All the current mirrors are triple cascaded to increase their output resistances.

Figure 9 (below). (a) Simulation of a type 4 pool with initial condition 0 volt. (b) Simulation of a type 4 pool with initial condition 1 volt.



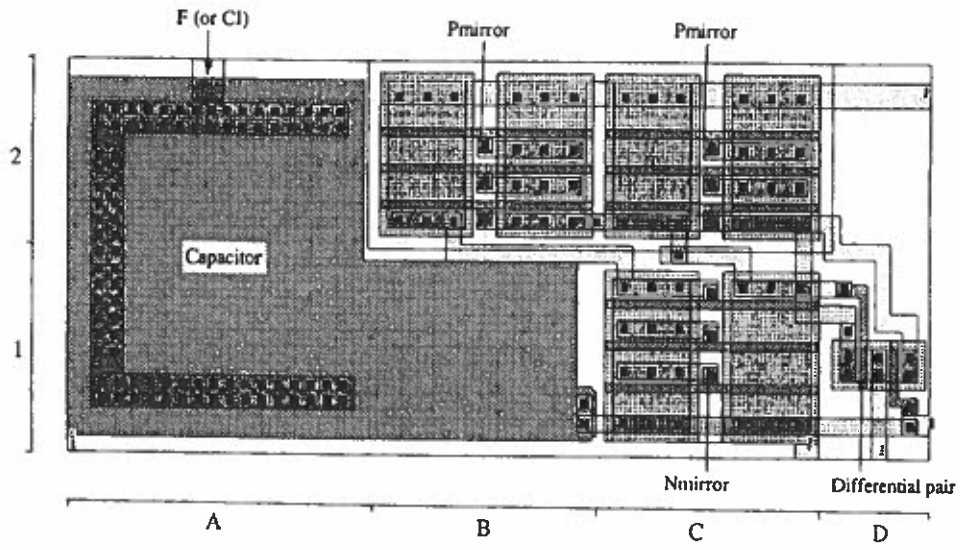


Figure 10. A MAGIC layout for the chemical pool shown in Figure 8. The area of the capacitor is 104μm2 and its capacitance is about 5nf.

3.2.2 Pools of Types 1 and 2

In section 3.1 we mentioned that pools of types 1 and 2 are conditioned by the transmitter binding. Thus, these two types of pools are grouped together and the realization of transmitter binding becomes the key for the implementation of them.

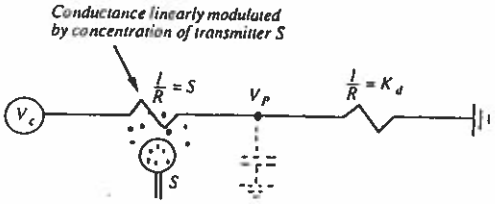


Figure 11. A basic connection of series resistors to realize the bound transmitter expression for pool types 1 and 2.

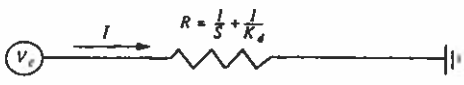


Figure 12. Simplified circuit for Figure 11.

To realize the bound transmitter equation, $CS/(S+K_d)$, it is impractical to multiply C and S and then divide this product by the sum of S and K_d because the circuit will become very complex. Instead series connected resistors with their resistance modulated by external sources can be used to implement the bound transmitter equation using very simple circuit components. The concept is illustrated by Figure 11 where V_c is a voltage source representing the number of receptor sites on the post-synaptic membrane and S represents the concentration of transmitters released by the pre-synaptic membrane.

The conductance of the left resistor is linearly modulated by the concentration of transmitter S and the conductance of the

right resistor is a constant which equals the dissociation constant K_d. Next, Figure 11 can be simplified to Figure 12, where we use an equivalent resistor to replace the two resistors in Figure 11.

As shown in Figure 12, the resistance of the resistor is

$$R = \frac{1}{S} + \frac{1}{K_d} = \frac{(S + K_d)}{SK_d} \tag{7}$$

Thus

$$I = \frac{(V_c - 0)}{R} = \frac{V_c K_d}{(S + K_d)} \tag{8}$$

From Figure 11 and Equation 8 we get the voltage on the middle of this connection as

$$V_p = I\frac{1}{K_d} = \frac{V_c S K_d}{(S + K_d)}\frac{1}{K_d} = \frac{V_c S}{(S + K_d)} \tag{9}$$

which is exactly the bound transmitter equation mentioned above.

Implementation of Pool Type 1

The hardware implementation of pool type 1 is based on the series connected resistors introduced in the previous section, except we replace the variable resistors by MOS resistors with their conductances controlled by their gate voltages. The VLSI circuit for pool type 1 is shown in Figure 13.

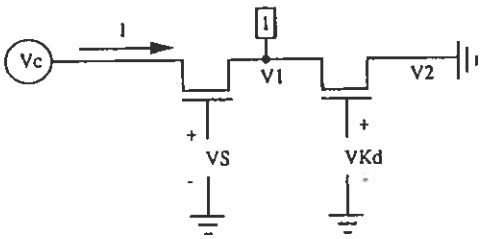


Figure 13. A pool type 1 circuit. Node '1', indicated as the junction point of two transistors in this circuit, represents the level (material concentration) of this pool.

In Figure 13 we assume that the conductances of the MOS resistors are linearly dependent on the gate voltages. That is, the two transistors whose gates are tied to VS and VKd are assumed to be operating in their ohmic region. To verify this assumption we set V_c to be very small (say, 0.1 volt) so that these two transistors are in their ohmic region as long as their effective gate voltages are greater than V_c. Figure 14 shows the PSPICE simulated conductances of the MOS resistors and Figure 15 shows the voltage level (pool concentration) of pool type 1. In both simulations we have added 1 volt to both gate voltages to compensate for the threshold voltage V_T of the MOS transistors. When V_c is not very small compared to VS and VKd, the conductances of these MOS resistors are no longer linearly modulated by their gate voltages because the voltage V1 in Figure 13 is no longer small enough to be omitted compared to VS; thus, the output voltage will not be exact when compared to the desired pool type 1 describing

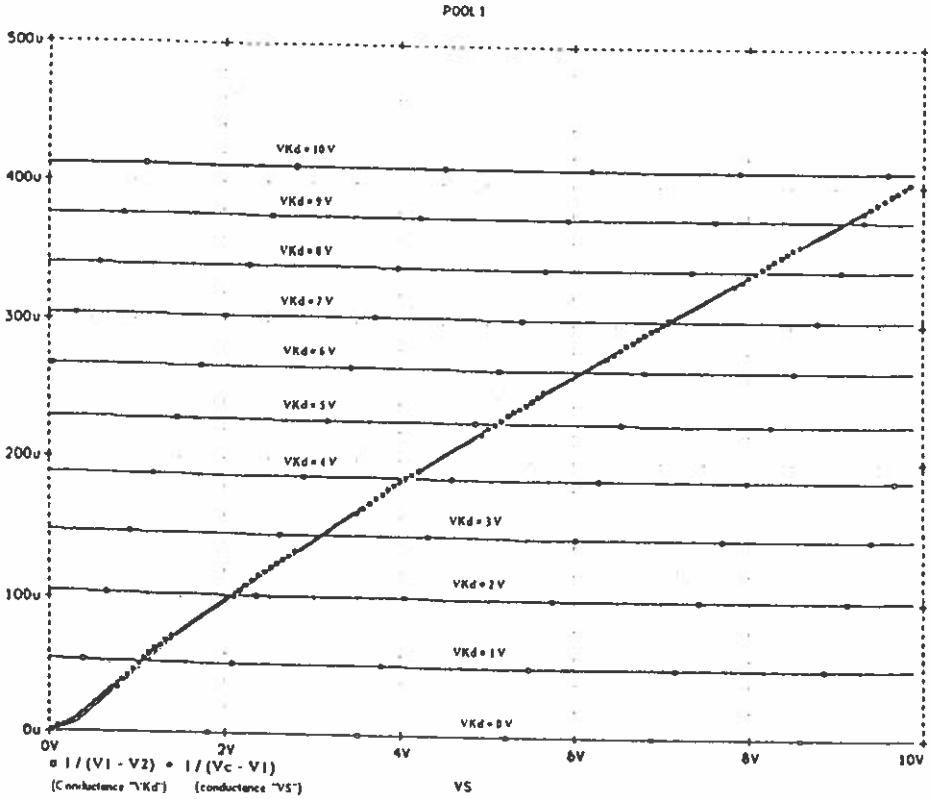


Figure 14. The conductances of the MOS resistors in the pool type 1 circuit. The conductance of the left MOS resistor is linearly dependent on the concentration voltage VS and the conductance of the right MOS resistor is constant as long as VKd is constant.

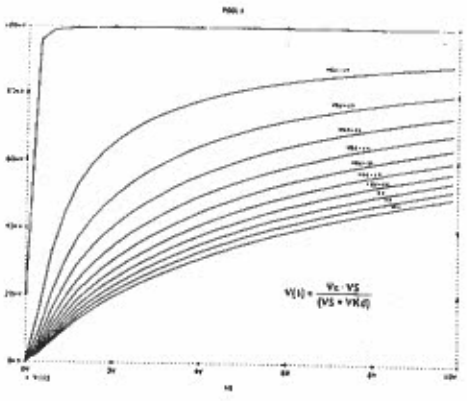


Figure 15. The simulation output of pool type 1. The pool concentration, represented as V(1), is the function of VS and VKd: P = V(1) = V_c VS/(VS + VKd).

For Figure 14 we made V_c equal to 0.1 volt and show the values of VS and VKd to vary from 0 volt to 10 volts. To make the MOS resistors work in the ohmic region, we need VS and VKd to be higher than about 1.1V, where the first 1 volt is that added to VS and VKd to compensate for the threshold voltage. All these assumptions result in the output graphs of Figure 15.

Implementation of Pool Type 2

The describing equation of a type 2 pool is

$$\frac{dP}{dt} = \frac{C \cdot S}{(K_d + S)} - C' P \qquad (10)$$

where S is the concentration of the transmitter in the synapse to which the pool belongs.

According to Equation 10 we can view a type 2 pool as a combination of a type 1 pool and a type 3 pool where the filling current of the type 3 pool is controlled by a type 1 pool. Using this decomposition, the circuit of a type 2 pool is shown in Fig. 16.

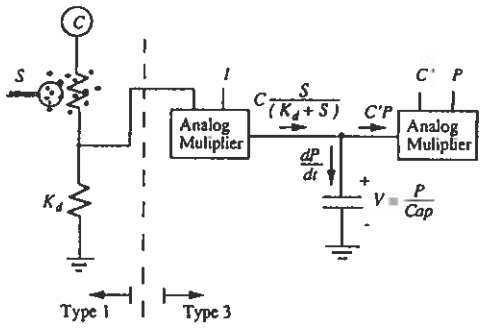
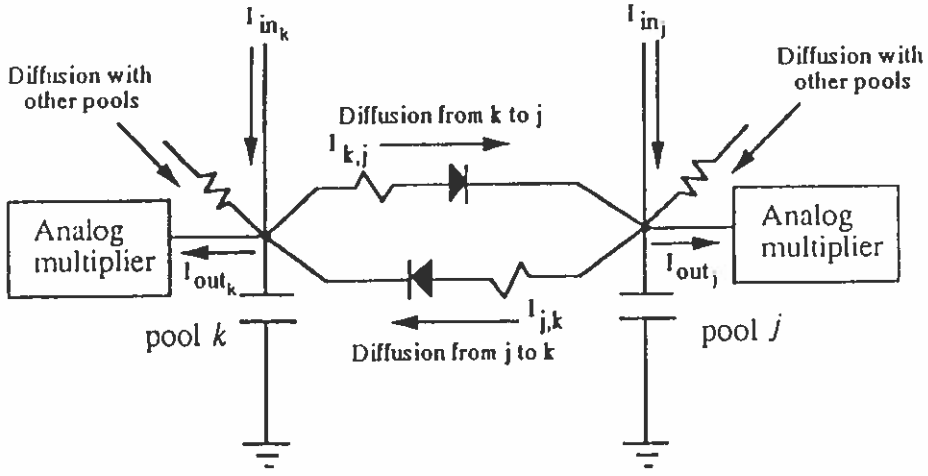


Figure 16 (above). A circuit for pool type 2. Pool type 2 is actually a type 3 pool whose filling current is controlled by the concentration of a type 1 pool.

3.3 Inter-Pool Diffusion

As mentioned in section 3.1, all pools are potentially interconnected by first order diffusion. That is, chemical material in pools can diffuse between pools. This phenomenon is simulated via a diode connected path between two pools. For types 2, 3 and 4 pools, the chemical material diffusing can be realized by charges traveling between capacitors in the diode path between the pools with the diode forward conductance interpreted as the

Figure 17 (below). Inter-pool diffusion between two type 4 pools k and j. The inter-pool diffusion between pools k and j is $I_{DIFF(k,j)} = I_{kj} - I_{jk}$



diffusion rate constant. Because the two directions of flow between two pools could be unequal, two paths are used with different conductances and with diodes to limit the direction of current flow in each path. Figure 17 shows the circuit to realize inter-pool diffusion between two type 4 pools with the same connection holding for types 2 and 3.

4. Neural-Type Cell

4.1 Introduction

A primary means of information transmittal between neurons in a biological neural network is via pulse coding. That is, one neuron will generate a train of pulses which carries the information and sends it to other neurons. Thus, implementation of a pulse generation mechanism is a must if we are trying to realize a biological neuron. The most celebrated analytical treatment of this phenomena is in the set of equations presented by Hodgkin and Huxley to model the oscillation in a neuron (HoHu). Although these H–H equations give results that are very close to experimental results, the H-H equations are so complex that it is extremely difficult to realize them compactly in silicon. And although SYNETSIM does have an H–H module, the time taken to solve the equations makes that module inefficient to use. Consequently, in SYNETSIM a table look up is to generate standard action potentials. But again, use of table look up in silicon is not the most feasible. Consequently, in this section we use a completely different oscillating device, the neural-type cell (NTC), to replace the H–H equations.

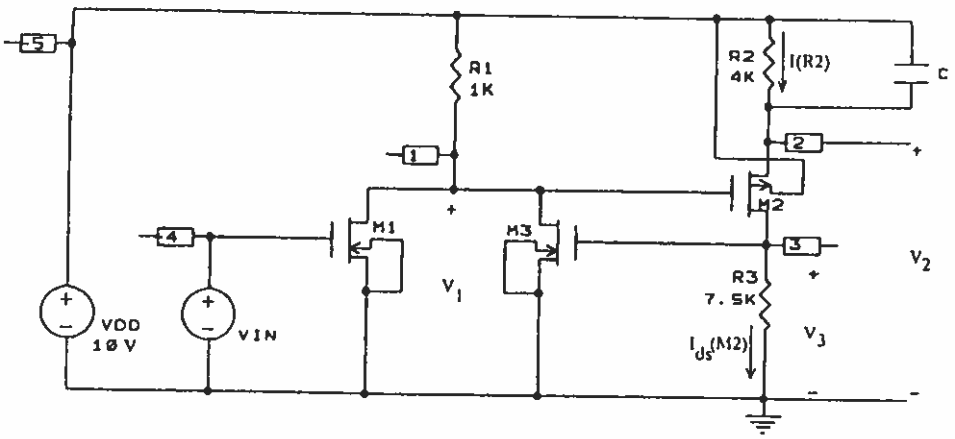


Figure 18. Basic circuit of an NTC (TsSEN, Figure 1).

The neural-type cell is an oscillating device which can be used to mimic the generation of biological spiking signals. Because of the simplicity of its structure, it has been studied through the years, both as to properties and as to circuit realizations (Ne)(KuNe)(El-Ne)(MoZN1,2)(MoZSN)(WoESTN). The original version of the NTC contained resistors which take a big die area when implemented on a chip while also limiting the oscillating range to be very small. The NTC we present here is an improved version that contains no resistors so that its size is dramatically reduced while some simple added circuitry greatly expands its

oscillating range. As we show below (see Figures 19 and 24), the NTC operation rests upon the proper use of hysteresis, something which is known to be important to the operation of neurons in the immune system (HoBBK).

4.2 Basic Circuit

The original basic circuit of an NTC contains a capacitor, three resistors, and three MOS transistors as shown in Fig. 18. The input voltage of the NTC is tied to the gate of Ml and the output voltage is taken at the drain of M2. Feedback is achieved via the connection between the drain of M2 and the gate of M3

4.2.1 Analysis of Hysteresis in NTC

An analysis of how the NTC oscillates is best based upon the hysteresis it contains. The hysteresis of the NTC can be seen in I_{ds} (M2) as a function of V_2; the shape of this hysteresis changes with Vin, which can be considered a parameter in it. To see this hysteresis, we remove the capacitor in Figure 18 and plot the curve of I_{ds} (M2) vs V_2. The current I(R2) vs V_2 is also plotted since this gives the load line on the hysteresis for NTC operation. Both the hysteresis curve for I_{ds} (M2) and the load line for I(R2) vs V_2 of the NTC are shown in Figure 19. One thing to be noted is that the load line (I(R2)) should intersect the hysteresis on the steep edges B and D so that the intercepts are unstable in order that the NTC oscillates; typical oscillations for the conditions of Figure 19 are shown in Figure 20, with portions marked A to D corresponding. If the intersection is not on a steep edge, the NTC's driving point will stay at that intercept and no oscillation will result. Although the load line is fixed, when the input voltage is raised or lowered the hysteresis curve will move left or right and its width will shrink or expand. There exists a range of input voltages over which the two intercepts of hysteresis and load line both stay on the steep edges. This set of input voltages is called the oscillating range of the NTC. For the NTC of Figure 18 with three resistors, the oscillating range is quite limited, being under 1 volt for Vin (SaMEZN). In the next section we show how to expand this oscillating range.

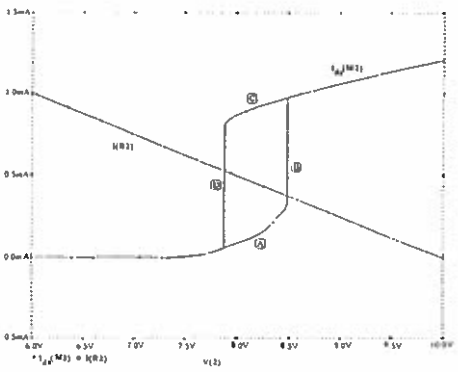


Figure 19. Hysteresis and load line of NTC (TsSEN, Figure 2)

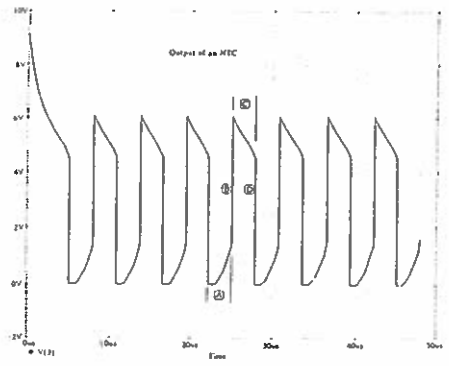


Figure 20. Output of NTC for Vin = 4V (TsSEN, Figure 3)

4.3 All MOS NTC

Two major limitations of the regular NTC are: 1) The three resistors in the NTC take a much bigger chip area than the MOS transistors. The resistances of these resistors are also subject to being changed by different process parameters. 2) There is a limited oscillating range for which the regular NTC oscillates. The reason is, as we mentioned in the previous section, the intercepts of the load line with the hysteresis should be both on the steep edges. When the input voltage, Vin, is changed, the hysteresis in Figure 20 will either grow wider or narrower while also moving to the right or left, according to whether Vin is higher or lower, respectively. That means, once Vin is changed, the intercepts will probably no longer be on the steep edges of the hysteresis.

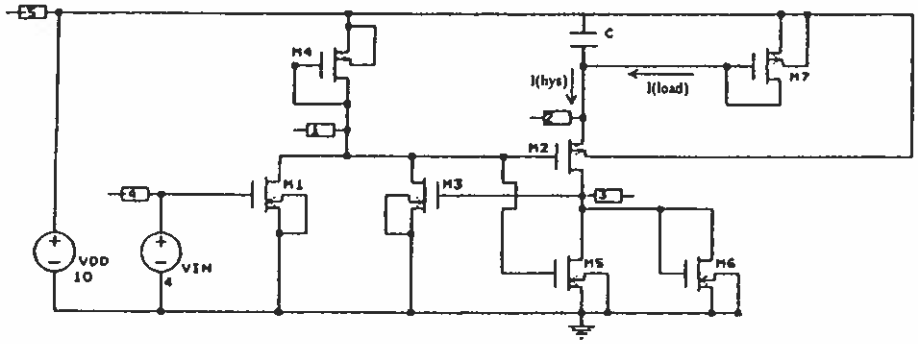


Figure 21. An NTC with its resistors replaced by MOS resistors (TsSEN, Figure 4).

To remove the first limitation, we can replace all the resistors by diode connected MOS transistors (which act as nonlinear resistors) as shown in Figure 21. Carefully choosing the W/L ratios of these MOS transistors will allow the generation of hysteresis with steep edges. This type of NTC, however, is worse in the second limitation because the load MOS resistor is in its saturation mode and it is more difficult to pass both steep edges with a load line of its square law shape. Figure 22 shows a typical situation.

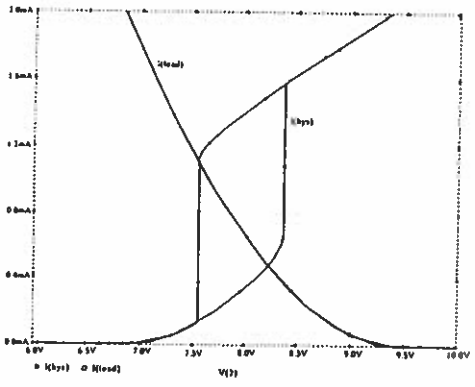


Figure 22. Hysteresis and load line for an NTC with resistors replaced by MOS resistors (TsSEN, Figure 5).

The second limitation can be overcome by shaping the resistor R2 of Figure 18 as a nonlinear resistor generated by a combination of three transistor PM3, PM4 and NM5, as shown in Figure 23. With this special kind of nonlinear resistor, the oscillating range of the NTC is now increased since the load line can be made to pass through the steep edges easily even though the shape of the hysteresis will change with different input voltages, as mentioned above.

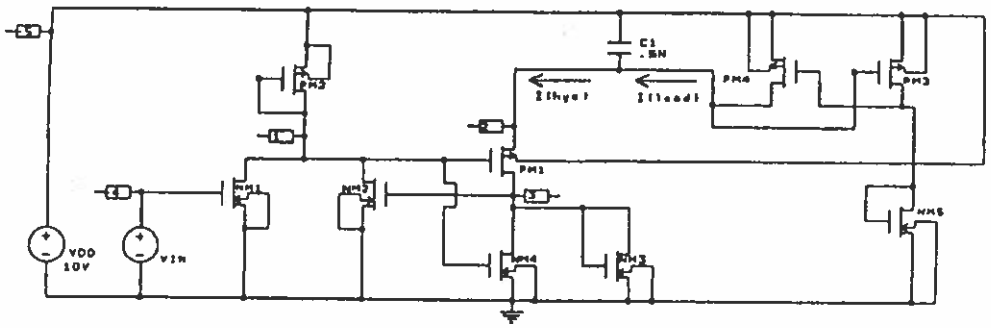


Figure 23. An improved all MOS NTC with nonlinear load (TsSEN, Figure 6).

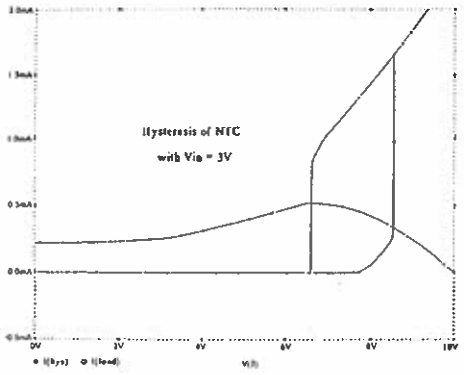


Figure 24(a). Hysteresis and load line of all MOS NTC in Figure 23 with Vin = 3V

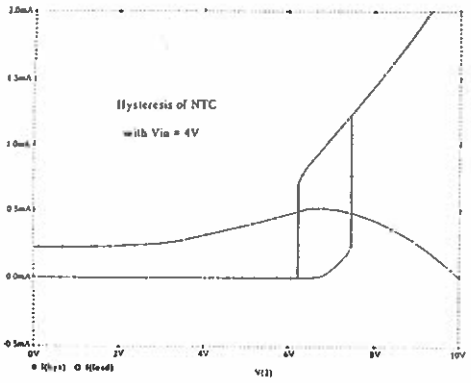


Figure 24(b). Hysteresis and load line of all MOS NTC in Figure 23 with Vin = 4V

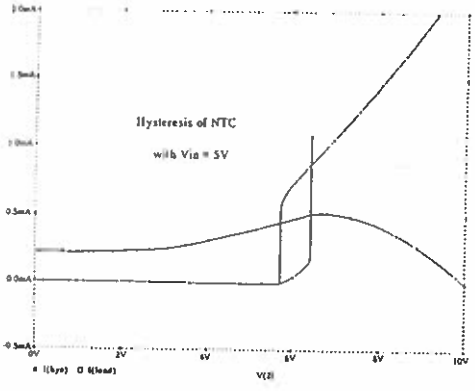


Figure 24(c). Hysteresis and load line of all MOS NTC in Figure 23 with Vin = 5V.

Figures 24(a)(b)(c) show three hysteresis curves for the input voltages being 3, 4 and 5 volts, respectively, along with the new nonlinear load line. As we can see, the hysteresis curve moves left and becomes narrower when the input voltage becomes higher. This will result in an oscillation with higher frequency since it takes less time to switch between the right intercept and the left intercept of the hysteresis and the load line. On the other hand, when the input voltage is lower, the oscillating frequency is lower because of the wider hysteresis curve. Although the frequency to input voltage ratio is highly nonlinear, the frequency is monotonic in the input voltage, as is seen in

Figure 25 where a 0.1 ms ramp of the input voltage between 0 and 10 volts is used and causes oscillations over the range 2.7 volts to 5.9 volts.

Thus all MOS NTC have been fabricated by MOSIS using the double-poly 2 micron technology. Because there is no resistor needed, this NTC occupies a die area of dimension 79μm by $75\mu m$, excluding the capacitor whose size determines the pulse repetition rate of the spike train. The physical layout of the all MOS NTC, made in MAGIC, is shown in Figure 26. In this layout we choose the value of the capacitance to be 5pF which occupies a chip area about $10^4 \mu m^2$.

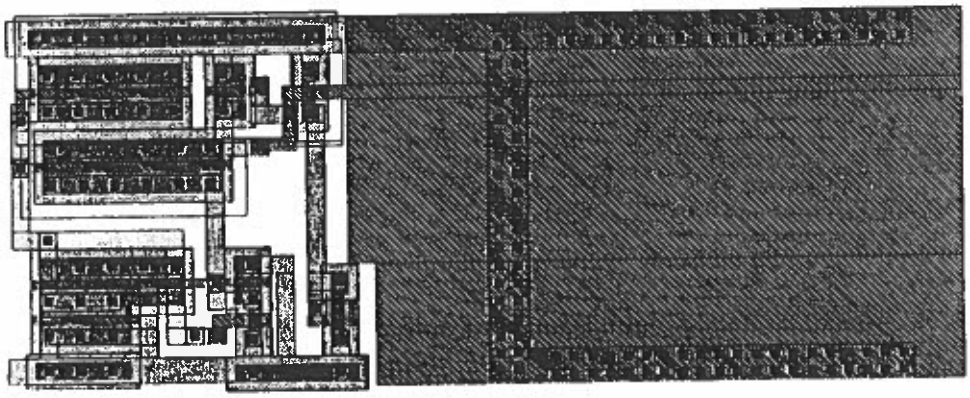


Figure 25. The oscillating range for all MOS NTC (TsSEN, Figure 9)

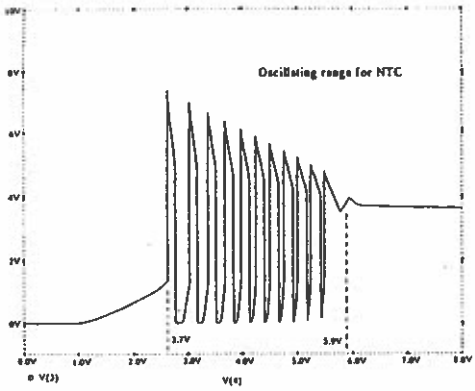


Figure 26. A physical layout for an all MOS NTC via MAGIC (TsSEN, Figure 8).

5 Conclusions

The neurons used in most present-day artificial neural networks (Da)(Ho) are somewhat primitive compared to true biological neurons. As a means to improve the situation, the neural modules of SYNETSIM are taken as the starting point for the ideas of this article. Thus, it presents some circuits which provide possible means to realize in VLSI circuits various properties of the biological neural modules of SYNETSIM. Specifically, two important concepts are covered: the incorporation of second messenger behavior through pools and

Network Models for Control and Processing

Edited by
Martin D. Fraser

Georgia State University

intellect™
Bristol, UK
Portland, OR, USA
2000