# VLSI Floating Resistors for Neural Type Cell Arrays

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## Abstract

Two novel CMOS circuits designs implementing floating resistors are introduced, using the structure of a two-transistor CMOS bilateral linear resistor in the first configuration and two two-transistor CMOS bilateral linear resistors and cascode current mirrors in the second configuration. Linearity is achieved through nonlinearity cancellation via current mirrors over an applied range of ±5V. PSpice simulation results using parameters of MOSIS transistors are presented to verify the theory. These floating resistors can be used for coupling weights in VLSI neural-type cell arrays.

## 1. Introduction

In Artificial Neural Networks (ANNs) [1] the neurons are connected by weights which govern how much of an effect the information from one neuron will have on other neurons. In VLSI implementations of ANNs, the weights can be set by resistor values [2], in which case it is important to have good VLSI floating bilateral resistors. Here we consider resistors to couple neural-type cells [3, 4] and present a suitable class of simple VLSI floating bilateral, voltage tunable resistors which are essentially linear.

At times, standard MOS processes monolithic resistors have been implemented as polysilicon or diffusion strips acting as passive devices. But over the years many authors have developed uni- and bilateral linear floating active resistors containing MOS devices [5]-[16] due to the unpredictable dependence of resistor values on different fabrication process runs and the lack of means to tune these values. Unlike passive resistors, active CMOS resistor implementations usually take less die area and provide controllable resistor values. However, the nonlinearity of the MOSFET prohibits the use of large signals and, therefore, limits the dynamic range. To circumvent these limitations different circuit structures are proposed.

Starting with the architectures of [5] and [6], we expand upon the ideas presented in [17] where we proposed two configurations for a generalized floating active linear bilateral enhancement-mode CMOS resistor. The first configuration is based on the operation of a pair of NMOS and PMOS transistors with the resistance controlled via the gate voltage of either transistor. The second configuration uses current mirrors and

nullators to cancel the nonlinearity. Both resistor configurations are voltage controlled over a wide range and have suitably been fabricated in VLSI. The ideal cases of two configurations are presented in section 2 with circuit realizations and analyses for the floating CMOS bilateral linear resistor configurations shown in section 3. In section 4, PSpice simulations results are included to demonstrate the characteristics of the CMOS resistors.

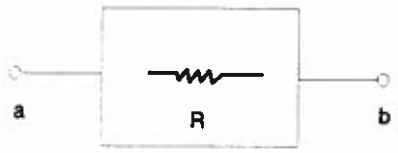


Figure 1: Configuration I of the CMOS bilateral linear floating resistor.

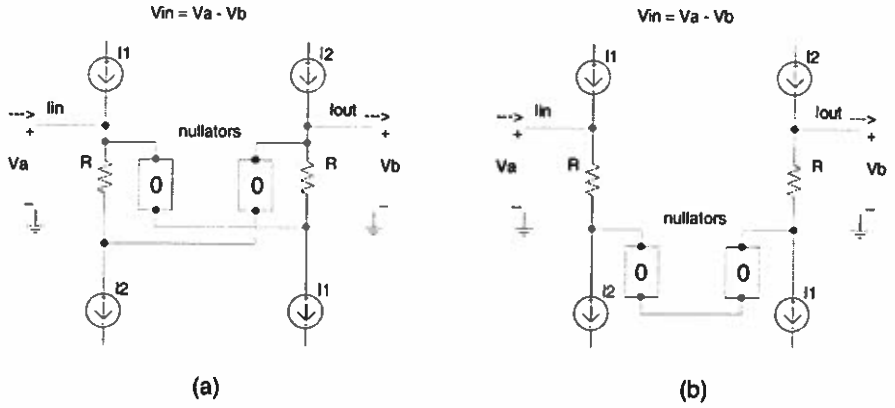


Figure 2: (a) Proposed configuration II of the CMOS bilateral linear floating resistor. (b) Alternate configuration.

## 2. The Ideal Floating Resistor Configurations

The first configuration, shown in Figure 1, is based on [5] and the second one shown in two different forms in Figure 2 follows Rasmussen's architecture [6] for a total of four current sources in a technique similar to that of Singh [7]. In this figure, two nullators are used which are devices that have $I = 0$ and $V = 0$. For configuration II(a) of Figure (2a), realized by the scheme of Figure 3, a pair of NMOS and PMOS current mirrors on one side are employed to mirror the current to the other side by another pair of NMOS and PMOS current mirrors which also allow cancellation of nonlinearities. The current is forced equally through the input and output sides [5] and equal voltages on the current mirrors can generate the nullators. In Figure

(2a) currents $I_1$ and $I_2$ can be written, by virtue of the nullators, as

$$I_1 = \frac{(V_b - V_a)}{R} \tag{1}$$

and

$$I_2 = \frac{(V_a - V_b)}{R} \tag{2}$$

Therefore, the total input current $I_{in}$ can be written as

$$I_{in} = I_2 - I_1 = 2\frac{(V_a - V_b)}{R} = \frac{2}{R}V_{in} = I_{out} \tag{3}$$

For configuration II(b) of Figure (2b), $V_{in} = RI_{out}$ is readily seen.

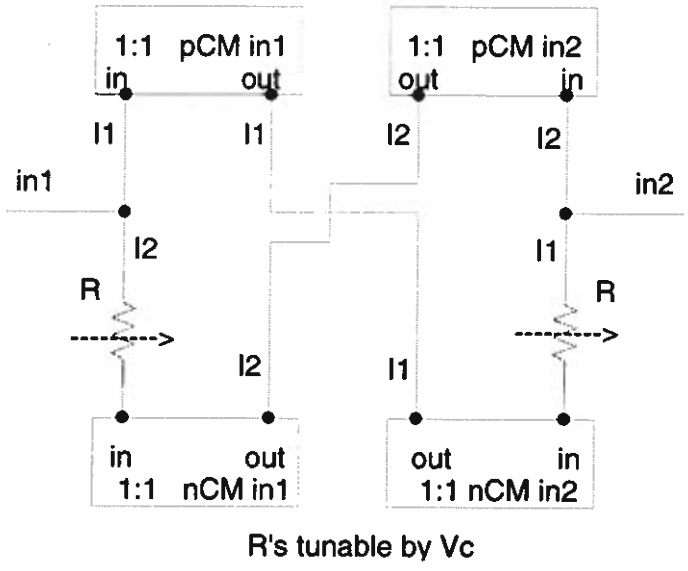


Figure 3: Practical realization of configuration II(a) of the CMOS bilateral linear floating resistor.

## 3. CMOS Realizations and Analyses of the Floating Resistors

Configuration I is realized by Figure 4 and consists of two MOS transistors and two control voltage sources which could be voltage controlled voltage sources (VCVS) for use in ANN weight adaptation. The PMOS transistor $M_1$ is connected to the NMOS transistor $M_2$ to form a floating resistor. The resistance of the circuit is controlled by $V_{cp}$ connected to the gate of the PMOS transistor and by $V_{cn}$ connected to the NMOS transistor, as illustrated in Figure 4. The substrate of the PMOS transistor is connected to $V_{DD}(+5V)$ and

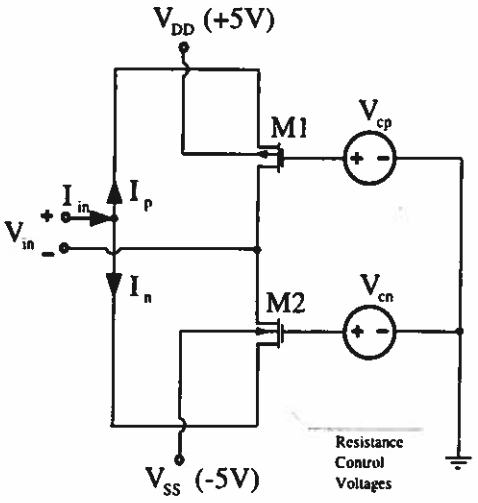


Figure 4: Circuit schematic of the CMOS bilateral linear floating resistor of configuration I.

that of the NMOS transistor is connected to $V_{SS}(-5V)$ in order to back bias the substrate under all loads within the bias source ranges.

Configuration II(a) can be realized with four transistorized cascoded current mirrors as shown in Figure 5. In Figure 3, the first pair consists of NMOS current mirror $nCM_{in1}$ and PMOS current mirror $pCM_{in1}$, on the one side, mirroring the currents $I_1$ and $I_2$ to the other side and similarly for the second pair of current mirrors which consists of NMOS current mirror $nCM_{in2}$ and PMOS current mirror $pCM_{in2}$. This scheme of current mirrors is employed to from the nullators (with equal but opposite voltages) and cancel nonlinearities. The goal is to make the input and output currents the same and equal to the difference of the currents flowing in the PMOS current mirror and the NMOS current mirror at the two sides of the structure. Essentially, this structure of combination of current mirrors with two of the two-transistor CMOS bilateral linear resistors of Figure 4 gives the floating CMOS bilateral linear resistor shown in Figure 3. It should be noted that half of the circuit of Figure 5 is not too different from the CMOS resistor design of Cauwenberghs [15, Figure 3] (although not bidirectional) that employed current mirrors.

The resistor blocks of the circuit schematic of configuration II (Figure 5) are made from blocks of Figure 4 and consist of four MOS transistors and two control voltage sources. The pair of MOS transistors $M_1$ and $M_2$ is connected as the bilateral resistor on the middle left of Figure 5 while the other pair of MOS transistors $M_3$ and $M_4$ is similarly connected to the middle right. These resistors are controlled by the common voltage $V_{cp}$ for the PMOS transistors $M_1$ and $M_3$ and by the voltage $V_{cn}$ for the NMOS transistors $M_2$ and $M_4$ as illustrated in Figure 5. The substrates of all the PMOS transistors are connected to $V_{dd}(+5V)$ and that of all the NMOS transistors are connected to $V_{ss}(-5V)$. In the upper left corner, transistors $M_5$ - $M_8$ form a 1:1 PMOS cascode current mirror $pCM_{in1}$ and in the upper right corner transistors $M_9$ - $M_{12}$ form a 1:1

PMOS cascode current mirror $pCM_{in2}$. Similarly, in the bottom left corner, transistors $M_{13}$ - $M_{16}$ form a 1:1 NMOS cascode current mirror $nCM_{in1}$ and in the bottom right corner, transistors $M_{17}$ - $M_{20}$ form a 1:1 NMOS cascode current mirror $nCM_{in2}$. The cascode current mirrors are used to achieve more linear current matches between the input and output sides of the circuit, with the drawback of restricting the voltage swing on the output voltages. Other types of current mirrors can be used as summarized in [18, pp. 333-353]. It should be noted that the nullators are only indirectly realized in Figure 5. In essence, with good operation of the current mirrors the voltage at the drain of $M_{15}$ with respect to $M_{13}$ is transfered to the drain of $M_{10}$ with respect to $M_{12}$ giving zero volts between the drains of $M_{12}$ and $M_{13}$ for nullator type behavior.

Now we analyze the circuit of Figure 5 for the case of positive input voltage $V_{in}$; the other case results by symmetry. We will assume $V_{cp} < 2V_{th1} < 0$, $V_{cp} < 2V_{th3} < 0$, $0 < 2V_{th2} < V_{cn}$, and $0 < 2V_{th4} < V_{cn}$. As this forces $V_{cp} < V_{th1}$ and $V_{cp} < V_{th3}$ then $M_1$ and $M_3$ are operating in the Ohmic region [5] which guarantees the possibility of linearization. The drain current of $M_{19}$ is mirrored to the drain current of $M_6$ to obtain the two equal $I_1$'s and, similarly, the drain current of $M_{13}$ is mirrored to the drain current of $M_{12}$ due to the equal magnitude of drain currents in $M_{10}$ and $M_{15}$.

## Simulation Results

To verify the analysis, configurations I and II(a) of the floating resistor were simulated with PSpice. The input voltage $V_{in}$ was swept from $-5V$ to $5V$, $V_{cp}$ was held at $-V_{cn} + V_{TOn} + V_{TOp}$, and the total input current $I_{in}$ is plotted in Figures 6, 7 and 8. Figure 6 shows the curves for the two-transistor configuration of Figure 4 with the control voltage $V_{cn}$ as a parameter varied between 0 and 5 in $1V$ steps. Figure 7 shows the curves for the two-transistor configuration for $V_{cn} = 5V$ with channel length $L_2$ of $M_2$ as a parameter varying between $10\mu$ and $110\mu$ in $20\mu$ steps. Figure 8 shows the simulated curves for configuration II(a) realized by the circuit of Figure 5 with the control voltage $V_{cn}$ as a parameter varying between $0V$ and $5V$ in $1V$ steps to compare with Figure 6. Note that in Figures 6 and 8 we get the largest linear range for the resistor for $V_{cn} = 5V$, and as $V_{cn}$ is decreased the linear range also decreases [5]. In Figure 7, we get linear resistors for larger values of $L_2$. The current decreases as $L_2$ increases with the change expected as $1/L_2$ [5]. In all the simulations PSpice MOS level 2 parameters are used following MOSIS data from run N21H of 04/28/93 for which the key parameters are $KP_n$=5.048E-5, $KP_p$=1.908E-5, $V_{T0n}$=0.858, $V_{T0p}$=-0.889, $\lambda_n$=1.844E-2, $\lambda_p$=5.012E-2, $\phi$=0.6, $\gamma_n$=0.198, $\gamma_p$=0.6289. The various transistor channel lengths, $L$, and channel widths, $W$, used in the simulations of Figure 8 are as follows: all lengths are $10\mu$ while the PMOS widths are 2.6 times those of the corresponding NMOS; for all NMOS in the current mirrors, $W = 120\mu$ while for the resistors $W = 10\mu$. For the chosen aspect ratios, as seen from these simulations, configuration I gives a linear resistance in the range of about 8.3K$\Omega$ to 50K$\Omega$ while configuration II(a) gives a linear resistance in

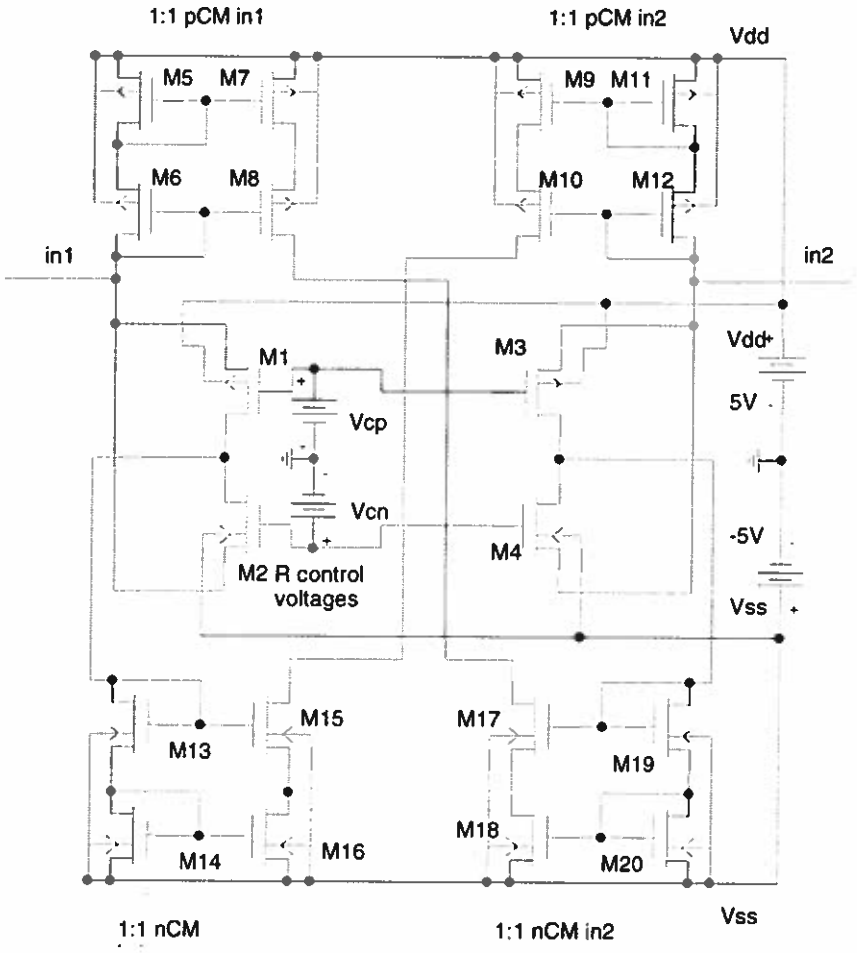


Figure 5: Circuit schematic of the CMOS bilateral linear floating resistor of configuration II(a).

the range of about $4.2\text{K}\Omega$ to $25\text{K}\Omega$.

Note that the circuit for configuration II(b) can be realized by reversing the *in* and *out* terminals of the PMOS current mirrors at the top of Figure 3. This is accomplished by moving the gate-to-drain shorts in Figure 5 from $M_5$, $M_6$, $M_{11}$, $M_{12}$ to $M_7$, $M_8$, $M_9$, $M_{10}$ respectively. PSpice simulation results (which are not included here) on the resulting circuit show that this circuit is not as linear as that of Figure 5. This was discovered thanks due to a reviewer's suggestion that possibly our original results were for Figure (2b) with a ground at the middle of the nullators. Our simulations now show that this is close to the case but without the nullators grounded.

The circuits for configuration I and configuration II(b) of the floating resistor were fabricated using MOSIS CMOS process of n-well $2\mu m$ technology, with the VLSI layouts given in Figure 9 and Figure 10. The aspect ratios chosen were $W_1/L_1 = 10/10$ (for transistor $M_1$) and $W_2/L_2 = 10/90$ (for transistor $M_2$) for configuration I. Those of configuration II(b) are summarized in Table 1.

| Transistor Type | Transistor Number | Length $L$ | Width $W$ |
|---|---|---|---|
| NMOS | $M2$,$M4$,$M13$,$M14$, $M15$,$M16$ $M17$,$M18$,$M19$,$M20$ | $10\mu$ | $10\mu$ |
| PMOS | $M1$,$M3$,$M5$,$M6$, $M7$,$M8$ $M9$,$M10$,$M11$,$M12$ | $10\mu$ | $27\mu$ |

Table 1: Various channel lengths and channel widths chosen for configuration II(b).

## Discussion

In this paper, we have presented two types of linear bilateral CMOS floating resistors for neural-type cell arrays. These resistors are floating versions of the resistors of [5,6,19]. They offer an efficient usage of die area since the area consumed by them is much smaller compared to similarly sized directly implemented polysilicon or diffusion strip based passive resistors. Also, they are voltage controllable over a wide dynamic range. Although these floating resistors were targeted for neural-type cell arrays to enable their use in both excitatory and inhibitory synapses, they can be used in other VLSI applications, such as cellular neural networks (CNNs) [20, 21]. Because the circuits give good large signal resistors, it would be of interest to develop good analytic design formulas, a topic which we point out as a good one for further research.

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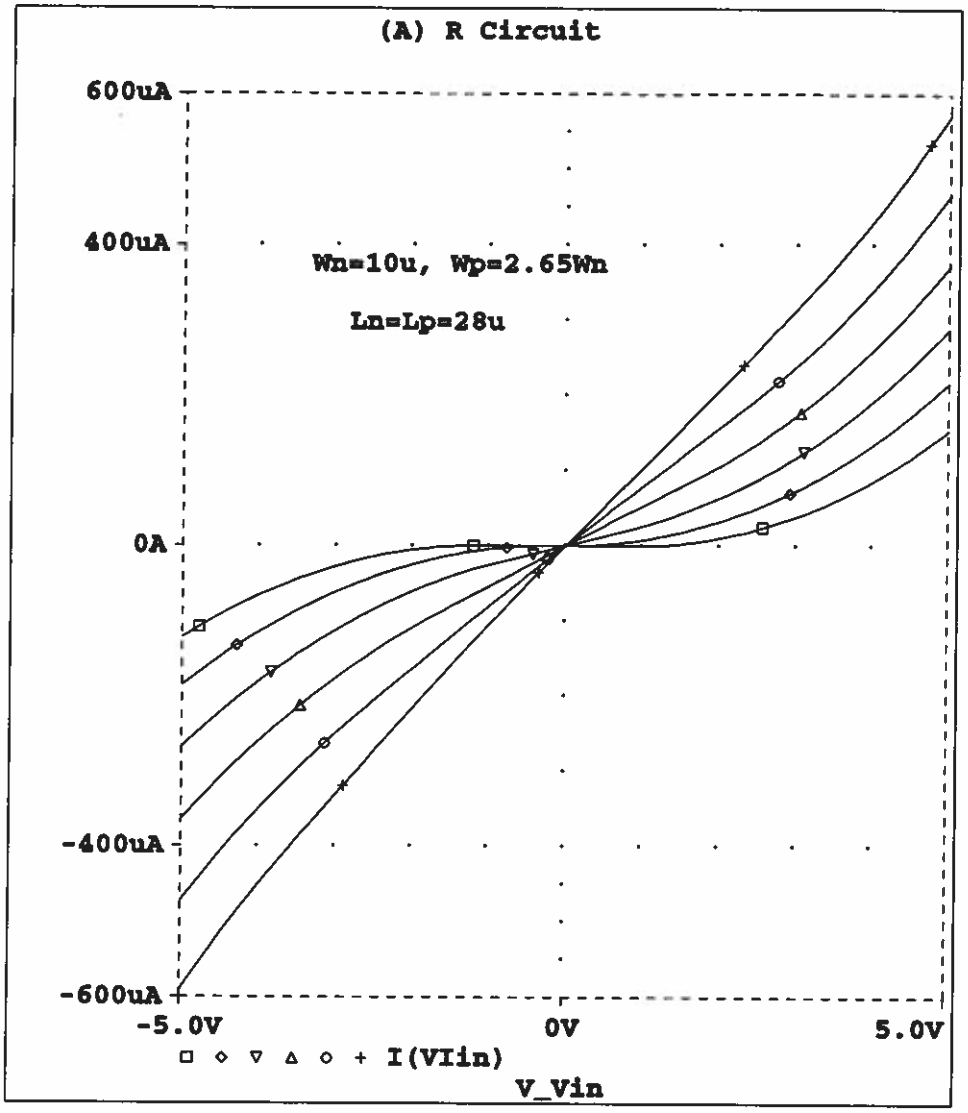


Figure 6: PSpice simulated curves for the two-transistor linear bilateral CMOS floating resistor of configuration I, with the top right curve for $V_{cn}$=5V and decreasing in IV steps to the bottom curve for $V_{cn}$=0V and $V_{cp} \triangleq -V_{cn}$.

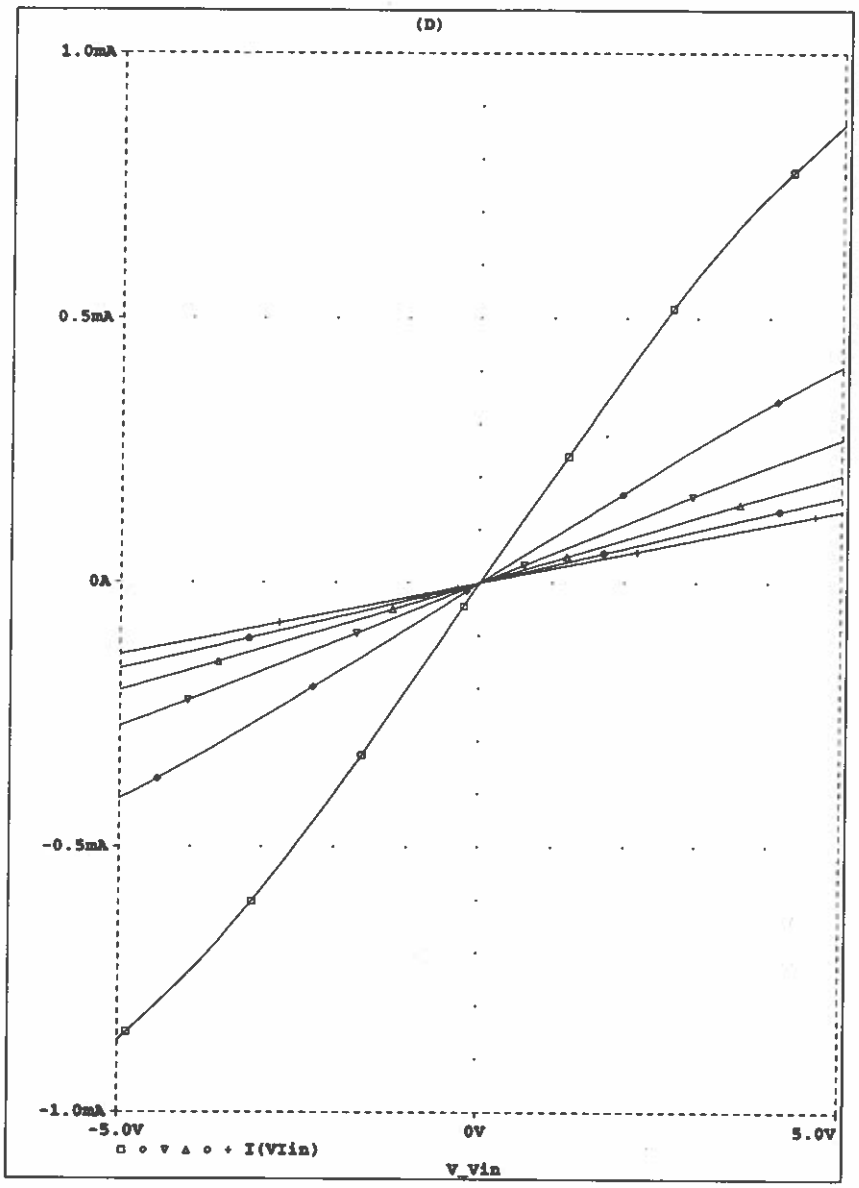


Figure 7: PSpice simulated curves for the two-transistor linear bilateral CMOS floating resistor of configuration I for $V_{cn} = 5\text{V}$ and $V_{cp} \approx -V_{cn}$ , with the top right curve for $L_2 = 10\mu$ and increasing in steps of $20\mu$ to the bottom curve for $L_2 = 110\mu$.

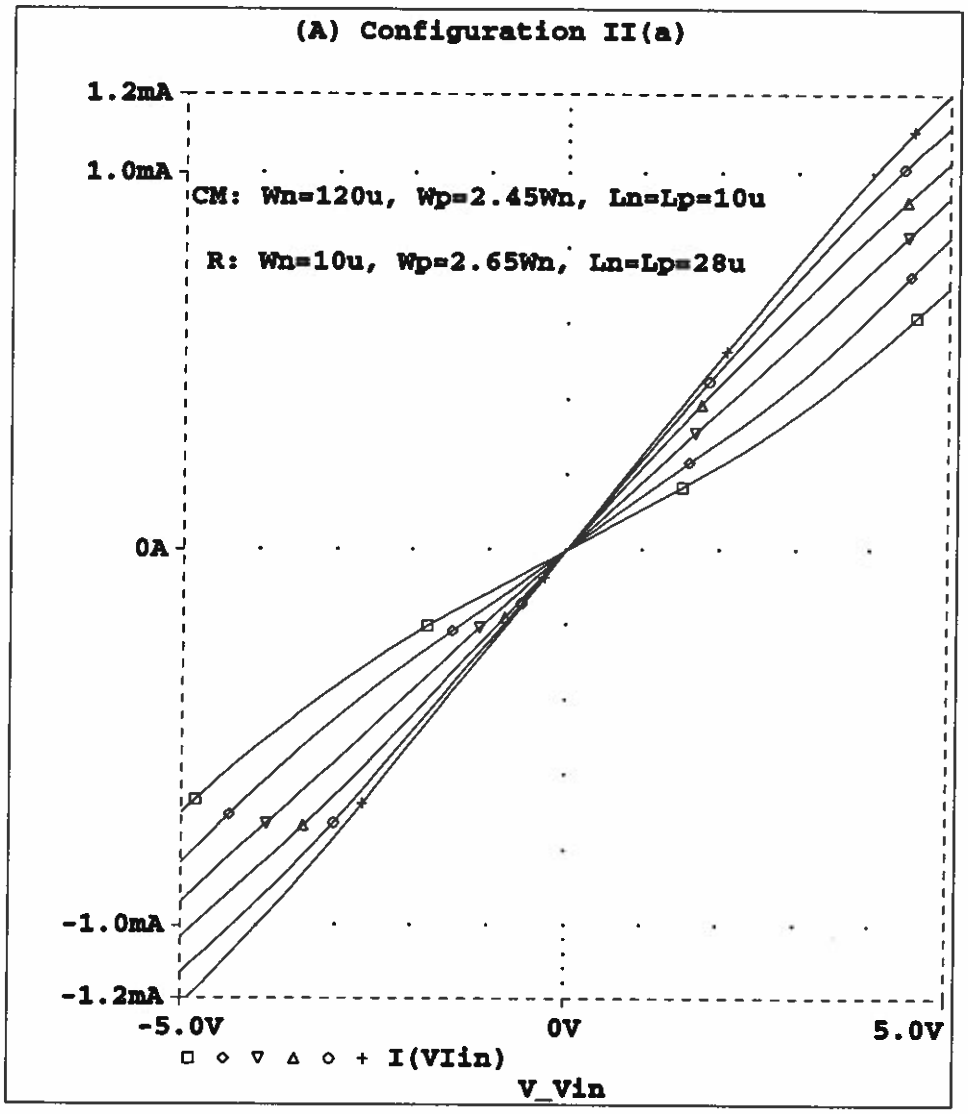


**Figure 8:** PSpice simulated curves for configuration II(a) with the top right curve for $V_{cn}$=5V and decreasing in IV steps to the bottom curve for $V_{cn}$=0V. $V_{cp} \doteq -V_{cn}$.

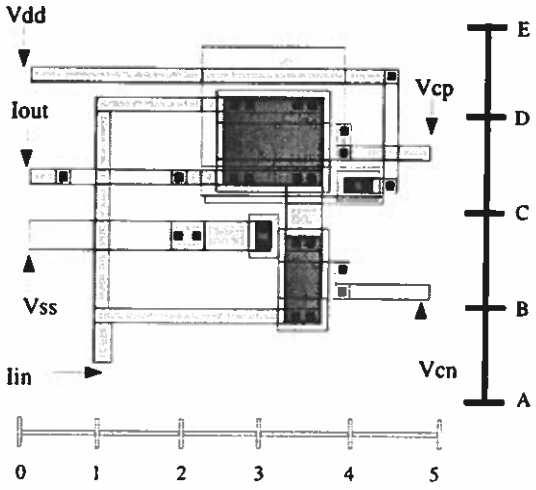


Figure 9: VLSI layout of the CMOS floating resistor of configuration I. The chip is $87\mu m \times 110\mu m$ with horizontal and vertical scales of $18\mu m$ and $30\mu m$ per division respectively.

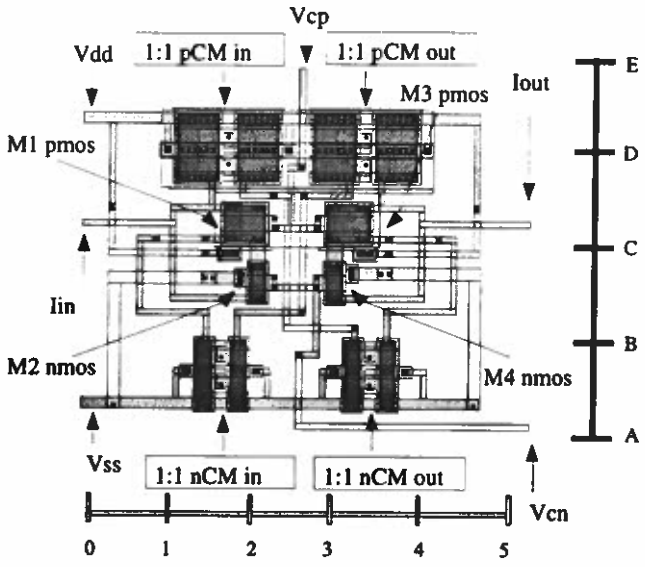


Figure 10: VLSI layout of the CMOS floating resistor of configuration II(b). The chip is $232\mu m \times 288\mu m$ with horizontal and vertical scales of $45\mu m$ and $75\mu m$ per division respectively.