Complementary Clock Feed-Through Reduction for Switched-Current Systems

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Abstract - **A novel method of clock feed through reduction in switched-current circuits is introduced here that outperforms previous methods. In principle, the output of identical circuits with complementary switches are added to cancel out switch based error without the requirement of separate DC and signal distortion cancellation in separate stages. Spice results are shown and compared with analysis and hardware layout. These circuits are useful for digital computation with analog hardware, and with respect to simulation, this circuit has yielded successful results when used in an ear-type network that requires a delay as part of its matrix.**

I. INTRODUCTION

For a good part of this decade, transistor-mode switched current systems have arisen as a cheap and simple form of analog to digital conversion [1], useful especially for current mode systems and biomedical applications with specific relevance to ear type systems [2]. The mechanism of this converter is that a switch controlling input to output amplification connection is periodically pulsated, giving an output that has the original signal alternated with a held, or discrete, value of the signal. A basic problem arising with the technique is the inaccuracy of the signal's held value on the output. Charge buildup on the switch and amplifier causes a differential transfer of the switch control voltage at the switch stage based on the basic capacitance properties of the materials [3]. These inaccuracies are problematic due to their high non-linearity and low-predictability. Previous techniques used for compensation at the receiver end vary from adjusting output widths to lower the significance of the voltage error difference [4,5], splitting the transition area into parts that have their own compensation switches [5], and multiple component optimization [6]. Our approach is to compensate feedthrough by adding the output of two filters that are identical except for the polarity of their inside switches. This technique ultimately reduces design factors and mismatch error due to its conceptual simplicity, although it does require as great a number of transistors as the techniques mentioned above.

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II. THEORETICAL AND PHYSICAL DESIGN ASPECTS

The circuit used here begins with the conceptual structure of [1]. Following through either the top or bottom part of Fig. 1(a), an input, *In(n)*, injected into the central node is added to the previous output, *-(B/A)Out(n-1)*, withheld due to capacitor storage at switch outputs and the non-overlapping nature of the complementary switching system. This is then modified by A to yield the final output, giving the following transfer function:

$$\frac{Out(n)}{In(n)} = \frac{-A}{1 - B \cdot \frac{Out(n-1)}{Out(n)}}. \quad (1)$$

The bias currents cancel out and are not necessary in the block model, but are required for the physical model in order to raise the input to the transistor saturation region: $V_{DS} \geq V_{GS} - V_{t2}$, where

$$V_{GS} = \sqrt{\frac{2I_{in}}{\mu \cdot C_{ox}(W/L)_1}} + V_{t1}. \quad (2)$$

μ denotes electron mobility, C_{ox} is the specific capacitance formed in the gate and channel junction, $(W/L)_1$ is the width over length of the input transistor, V_{t1} is the threshold voltage of the input transistor, V_{t2} of the output transistor, and V_{GS} the gate to drain voltage. The bias, *Idc*, in Fig. 1(a) is fed to the circuit through a buffering structure that prevents feedback distortion from its load [8]. Table I gives the comparison of the circuit's block diagram, Fig. 1(a), and its transistor implementation, Fig. 1(b), which is representative of its layout, Fig. 1(c).

TABLE I

Block	Transistors (Width:Length in microns per microns)			
Amp1	5(10:30)	6(10:10)	7(10:30)	
Amp2	8(25:30)	9(10:10)	10(9:30)	
Amp3	8(25:30)	9(10:10)	12(20:30)	
Amp4	14(10:30)		13(9:60)	
Amp5	14(10:30)		11(8:30)	
R1	1(10:10)	2(10:10)	3(10:10)	4(10:10)
R2	15(10:10)	16(10:10)	17(10:10)	18(10:10)
Amp6	25(10:30)	26(10:10)	27(10:30)	
Amp7	28(25:30)	29(10:10)	32(9:30)	
Amp8	28(25:30)	29(10:10)	30(20:30)	
Amp9	34(10:30)		33(9:60)	
Amp10	34(10:30)		31(8:30)	
R3	21(10:10)	22(10:10)	23(10:10)	24(10:10)
R4	35(10:10)	36(10:10)	37(10:10)	38(10:10)
J	19(10:30)	20(10:10)		

III. ANALYSIS

Error voltage, and in effect error current, occurs at the intermediary gate of any current mirror that contains a switch. This is due to the gate to drain or source junction capacitance expunging charge that it has withheld from a previous release stage. Rather than compensating with amplifier modification constants, the switches can be modified to give equal amount of error in order to cancel each other exactly and consistently. Error due to constant and signal components are canceled because of this, with only a necessary comparison of error due to P and N type switches. This can be obtained with simplified equations from [4]:

$$C_{total} = C_{OX}(WL)_{sw} \tag{3a}$$

$$Q_{total} = C_{total}(V_{Gsw} - V_{Tsw}) \tag{3b}$$

$$V_C = \frac{Q_{total}}{C_2} = \frac{C_{OX}(WL)_{sw}(V_{Gsw} - V_{Tsw})}{C_{OX}(WL)_2} = \frac{(WL)_{sw}}{(WL)_2}(V_{Gsw} - V_{Tsw}) \tag{3c}$$

Here C_{total} is the total gate capacitance of the switch transistor, C_2 is the capacitance of the output transistor.

So we see that the error voltage is a function of the threshold voltage, V_t and can be recompensed with $(WL)_2$, comparing terms of the N-switch, and P-switch, where V_{TN} and V_{TP} are the N and P switch threshold voltages respectively:

$$(WL)_{swN}(V_{Gsw} - V_{TN}) = (WL)_{swP}(V_{Gsw} - V_{TP}) \tag{4a}$$

$$W_{swP} = W_{swN}\left(\frac{V_{Gsw} - V_{TP}}{V_{Gsw} - V_{TN}}\right) \tag{4b}$$

Figure 1(c) shows the MOSIS 2 micron technology VLSI layout. Simulation was optimized for this technology: the N switches were set to have a *W/L* of *10/10*, and the P switches, *8/10* due to the relationship in (4b). The amplification, *A*, was taken as 0.45, and the delay modification, *B*, as 0.80. For non-biasing and non-switch transistors, the standard lengths used were 30 microns, and widths 10 or 25 microns for the NMOS or PMOS respectively. Figure 2 shows the output of the N-switch circuit (top curve) and the P-switch circuit (bottom curve) separated, along with the results of the complementary circuit (middle curve) and the input signal (smooth curve).

IV. SUMMARY AND CONCLUSIONS

We have demonstrated a circuit that cancels clock feed through with complementary addition that avoids signal rerouting. As well, the results of this sample and hold method are good, and have shown great improvement in comparison with previous methods.

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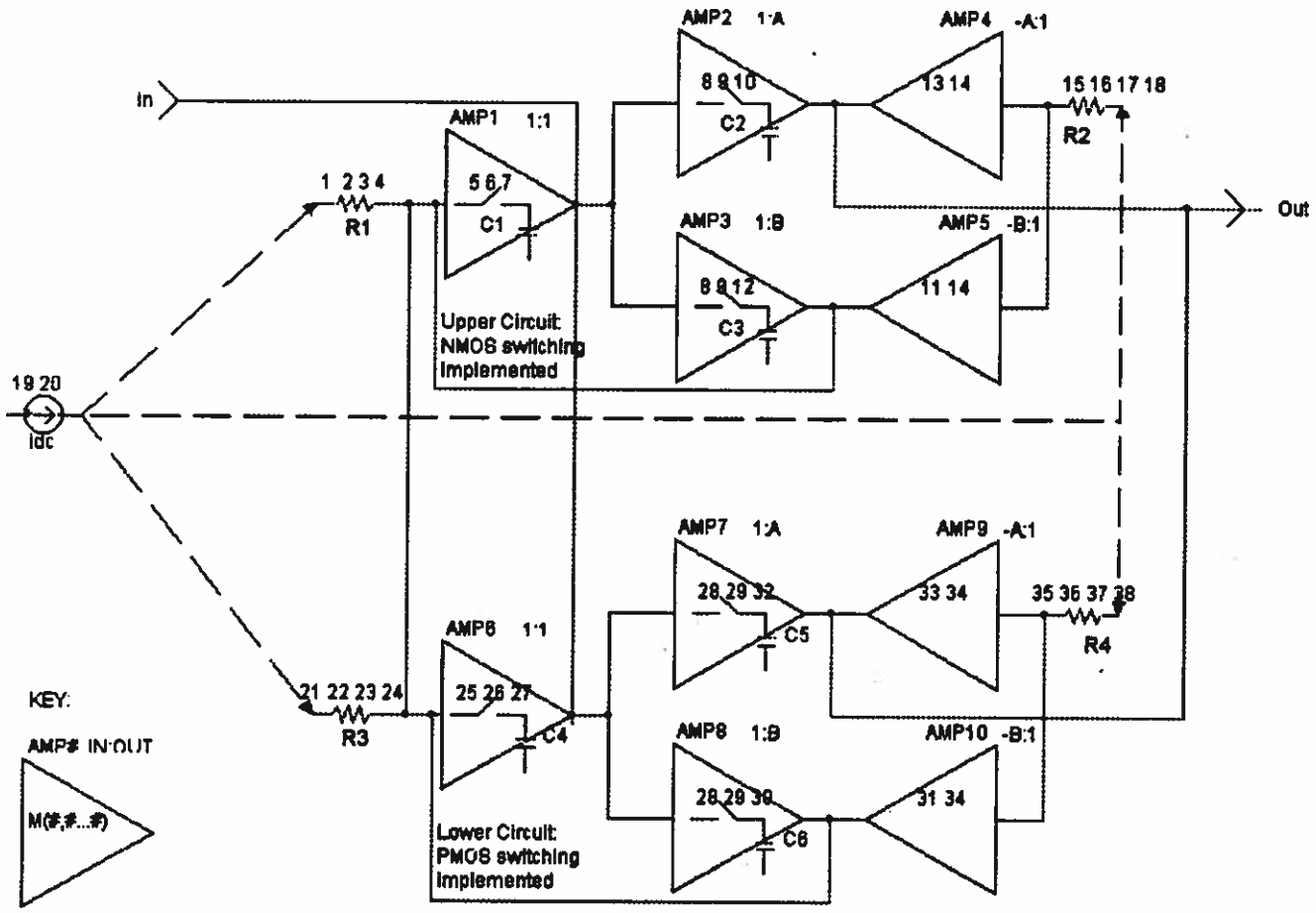
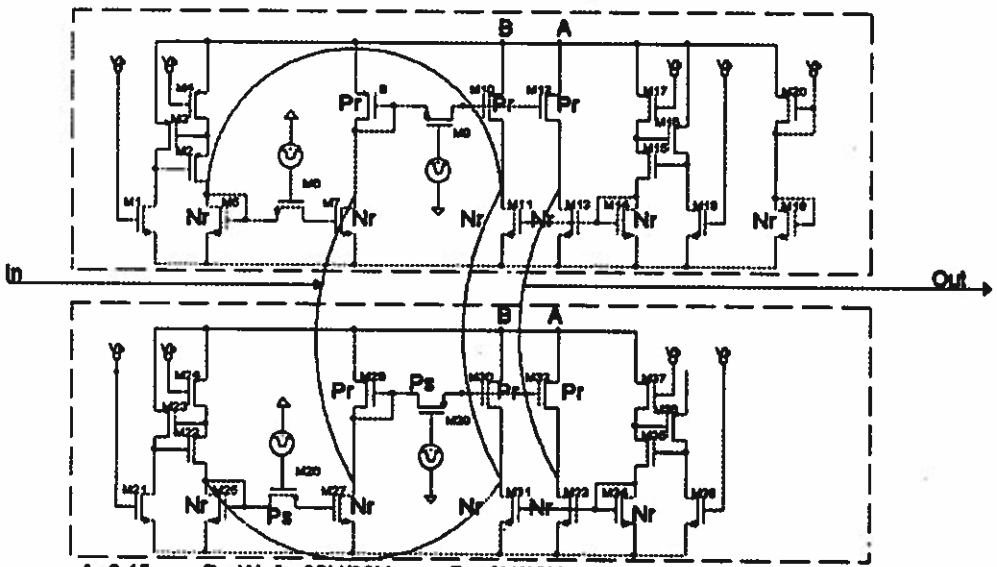


Figure 1(a). Block diagram of new circuit, the center-dashed-line that pulls the bias current also can be used to visualize the distinguishing of the N and P complements. The numbers inside or near the components indicate its counterpart in (b), also correlated to TableI.



W of M10 would be Pr*B=25U*0.80
*Unlabeled transistor have W/L=10U/10U

Figure 1(b). The transistor version of (a).

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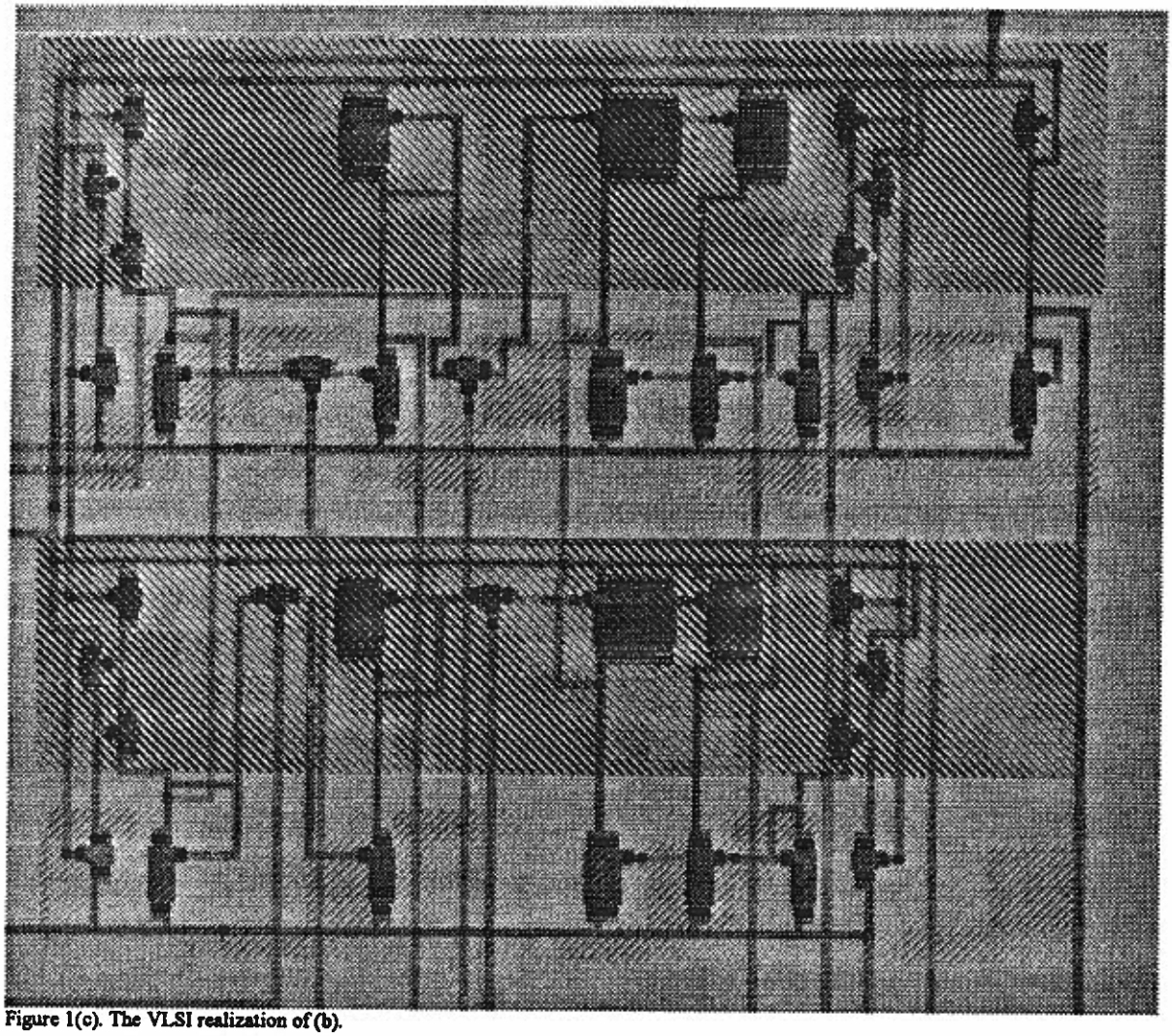

Figure 1(c). The VLSI realization of (b).

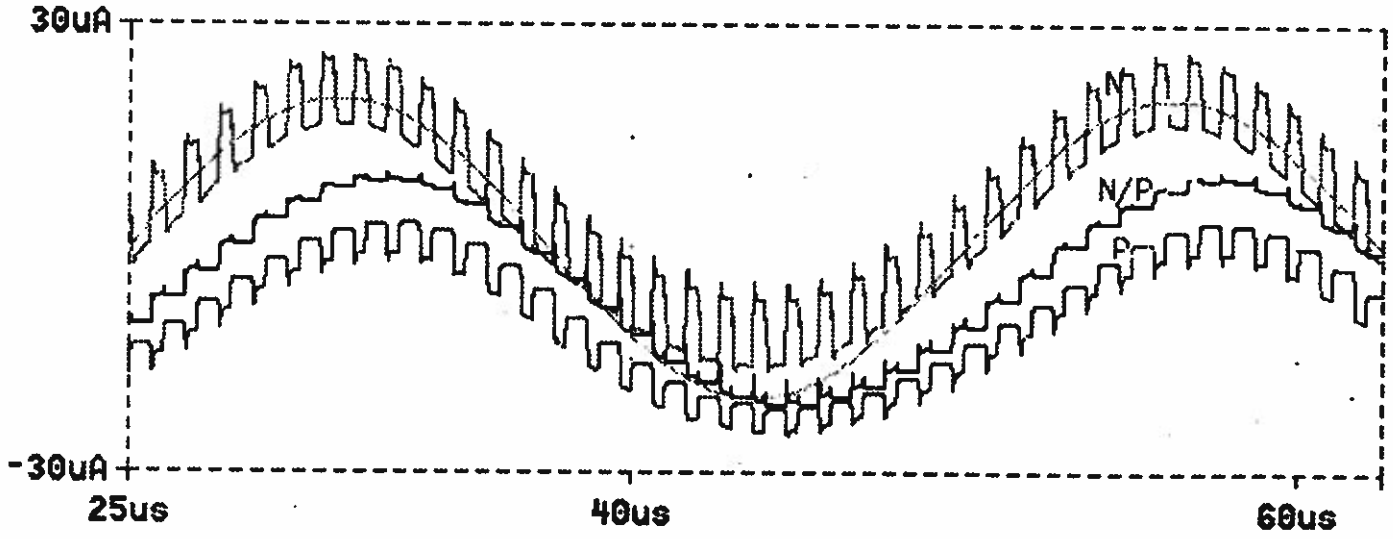

Figure 2. From top to bottom, N-switch, P-switch, and complementary circuit results. Smooth line is the input.

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