# A Switched Current Mode Real Ear-Type Lattice

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***Abstract*** **- Switched current circuits are used here to design real degree-one discrete time lattices for use in modeling the inner ear portion of ear-type networks. This lattice is characterized as an electrical two port system and is, therefore, described by a transfer scattering matrix relating input and output signals. This matrix is degree-one and requires only one delay function, which we realize with a switched current circuit containing only one delay. This circuit uses a new sampling switch that substantially reduces the distortion occurring due to the clock feed through in conventional MOS based switches. Spice simulation results are included to support the theory.**

## I. INTRODUCTION

With the advent of switched current circuits, digital signal processing systems can now be implemented with active solid state devices that require less layout space than switched capacitor systems and, as well, give more precision due to output values not being completely dependent on permanent values of passive components [1]. This advantage has specific applications in biomedical engineering where it is desirable to miniaturize and perfect a system that would serve as a surrogate sensory organ or as an organic interface to repair neural-signal transmission. The simulations presented ahead pertain to the digital implementation of a cochlear model of the inner ear.

Sound pitches are the human perceived frequency of a tone transmitted through alternating pressures of air against the outer ear. The purpose of the outer ear's shape is to localize sound sources and to pass the waves through the ear canal into the eardrum. The center of the eardrum is attached to the malleus, which is tapered to the incus, passing the vibrations through the faceplate. The ossicular section forces the wave into the stapes, of much smaller volume, amplifying the pressure by 30 dB. This extra amplification is necessary to accelerate the cochlea fluid, requiring more force due to its greater inertia. The cochlea is spatially organized so that the apex is the most sensitive to low pitches and the base to high pitches (Fig. 1), as the cochlea is structured such that higher frequencies dissipate closer to the base. The stapes is loosely connected to the oval window of the cochlea, on the outside of the scala vestibuli and media. Bulges due to the inward thrust are kept in balance by the round window, attached to the scala tympani as in Fig.1. The two sections are separated by the basilar membrane, connected to sound receptive hair cells that connect to the cochlear section of the brain [2].

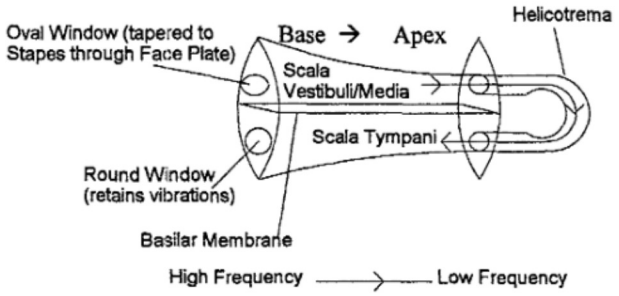


Figure 1. Cochlea Model. Fluid waves are produced by vibrations against the oval window, retained by the round window, and travel along the basilar membrane, and through the helicotrema. The distance away from the base along the basilar membrane is inversely proportional to the frequency the receptive hair cell at that point is resonant with.

The round window does not fully retain the vibrations however and a return signal is sent back to the outside world, the Kemp Echo [3]. This is emitted as a function of the input pitch and amplitude, with a delay commensurate with the effective sampling rate, or the location along the basilar membrane that corresponds to the input pitch. This can be modeled as a loaded two port network system which has been shown to best be characterized by a scattering matrix which can be implemented with a cascade of lattices described by scattering transfer matrices [4]. This cascade consists of degree two and one sections as one travels along the cochlea and combines ideal and limited operating regions within the cochlea. The order of speed required for these operations, and the design aspects involved are in the same order and mechanism of electric current, which makes current-mode transistorized implementation ideal.

By nature, human receptive systems are non-continuous due to lumped hair cells which sample input signals at a given rate, and then integration operations are performed within the brain. In this light, the lattice is composed of digital signal processing components, specifically, the return delay of the Kemp Echo, for which zeros of the transfer function do not occur on the unit circle. These components are expressed in the discrete time domain, or the z-domain where $z$ is the unit advance.

Over the past decade, much development has been accomplished in switched circuit systems [5,6,7]. In theory, this method accomplishes sample-and-hold type analog to digital conversion. At first, linear floating capacitors would take on this task, leading to precision errors, as well as the

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requirement of operational amplifier components [8]. Now, however, we utilize the built in capacitance of MOS transistors for holding, and their operating region dependencies to dictate switch states. One problem associated with this method is that the signal output value during the hold stage has clock and signal-based components added to it, known as clock-feed through error. Capacitance connections between the switch transistor and the output transistor are the main cause [9]. Many methods in the past have been shown to reduce this problem, usually by either increasing area ratios between the switch and output transistor [10], or reproducing the distortion to subtract it from the output [11]. In the simulations, a new method is used showing a considerable improvement [12].

## II. GENERAL MATRIX MODEL

The cochlea can be treated as blocks of cascaded two port networks as seen in Fig. 2(a), a single block of which would have a scattering matrix $\theta(z)$ relating its incident and reflected signals in matrix form:

$$\begin{bmatrix} v_1^i \\ v_1^r \end{bmatrix} = \theta(z) \begin{bmatrix} v_2^r \\ v_2^i \end{bmatrix} \tag{1a}$$

$$\theta(z) = \frac{1}{\sqrt{1-kk^*}} \begin{bmatrix} 1 & -k \\ -k^* & 1 \end{bmatrix} \cdot \begin{cases} \begin{bmatrix} f(z) & 0 \\ 0 & 1 \end{bmatrix} & |a|>1 \\ \begin{bmatrix} 1 & 0 \\ 0 & f(z) \end{bmatrix} & |a|<1 \end{cases} \tag{1b, 1c}$$

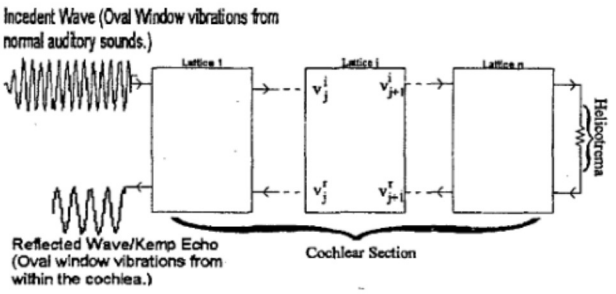
$$f(z) = \frac{z^{-1} - a^*}{1 - az^{-1}} \tag{1d}$$

where $a$ is the non-unit pole of transmission and $k$, the cross-arm gain, is between zero and one, as shown in Fig. 2(b).

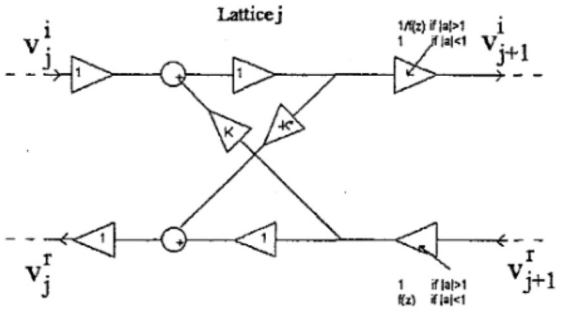
We limit ourselves here to real cases, that is, where imaginary components are non-existent. The parameters, $a^*$ and $k^*$, represent the complex conjugates of $a$ and $k$ which are consequently real.

In our realization, both the incident and reflected signals are represented by electric current values in the microampere range. Lattice branches can be represented by MOS current mirrors with gains proportional to area ratios, block-input nodal summation connections in the lattice are the same as in the current domain because of the current addition properties of Kirchhoff's Law. Nodal splitting can be accomplished with a current mirror containing parallel output branches.

To implement digital delay operations, we make use of Hughes' circuits [1] as seen in Fig. 3. A simple memory cell can consist of a switch connected MOS current mirror. The unit delay, $z^{-1}$, is obtained by placing a half-cycle switch (sampler) in between the drain and gate of an NMOS with a second half-clock cycle switch (holder) isolating the output to give half of a sample and hold. Another half-cycle delay configuration cascades two of these memory cells with non-overlapping complementary switches to obtain the full cycle. As shown in Fig. 3 (without the feedback $i_f$ branch) the output transistor of the first stage, *M2*, charges its gate source capacitance to

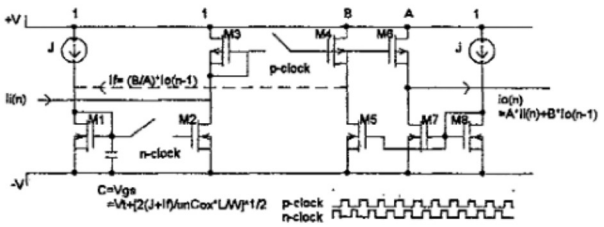



(a)




(b)

Figure 2. *(a)* For $a \neq 1$ and $|k|<1$, a cascade of lattices representing the cochlear section, *(b)* inspection of block j.




(c)

Figure 3. Realization of $-A/(1-Bz^{-1})$.

$$Vgs = Vt + \sqrt{(2Ids \cdot L/W)/(u_n C_{ox})} \tag{2}$$

when the *n-clock* switch is closed. When opened, the *p-clock* closes, and the voltage level is transferred through *M3*, *M4*, and *M6*, to $i_o$. This value is constant throughout the full cycle since the *n-clock* only closes after the *p-clock* reopens.

## III. REALIZATION OF F(Z) FOR REAL SECTION

1) The function, $f(z)$, of (1d) is a lossy integrator but by partial fraction expansion it is reducible to a backwards integrator plus a constant:

$$f(z)=\frac{1/a-a^*}{1-az^{-1}}-\frac{1}{a}, \qquad \frac{1}{f(z)}=\frac{a-1/a^*}{1-z^{-1}/a^*}-a. \tag{3a, b}$$

We will therefore limit our discussion to the backwards type.

Also, since we are dealing with the non-complex instance, $a^*$ is equal to $a$, so that $f(z)$ and its reciprocal are realized by the same structure within a sign.

Pole and zero scaling, changing the $z^{-1}$ coefficients, is necessary, and performed by increasing the output width to length ratios of the second memory cell (*M4-M7*) in Fig. 3, splitting the drains of *M4* and *M5* into a feedback connection, and the drains of *M6* and *M7* into the output branch. To get the transfer function for Fig. 3, taking the initial clock cycle as *(n-1)*, we obtain through branch arithmetic as in [1]:

$$i_o(n)=Bi_o(n-1)-A\,i_i(n), \text{ or} \tag{4a}$$

$$i_o(z)=Bi_o(z)z^{-1}-A\,i_i(z), \tag{4b}$$

Giving the first term of (3a or b) as

$$H(z)=\frac{i_0(z)}{i_i(z)}=\frac{-A}{1-Bz^{-1}}. \tag{4c}$$

The lattice was simulated in PSpice, Fig. 4, using ideal current transfer blocks, and an optimized $f(z)$ [12], with $a=1.25$. $A$ was taken as $1/a-a$, and $B$ as $1/a$ in accordance with the comparison of (3b) and (4c). The input frequency used was 10 kHz, with a clock rate of 250 kHz (25 clock samples per signal period). Both Matlab, Fig. 5(a), and PSpice, Fig. 5(b), showed an equal phase shift of 24°±24', one full clock cycle.

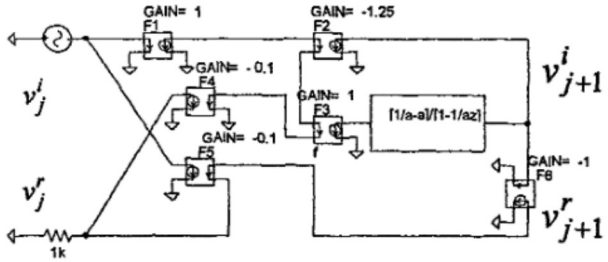



Figure 4. Ideal circuit realization for $|a|>1$ with the block portion representing the optimized version of Fig. 3 from [12].

## IV. TRANSISTOR REALIZATION OF REAL DEGREE ONE LATTICE

The transistor realization of the lattice is obtained by replacing the gain blocks with current mirrors, whose output width to length ratios are proportional to the respective block gains. Bidirectional current mirrors were used to eliminate the need for large input bias currents. A bias current was still required to account for offset error within the transistors but no loading problems were encountered. As well, output transistors were given width to length ratios up to 135 percent the size its input transistor to account for current attrition. The circuit is shown in Fig. 6 with results in Fig. 5(c).

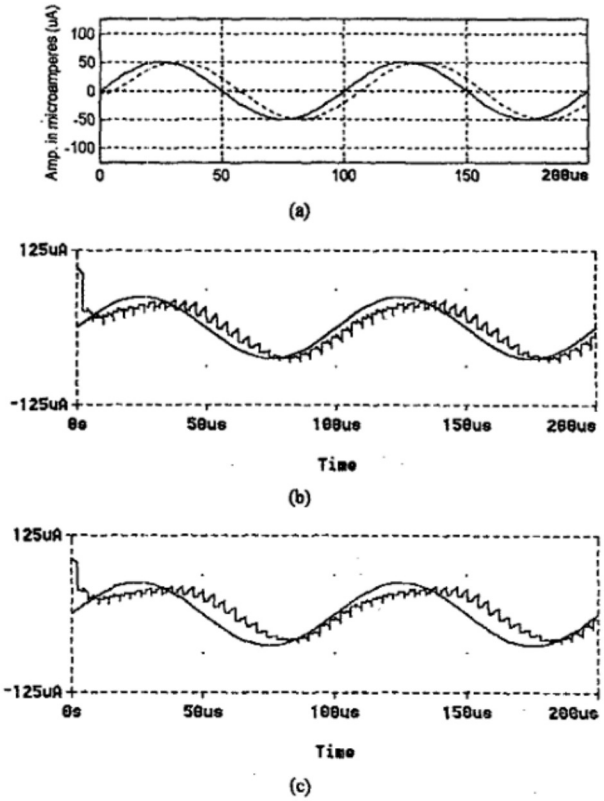



Figure 5. Lattice simulation results of *(a)* purely numerical system based on (1b) using Simulink (Matlab), *(b)* current gain block circuit using PSpice, and *(c)* full transistorized circuit using PSpice.

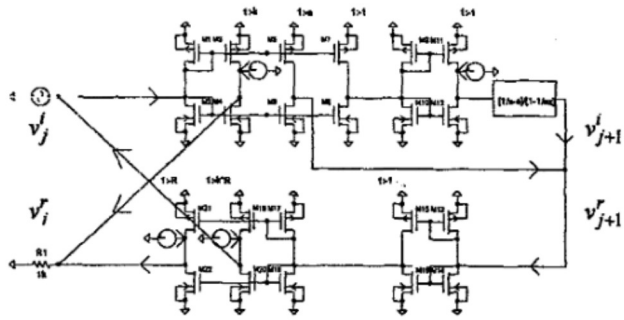


Figure 6. Full transistorized lattice.

## V. TRANSISTOR REALIZATION OF TERMINAL LATTICE

To obtain the Kemp Echo through building current mirror structures, physical design requires obtaining the echo, $v_i^r$ in terms of $v_i^i$, the input incident wave. This can be easily

accomplished by setting the termination end (helicotrema) as a one port network, with backwards amplification, $R$, as in [4]. By combining the final lattice with the termination, a simplified realization can be obtained for the two with:

$$v_2^i = Rv_2^r , \tag{5a}$$

giving a gain of:

$$A_1(z) = \frac{v_1^r}{v_1^i} = \frac{\theta 21 + R\theta_{22}}{\theta 11 + R\theta 12} . \tag{5b}$$

From (1b) and (1c), we obtain $\theta$ for $|a|>1$ *or* $|a|<1$:

$$\theta = \frac{1}{\sqrt{1-kk^*}} \left\{ \begin{bmatrix} f(z) & -k \\ -f(z)k^* & 1 \end{bmatrix} or \begin{bmatrix} 1 & -kf(z) \\ -k^* & f(z) \end{bmatrix} \right. . \tag{6a,b}$$

Substituting (1d) into (6a), then (6a) into (5b):

$$A(z) = \frac{-(R + a^* k^*)}{a^* + kr} \cdot \frac{1 - (k^* + aR)(R + a^* k^*)^{-1} z^{-1}}{1 - (1 + akR)(a^* + kR)^{-1} z^{-1}} . \tag{7a}$$

Separating variables:

$$A(z) = \frac{(k^* + aR)(1 + akR)^{-1} - (a^* k^* + R)(a^* + kR)^{-1}}{1 - (1 + akR)(a^* + kR)^{-1} z^{-1}} - \frac{k^* + aR}{1 + akR} . \tag{7b}$$

For the case of $|a| < 1$, we can apply the same methodology to obtain:

$$A(z) = \frac{(ak^* + R)(a + kR)^{-1} - (k^* + a^* R)(1 + a^* kR)^{-1}}{1 - (a + kR)(1 + a^* kR)^{-1} z^{-1}} - \frac{ak^* + R}{a + kR} . \tag{7c}$$

Hence we obtain a backwards integrator for both cases of the termination lattice in the form $-A/(1-Bz^{-1})-C$, the termination lattice only requires the circuit in Fig. 3, and an added constant transfer function attainable with an extra current mirror.

## VI. CONCLUSIONS

In this paper we use switched current circuits to realize real degree-one discrete-time lattice sections. We also use partial fraction expansion to reduce the need for a full integrator so we can use the more easily implemented offset backward one. By treating the cochlear termination as an amplification factor, we were as well able to reduce the terminating lattice section to an offset z function with a zero at infinity, allowing us to use the same circuit as for the simple switch current circuit of Fig. 3, only requiring the modification of transistor width values.

Due to space limitations, analysis of the new switched current structure used to realize Figs. 4 and 6 is being prepared as a separate article [12].

## ACKNOWLEDGEMENTS

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