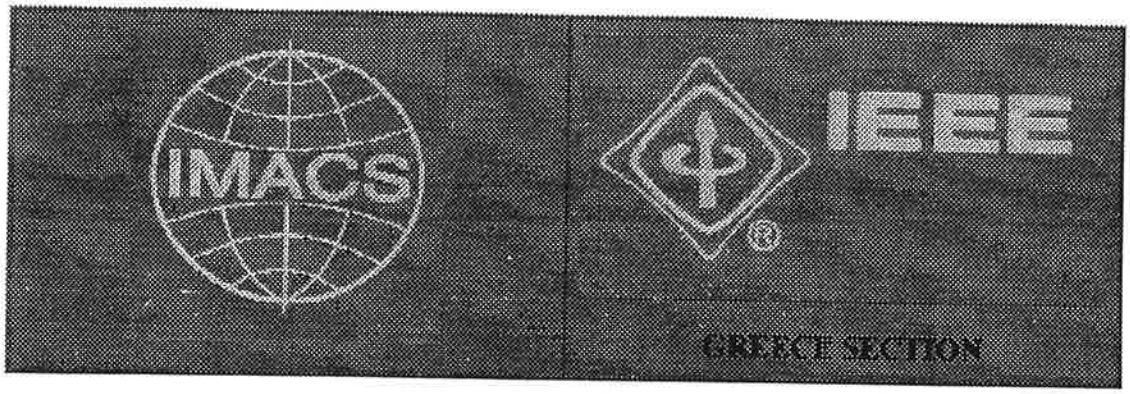

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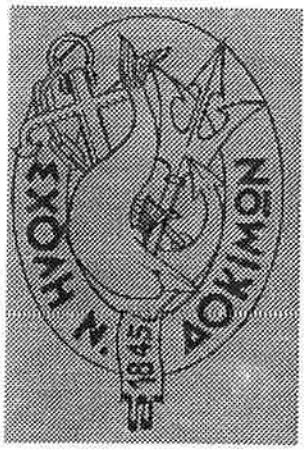

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The Large Signal Behavior of El Masry's Differentiator

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Abstract

Analysis of the continuous-time current-mode differentiator introduced by El-Masry and Gates, is performed in this work. It is shown that this circuit differentiates not only under the small-signal assumption made by El-Masry and Gates, but for large-signals as well. This circuit is studied because of its simplicity in CMOS implementation, its small size, low power consumption, and its applicability to filter design.

1. Introduction

The continuous-time current-mode differentiation circuit, introduced by El-Masry and Gates [1], is shown in figure 1. The input stage of MOSFETs M1 and M4 is an active load that forms the input resistance. This active load is capacitively coupled to the input of a bi-directional current mirror which is composed of M2, M3, M5 and M6, through the capacitor C. The differentiated current is output from the drains of transistors M3 and M6. The active load allows to establish a low resistance at the input of the differentiator, which along with the capacitor C sets the integration time-constant to be small.

In [1] the small-signal behavior of this differentiation circuit is obtained using the small-signal model for MOSFETs. Under the assumption that the output resistance of the input current source is much higher than the differentiator's input resistance and that the differentiator's output resistance is much higher than the resistance of the load that is connected to the output of this circuit, the differentiator's transfer function is approximated in [1] as $\frac{i_{out}}{i_{in}} \approx -\frac{C}{g_{m_p} + g_{m_n}} \cdot s = -\alpha \cdot s$, where g_{m_p} and g_{m_n} are the incremental transconductances for the pMOS and nMOS transistors respectively. The application of this differentiator to the implementation of first and second order filters is also demonstrated in [1]. Two major advantages and one disadvantage of this circuit, regarding filter design, are discussed in [1]. The advantages are low power consumption and high bandwidth, while the disadvantage in comparison to integration circuits is that this differentiator cannot reach the highest frequencies that can be reached with an integrator.

Here, the analysis of the circuit in figure 1 is based on the large-signal model for MOSFETs, and both the small-signal and the large-signal behavior of the circuit are obtained.

2. General Analysis of the Differentiator Circuit

The MOSFETs in the differentiator circuit of figure 1 work in saturation. The quadratic model for the drain current of a MOSFET in saturation, enhanced with the channel modulation parameter, is

$$I_{d_\nu} = \beta_\nu \cdot \left(V_{gs} - V_{T_\nu}\right)^2 \cdot \left(1 + \lambda_\nu \cdot V_{ds}\right) \qquad (1)$$

with $V_{gs} = V_g - V_s$, $V_{ds} = V_d - V_s$, where V_g, V_s, V_d, V_T, are the gate, source, drain, and threshold voltages respectively, λ is the channel modulation factor, and the index ν refers to the type of channel, i.e. either ν=p or ν=n. For n-channel $\beta_n = \frac{KP_n}{2} \cdot \frac{W_n}{L_n}$ while for p-channel $\beta_p = -\frac{KP_p}{2} \cdot \frac{W_p}{L_p}$, where W and L are the channel width and length respectively, and KP is the transconductance parameter. The MOSFETs M1, M2, M4, M5, in the circuit of figure 1 have $V_{ds} = V_{gs}$, where $V_s = V_{dd}$ for the pMOS devices and $V_s = V_{ss}$ for the nMOS devices. Then, assuming all parameters being constant in Eq (1) except for the gate voltage, the drain current I_d in each of these transistors is a function $f(\cdot)$ of their gate voltage which is represented by the variable u:

$$I_{d_\nu} = f_\nu(u)$$

$$= \beta_\nu \cdot \left(u - V_s - V_{T_\nu}\right)^2 \cdot \left(\left(1 - \lambda_\nu \cdot V_s\right) + \lambda_\nu \cdot u\right) \qquad (2)$$

Use of KCL at node with voltage V_1 results in

$$I_{in} - f_p(V_1) - f_n(V_1) - C\frac{d\left(V_1 - V_2\right)}{dt} = 0 \qquad (3)$$

Use of KCL at node with voltage V_2 results in

$$-f_p(V_2) - f_n(V_2) + C\frac{d\left(V_1 - V_2\right)}{dt} = 0 \qquad (4)$$

Let us assume that the MOSFETs M3, M6, in the output current mirror stage are larger (i.e. wider channel) by a factor k than the other MOSFETs. Then, the current through M3 is $I_{d_3} = k \cdot f_n(V_2)$ and the current through M6 is $I_{d_6} = k \cdot f_p(V_2)$. Application of KCL at the output node gives

$$I_{out} = -k \cdot f_p(V_2) - k \cdot f_n(V_2) \qquad (5)$$

3. Large-Signal Analysis of the Differentiator Circuit

Let us use Eq (2) and calculate the term $f_p(u)+f_n(u)$ that is used in Eqs (3)-(5), as

$$f_p(u)+f_n(u)=$$

$$\left(\beta_p\cdot\lambda_p+\beta_n\cdot\lambda_n\right)\cdot u^3$$

$$+\left(\begin{array}{l}\beta_p\cdot\begin{pmatrix}1-\lambda_p\cdot V_{dd}\\-2\cdot\lambda_p\cdot\left(V_{dd}+V_{T_p}\right)\end{pmatrix}\\+\beta_n\cdot\begin{pmatrix}1-\lambda_n\cdot V_{ss}\\-2\cdot\lambda_n\cdot\left(V_{ss}+V_{T_n}\right)\end{pmatrix}\end{array}\right)\cdot u^2$$

$$+\left(\begin{array}{l}\beta_p\cdot\begin{pmatrix}\lambda_p\cdot\left(V_{dd}+V_{T_p}\right)^2\\-2\cdot\left(1-\lambda_p\cdot V_{dd}\right)\cdot\left(V_{dd}+V_{T_p}\right)\end{pmatrix}\\+\beta_n\cdot\begin{pmatrix}\lambda_n\cdot\left(V_{ss}+V_{T_n}\right)^2\\-2\cdot\left(1-\lambda_n\cdot V_{ss}\right)\cdot\left(V_{ss}+V_{T_n}\right)\end{pmatrix}\end{array}\right)\cdot u$$

$$+\beta_p\cdot\left(1-\lambda_p\cdot V_{dd}\right)\cdot\left(V_{dd}+V_{T_p}\right)^2$$

$$+\beta_n\cdot\left(1-\lambda_n\cdot V_{ss}\right)\cdot\left(V_{ss}+V_{T_n}\right)^2 \qquad (6)$$

Let us assume the special, but most usual, case of complementary transistors where $|\beta_p|=|\beta_n|$, $|V_{T_p}|=|V_{T_n}|$, $\lambda_p=\lambda_n$. If the substitutions $\beta_p=-\beta_n$, $V_{T_p}=-V_{T_n}$, $\lambda_p=\lambda_n$ are made in Eq (6), then it simplifies to Eq (7):

$$f_p(u)+f_n(u)=$$

$$\beta_n\cdot\lambda_n\cdot\left(3\cdot\left(V_{dd}-V_{ss}\right)-4V_{T_n}\right)\cdot u^2$$

$$+\beta_n\cdot\left(\begin{array}{l}\left(V_{dd}-V_{T_n}\right)\cdot\left(2-3\cdot\lambda_n\cdot V_{dd}+\lambda_n\cdot V_{T_n}\right)\\+\left(V_{ss}+V_{T_n}\right)\cdot\left(-2+3\cdot\lambda_n\cdot V_{ss}+\lambda_n\cdot V_{T_n}\right)\end{array}\right)\cdot u$$

$$+\beta_n\cdot\begin{pmatrix}\left(1-\lambda_n\cdot V_{ss}\right)\cdot\left(V_{ss}+V_{T_n}\right)^2\\-\left(1-\lambda_n\cdot V_{dd}\right)\cdot\left(V_{dd}-V_{T_n}\right)^2\end{pmatrix} \qquad (7)$$

Let also the approximation $\lambda_n=0$ be made in the MOSFET's model in Eq (1). Then Eq (7) simplifies to Eq (8):

$$f_p(u)+f_n(u)=$$

$$\beta_n\cdot 2\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)\cdot u$$

$$-\beta_n\cdot\left(V_{dd}+V_{ss}\right)\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right) \qquad (8)$$

Then, using Eq (8) in Eq (3) it becomes

$$C\frac{d\left(V_1-V_2\right)}{dt}=$$

$$-\beta_n\cdot 2\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)\cdot V_1$$

$$+\beta_n\cdot\left(V_{dd}+V_{ss}\right)\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)+I_{in} \qquad (9)$$

and likewise Eq (4) becomes

$$-C\frac{d\left(V_1-V_2\right)}{dt}=$$

$$-\beta_n\cdot 2\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)\cdot V_2$$

$$+\beta_n\cdot\left(V_{dd}+V_{ss}\right)\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right) \qquad (10)$$

Subtraction of Eq (10) from Eq (9) gives

$$2\cdot C\frac{d\left(V_1-V_2\right)}{dt}=$$

$$-\beta_n\cdot 2\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)\cdot\left(V_1-V_2\right)+I_{in} \qquad (11)$$

Let a change of variables where $y=\dfrac{d\left(V_1-V_2\right)}{dt}$. Differentiation on both sides in Eq (11) and substitution of the new variable y, yields:

$$\frac{dy}{dt}=-\frac{\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}{C}\cdot y+\frac{1}{2\cdot C}\cdot\frac{dI_{in}}{dt} \qquad (12)$$

Solution of Eq (12) for y results in

$$y(t)\approx\frac{1}{2\cdot\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}\cdot\frac{dI_{in}(t)}{dt} \qquad (13)$$

Also, Eqs (4) and (5) give

$$I_{out}=-k\cdot C\frac{d\left(V_1-V_2\right)}{dt}=-k\cdot C\cdot y \qquad (14)$$

Substitution of y from Eq (13) into Eq (14) results in

$$I_{out}=-k\cdot\frac{C}{2\cdot\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}\cdot\frac{dI_{in}}{dt} \qquad (15)$$

Equation (15) shows that the current at the output of this circuit is proportional to differentiation on its input current.

The derivation of Eq (13) is shown next. If the input current is the step function, i.e. $I_{in}(t)\equiv u(t)$, then the driving input in the differential Eq (12) is impulse, i.e. $\dfrac{dI_{in}(t)}{dt}=\delta(t)$. Then, the response $y(t)$ to impulse is

$$y_\delta(t)=A\cdot\exp\left(-\frac{\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}{C}\cdot t\right) \qquad (16)$$

where $A=y_\delta(0)=1$ and $t>0$. If $I_{in}(t)$ is any function, then the solution to Eq (12) is the sum of its zero input response and zero state response [2]:

$$y(t) = y(0)\cdot\exp\left(-\frac{\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}{C}\cdot t\right)$$

$$+\int_0 y_\delta(t-\tau)\cdot\frac{1}{2\cdot C}\cdot\frac{dI_{in}(\tau)}{d\tau}d\tau \qquad (17)$$

The time-constant $\frac{C}{\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}$ is very small; if C is a few picofarads, then this time-constant is of the order of 10^{-8} sec. Thus, $y_\delta(t)$ drops very fast to zero for $t>0$. Using this observation, the convolution in Eq (17) is approximated as

$$\int_0 y_\delta(t-\tau)\frac{dI_{in}(\tau)}{d\tau}d\tau = \int_0 y_\delta(\tau)\frac{dI_{in}(t-\tau)}{d(t-\tau)}d\tau$$

$$\approx \int_0 y_\delta(\tau)\cdot\frac{dI_{in}(t)}{dt}d\tau$$

$$= \frac{dI_{in}(t)}{dt}\cdot\int_0 y_\delta(\tau)d\tau \qquad (18)$$

Then, from Eqs (16) and (18) the zero-state response becomes

$$\int_0 y_\delta(t-\tau)\cdot\frac{1}{2\cdot C}\cdot\frac{dI_{in}(\tau)}{d\tau}d\tau =$$

$$-\left(\frac{1}{2\cdot C}\cdot\frac{C}{\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}\cdot\left(\exp\left(-\frac{\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}{C}\cdot t\right)-1\right)\right)\cdot \qquad (19)$$

If $\frac{\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)}{C}\cdot t >> 1$ then the exponents in Eqs (17) and (19) are approximately zero, so Eq (17) is approximated by Eq (13).

4. Small-Signal Analysis of the Differentiator Circuit

Under the assumption of small-signal operation, the following approximation is valid:

$$f_v(V_i)\approx f_v(V_{Q_i})+\left.\frac{d\left(f_v(u)\right)}{du}\right|_{u=V_{Q_i}}\cdot v_i \qquad (20)$$

where V_{Q_i} is the quiescent voltage at node i, that biases the corresponding MOSFET with $V_{gs}\big|_{Q\text{-point}} = V_{Q_i}-V_s$, and $v_i = V_i - V_{Q_i}$ is the incremental voltage at node i. Then, from Eq (20) the following also holds true:

$$\frac{d\left(f_v(V_i)\right)}{dV_i}=\frac{d\left(f_v(V_i)\right)}{dv_i}=\left.\frac{d\left(f_v(u)\right)}{du}\right|_{u=V_{Q_i}} \qquad (21)$$

Since the stages of M1, M4 and M2, M5 use the same geometry of transistors and are also biased similarly, they have $V_{Q_1}=V_{Q_2}$. Replacing u with V in Eq (8) and differentiating both of its parts gives

$$2\beta_n\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)=\frac{d\left(f_p(V_i)+f_n(V_i)\right)}{dV_i} \qquad (22)$$

Equation (22) with Eq (21) becomes

$$2\cdot\beta_n\cdot\left(V_{dd}-V_{ss}-2\cdot V_{T_n}\right)=\left.\frac{d\left(f_p(u)\right)}{du}\right|_{u=V_{Q_1}}+\left.\frac{d\left(f_n(u)\right)}{du}\right|_{u=V_{Q_1}} \qquad (23)$$

Using Eq (23) in the denominator of Eq (15) gives

$$I_{out}\approx-\frac{k\cdot C}{\left.\frac{d\left(f_p(u)\right)}{du}\right|_{u=V_{Q_1}}+\left.\frac{d\left(f_n(u)\right)}{du}\right|_{u=V_{Q_1}}}\cdot\frac{dI_{in}}{dt} \qquad (24)$$

where i refers either to node 1 or node 2 in Eq (24). Now, let us calculate the incremental parameters of transconductance g_m and output conductance g_{ds} that are used in the small-signal model of MOSFETs. Application of Eq (1) with $V_{ds}=V_{gs}$ gives

$$g_m=\left.\frac{dI_{d_n}}{dV_{gs}}\right|_{V_g=V_{Q_1}}$$

$$=2\cdot\beta_n\cdot\left(V_{Q_1}-V_s-V_{T_n}\right)\cdot\left(1+\lambda_n\cdot\left(V_{Q_1}-V_s\right)\right) \qquad (25)$$

and

$$g_{ds}=\left.\frac{dI_{d_n}}{dV_{ds}}\right|_{V_g=V_{Q_1}}=\beta_n\cdot\lambda_n\cdot\left(V_{Q_1}-V_s-V_{T_n}\right)^2 \qquad (26)$$

Differentiation in Eq (2) yields

$$\left.\frac{d\left(f_n(u)\right)}{du}\right|_{u=V_{Q_1}}=\left(\begin{array}{l}\left(2\cdot\beta_n\cdot\left(V_{Q_1}-V_s-V_{T_n}\right)\cdot\right.\\\left.\cdot\left(\left(1-\lambda_n\cdot V_s\right)+\lambda_n\cdot V_{Q_1}\right)\right)\\+\beta_n\cdot\left(V_{Q_1}-V_s-V_{T_n}\right)^2\cdot\lambda_n\end{array}\right) \qquad (27)$$

Comparison of Eqs (25), (26) and (27) results in

$$\left.\frac{d\left(f_n(u)\right)}{du}\right|_{u=V_{Q_1}}=g_{m_n}+g_{ds_n} \qquad (28)$$

Then, using Eq (28), the Eq (24) is re-written as

$$I_{out}\approx-\frac{k\cdot C}{g_{m_p}+g_{m_n}+g_{ds_p}+g_{ds_n}}\cdot\frac{dI_{in}}{dt}$$

$$\approx-\frac{k\cdot C}{g_{m_p}+g_{m_n}}\cdot\frac{dI_{in}}{dt}=-\alpha\cdot\frac{dI_{in}}{dt} \qquad (29)$$

where the assumption that $g_{m_p}+g_{m_n}>>g_{ds_p}+g_{ds_n}$ was also made, as it is always true. Equation (29) gives the same result as in [1] for small-signal operation.

5. Simulation Results

Figures 2 and 3 demonstrate simulations on the differentiator circuit with $C = 10\text{pF}$, $V_{dd} = +5\text{V}$, $V_{ss} = -5\text{V}$, and the input current I_{in} being chosen as a quadratic function of time. In the case of figure 2, both pMOS and nMOS transistors are modeled with identical, ideal square law, voltage controlled current sources, i.e. $\lambda_n = 0$, with $KP = 5 \cdot 10^{-5}\text{A/V}^2$ and $V_T = 0.86\text{V}$. Also, $\frac{W}{L} = 5$ for M1, M2, M4 and M5, $\frac{W}{L} = 10$ for M3 and $\frac{W}{L} = 14.25$ for M6. The amplitude of I_{in} is selected to be small enough in order to assume small-signal operation. In the case of figure 3, the MOSIS 2.0μm parameters are used for MOSFETs, where $KP_n = 5 \cdot 10^{-5}\text{A/V}^2$, $KP_p = 1.9 \cdot 10^{-5}\text{A/V}^2$, $\lambda_p = 5 \cdot 10^{-2}$, $\lambda_n = 1.8 \cdot 10^{-2}$, $V_{T_n} = 0.86\text{V}$ and $V_{T_p} = -0.89\text{V}$. Also, $\frac{W_n}{L_n} = 10$ for M1 and M2, $\frac{W_p}{L_p} = 27.8$ for M4 and M5, $\frac{W_n}{L_n} = 20$ for M3, and $\frac{W_p}{L_p} = 57$ for M6. The amplitude of I_{in} is selected to be large enough, amplified by 1000 times in comparison to figure 2, in order to assume large-signal operation. We observe that in figure 2 the output current I_{out} is linear, denoting the output of an almost perfect differentiator. In figure 3 the output current I_{out} is almost linear, still demonstrating acceptable differentiation.

6. Conclusions

This work proves that the differentiator that is proposed by EL-Masry and Gates [1] works for large signals. Then it uses the large-signal behavior in order to obtain, as a subcase, the small-signal behavior which is also obtained in [1]. The assumption $\frac{\beta_n \cdot \left(V_{dd} - V_{ss} - 2 \cdot V_{T_n}\right)}{C} \cdot t >> 1$, that was made in section 3, implies that this circuit behaves properly as a differentiator for adequately low frequencies with $\omega << \frac{\beta_n \cdot \left(V_{dd} - V_{ss} - 2 \cdot V_{T_n}\right)}{C}$. Since $\omega = 2 \cdot \pi \cdot f$, for typical values of C (a few pF) and β_n the frequency of operation is $f << 16\text{ MHz}$.

The analysis here, Eqs (3) and (4), considers only the current I_{in} going into the circuit. If however one feeds the circuit with a lossy current source and considers the current out of the lossless part of the source then the source impedance becomes a factor in the differentiation constant.

The differentiator's large-signal behavior is further demonstrated through simulation. This circuit has also been fabricated through MOSIS using the 2.0μm n-well CMOS process, and it was measured to work successfully as a differentiator.

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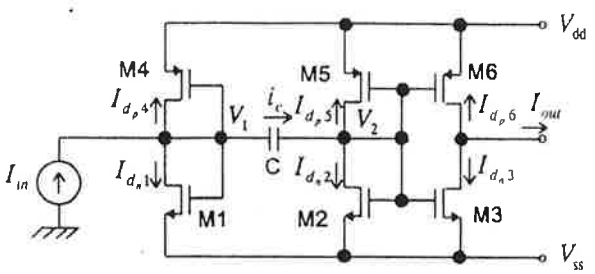

Figure 1: The differentiator circuit.

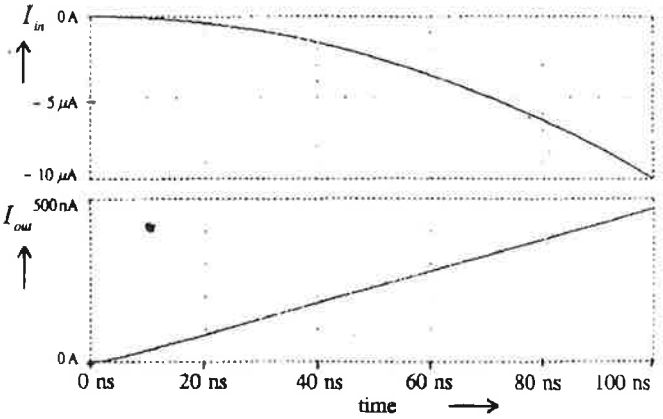

Figure 2: Simulation of the differentiator circuit, assuming quadratic transistor models and small-signal.

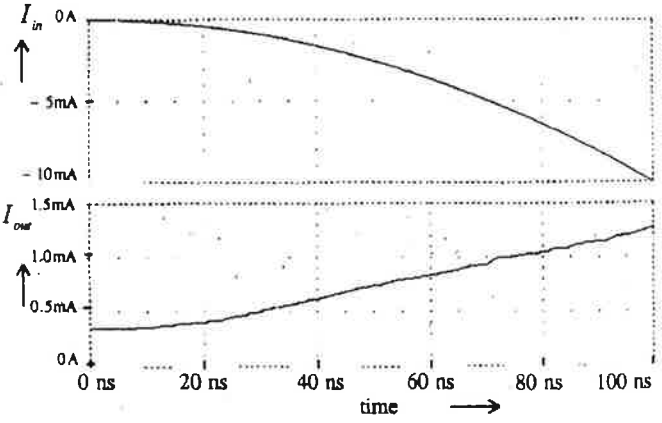

Figure 3: Simulation of the differentiator circuit, taking into account channel modulation in the transistor models. Also, large-signal operation is examined.