CMOS Bilateral Linear Floating Resistors for Neural-Type Cell Arrays

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Abstract

A previous CMOS bilateral linear resistor is modified into two different configurations of floating resistors using the structure of a two-transistor CMOS bilateral linear resistor in the first configuration and two two-transistor CMOS bilateral linear resistors and current mirrors in the second configuration. Simulation results using parameters of MOSIS transistors are presented to verify the theory. These floating resistors can be used for coupling weights in VLSI neural-type cell arrays.

1 Introduction

In Artificial Neural Networks (ANNs) [1] the neurons are connected by weights which govern how much of an effect the information from one neuron will have on other neurons. These weights can be set by resistor values [2], in which case it is important to have good VLSI floating bilateral resistors. Here we consider resistors to couple neural-type cells [3, 4]. We present a suitable class of simple VLSI floating bilateral, voltage tunable resistors which are essentially linear.

At times, standard MOS processes monolithic resistors have been implemented as polysilicon or diffusion strips acting as passive devices. But over the years many authors have developed uni- and bilateral linear floating active resistors containing MOS devices [5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15] due to the unpredictable dependence of resistor values on different fabrication process runs and the lack of means to tune these values. Unlike passive resistors, active CMOS resistor implementations usually take less die area and provide controllable resistor values. However, the nonlinearity of the MOSFET prohibits the use of large signals and, therefore, limits the dynamic range. To circumvent these limitations different circuit structures are proposed.

Since these active resistor implementations usually take less die area, compared to passive resistors, we present two configurations for a generalized floating active linear bilateral enhancement-mode CMOS device resistor. The ideal cases of two configurations are presented in section II with circuit realizations and analyses for the floating CMOS bilateral linear resistor configurations shown in section III. In section IV, PSpice simulation results using MOSIS parameters for the circuit are given.

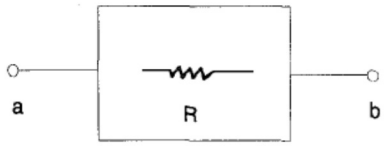

Figure 1: Configuration I of the CMOS bilateral linear floating resistor.

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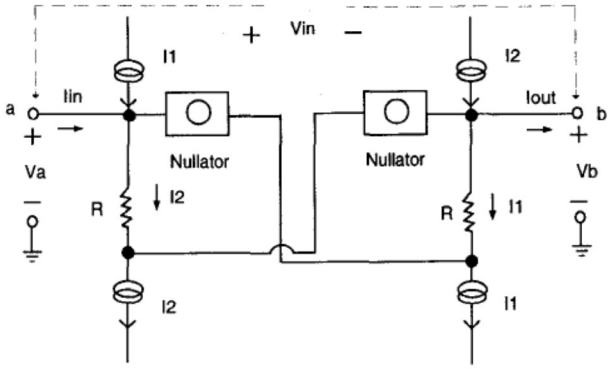

Figure 2: Configuration II of the CMOS bilateral linear floating resistor.

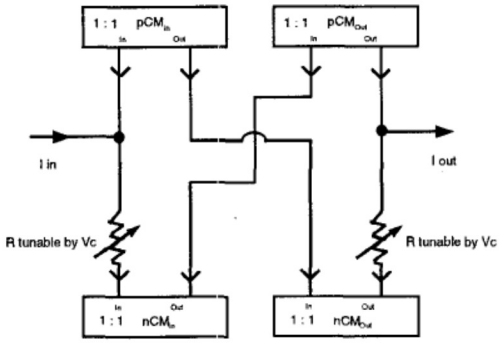

Figure 3: Practical realization of configuration II of the CMOS bilateral linear floating resistor.

2 The Ideal Floating Resistor Configurations

The first configuration, shown in Figure 1, is based on [5] and the second one shown in Figure 2 follows Rasmussen's architecture [6] of a total of four current sources in a technique similar to that of Singh [7]. For this resistor, realized by the scheme of Figure 3, a pair of NMOS and PMOS current mirrors on the input side are employed to mirror the current to the output side by another pair of NMOS and PMOS current mirrors which also allow cancellation of nonlinearities. The current is forced equally through the input and output sides [5] and equal voltages on the current mirrors can generate the nullators. In Figure 2 currents I_1 and I_2 can be written, by virtue of the nullators, as

$$I_1 = \frac{(V_b - V_a)}{R} \tag{1}$$

and

$$I_2 = \frac{(V_a - V_b)}{R} \tag{2}$$

Therefore the total input current I_{in} can be written as

$$\begin{aligned} I_{in} &= I_2 - I_1 = \frac{(V_a - V_b)}{R} - \frac{(V_b - V_a)}{R} \\ &= 2\frac{(V_a - V_b)}{R} \\ &= \frac{2}{R}V_{in} = I_{out} \end{aligned} \tag{3}$$

3 CMOS Realizations and Analyses of the Floating Resistors

Configuration I is realized by Figure 4 and consists of two MOS transistors and two control voltage sources which could be voltage controlled voltage sources (VCVS) for use in ANN weight adaptation. The NMOS transistor M_1 is connected to the PMOS transistor M_2 to form a floating resistor. The resistance of the circuit is controlled by V_{cp} connected to the gate of the PMOS transistor and by V_{cn} connected to the NMOS transistor, as illustrated in Figure 4. The substrate of the PMOS transistor is connected to $V_{DD}(+5V)$ and that of the NMOS transistor is connected to $V_{SS}(-5V)$ in order to back bias the substrate under all loads (less than bias sources).

Configuration II can be realized with four transistorized current mirrors as shown in Figure 5, the first pair consisting of NMOS current mirror nCM_{in} and PMOS current mirror pCM_{in} on the input side mirroring the currents I_1 and I_2 to the output side by the second pair of current mirrors consisting of NMOS current mirror nCM_{out} and PMOS current mirror pCM_{out}. This scheme of current mirrors is employed to cancel nonlinearities. The goal is to make the input and output currents the same and equal to the difference of the currents flowing in the PMOS current mirror and the NMOS current mirror at the output side of the structure. Essentially, this structure of combination of current mirrors with two of these

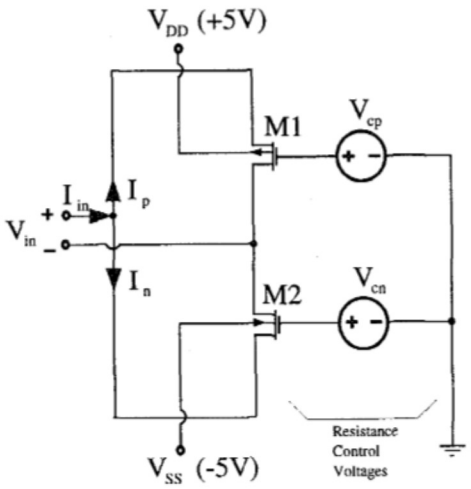

Figure 4: Circuit schematic of the CMOS bilateral linear floating resistor of configuration I.

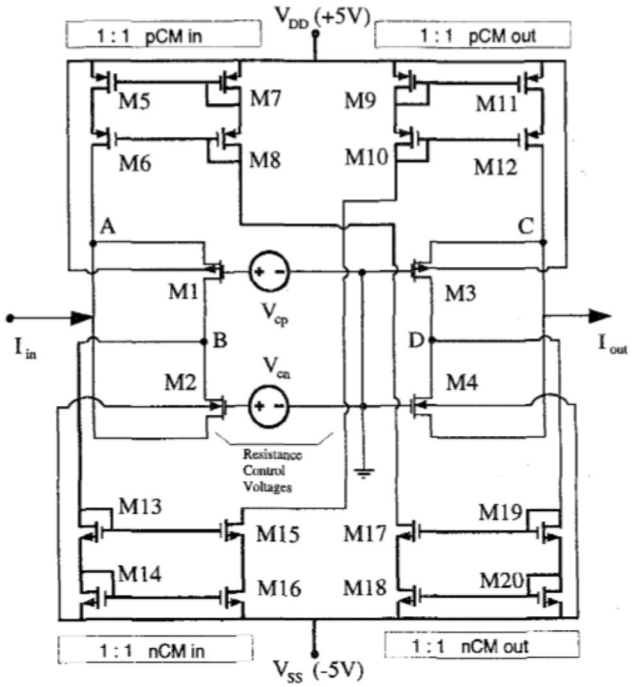

Figure 5: Circuit schematic of the CMOS bilateral linear floating resistor of configuration II.

two-transistor CMOS bilateral linear resistors gives the floating CMOS bilateral linear resistor shown in Figure 3.

The resistor blocks of the circuit schematic of configuration II (Figure 5) are made from blocks of Figure 4 and consist of four MOS transistors and two control voltage sources. The pair of MOS transistors M_1 and M_2 is connected as the bilateral resistor on the middle left of Figure 5 while the other pair of MOS transistors M_3 and M_4 is similarly connected to the middle right. These resistors are controlled by the commom voltage V_{cp} for the PMOS transistors M_1 and M_3 and by the voltage V_{cn} for the NMOS transistors M_2 and M_4 as illustrated in Figure 5. The substrates of all the PMOS transistors are connected to $V_{DD}(+5V)$ and that of all the NMOS transistors are connected to $V_{SS}(-5V)$. In the upper left corner, transistors M_5 - M_8 form a 1:1 PMOS cascode current mirror pCM_{in} and in the upper right corner transistors M_9 - M_{12} form a 1:1 PMOS cascode current mirror pCM_{out}. Similarly, in the bottom left corner, transistors M_{13} - M_{16} form a 1:1 NMOS cascode current mirror nCM_{in} and in the bottom right corner, transistors M_{17} - M_{20} form a 1:1 NMOS cascode current mirror nCM_{out}. The cascode current mirrors are used to achieve good current match between the input and output sides of the circuit. It should be noted that the nullators are only indirectly realized in Figure 5. In essence, with good operation of the current mirrors the drain voltage of M_{13} is transfered to the drain of M_{12} giving nullator type behavior.

Now we analyze the circuit of Figure 5 for the case of positive input voltage V_{in}; the other case results by symmetry. We will assume $V_{cp} < 2V_{th1} < 0$, $V_{cp} < 2V_{th3} < 0$, $0 < 2V_{th2} < V_{cn}$, and $0 < 2V_{th4} < V_{cn}$. As this forces $V_{cp} < V_{th1}$ and $V_{cp} < V_{th3}$ then M_1 and M_3 are operating in the Ohmic region [5] which guarantees the possibility of linearization. The drain current of M_{19} is mirrored to the drain current of M_6 to obtain the two I's and, similarly, the drain current of M_{13} is mirrored to the drain current of M_{12}.

4 Simulations

To verify the analysis, the two configurations of floating resistors were simulated with PSpice. The input voltage V_{in} was swept from $-5V$ to $5V$ and the total input current I_{in} is plotted in Figures 6, 7 and 8. Figure 6 shows the curves for the two-transistor configuration of Figure 4 with the control voltage V_{cn} as a parameter varied between 0 and 5 in $1V$ steps. Figure 7 shows the curves for the two-transistor configuration for $V_{cn} = 5V$ with channel length L_2 of M_2 as a parameter varying between 10μ and 90μ in 20μ steps.

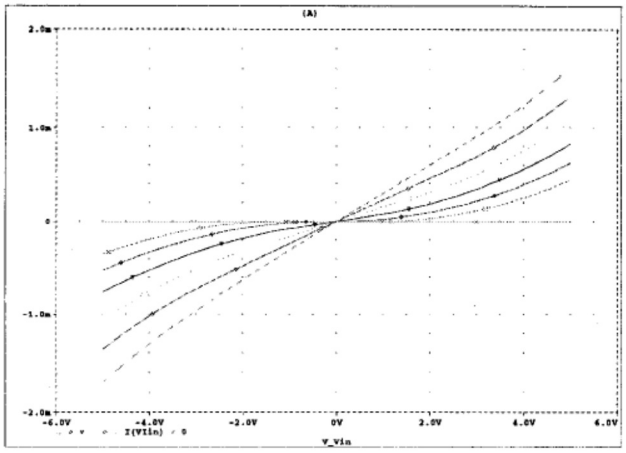

Figure 6: PSpice simulated curves for the two-transistor linear bilateral CMOS floating resistor of configuration I, with the top right curve for $V_{cn} = 5$V and decreasing in 1V steps to the bottom curve for $V_{cn} = 0$V.

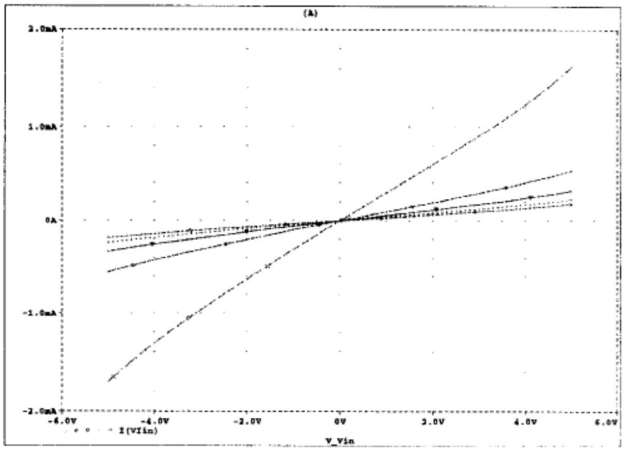

Figure 7: PSpice simulated curves for the two-transistor linear bilateral CMOS floating resistor of configuration I for $V_{cn} = 5$V, with the top right curve for $L_2 = 10\mu$ and increasing in steps of 20μ to the bottom curve for $L_2 = 90\mu$.

Figure 8 shows the simulated curves for configuration II of Figure 5 with the control voltage V_{cn} as a parameter varying between $0V$ and $5V$ in $1V$ steps to compare with Figure 6. Note that in Figures 6 and 8 we get the largest linear range for the resistor for $V_{cn} = 5V$, and as V_{cn} is decreased the linear range also decreases [5]. In Figure 7, we get linear resistors for all values of L_2. The current decreases as L_2 increases with the change expected as $1/L_2$ [5]. The curves of Figure 8 exhibit improved linearity compared to the curves of Figure 6. In all the simulations PSpice MOS level 2 parameters are used following MOSIS data from run N21H of 04/28/93 for which the key parameters are KP_n=5.048E-5, KP_p=1.908E-5, $VT0_n$=0.858, $VT0_p$=-0.889, λ_n=1.844E-2, λ_p=5.012E-2, ϕ=0.6, γ_n=0.198, γ_p=0.6289. The various transistor channel lengths L and channel widths W used in Figures 4 and 5 are tabulated in Table 1.

Table 1: Various channel lengths and channel widths for the MOS transistors of Figures 4 and 5.

Transistor Type	Transistor Number	Length L	Width W
NMOS	$M2$,$M4$,$M13$,$M14$, $M15$,$M16$ $M17$,$M18$,$M19$,$M20$	10μ	10μ
PMOS	$M1$,$M3$,$M5$,$M6$, $M7$,$M8$ $M9$,$M10$,$M11$,$M12$	10μ	27μ

5 Discussion

In this paper, we have presented two types of linear bilateral CMOS floating resistors for neural-type cell arrays. These resistors are floating versions of the resistors of [5, 16]. They offer an efficient usage of die area since the area consumed by them is much smaller compared to similarly sized directly implemented polysilicon or diffusion strip based passive resistors. Also, they are voltage controllable over a suitable dynamic range. Although these floating resistors were targeted for neural-type cell arrays to enable their use in both excitatory and inhibitory synapses, they can be used in other VLSI applications, such as cellular neural networks (CNNs) [17, 18].

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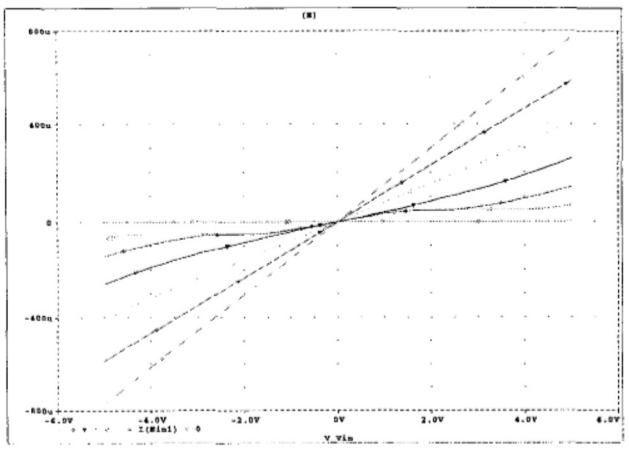

Figure 8: PSpice simulated curves for configuration II with the top right curve for $V_{cn} = 5$V and decreasing in 1V steps to the bottom curve for $V_{cn} = 0$V.

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