Linear Bilateral CMOS Resistor for Neural-Type Circuits

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***Abstract*—A previous CMOS bilateral linear resistor is analyzed and shown to be reducible from four to two transistors with improved linearity. This is developed for neural-type circuits to allow its use in emulating both excitatory and inhibitory voltage variable synapses. Simulation results using parameters of MOSIS transistors are presented to verify the theory.**

I. Introduction

In VLSI realization of Artificial Neural Networks (ANNs) [1] weights can be set by resistor values [2], in which case it is important to have good VLSI bilateral resistors. Besides that, if the weights are to be adapted it is advantageous to be able to adjust the resistances by controlling voltages. Consequently we present here a suitable class of simple VLSI bilateral, voltage adjustable resistors which are essentially linear. Previously in most standard MOS processes monolithic resistors were implemented as polysilicon or diffusion strips acting as passive devices but recently many authors have presented unidirectional linear active resistors containing MOS devices [3]–[13]. However, the nonlinearity of the MOSFET prohibits the use of large signals and limits its signal swing. To circumvent these limitations different circuit structures are introduced [4], [8], [10], [11]. Since these active resistor implementations usually take less die area as compared to passive resistors we present a generalized active linear bilateral enhancement-mode CMOS device resistor. This resistor is based on Youssef's [10], [11] circuit, which is a bilateral version of that of Moon [8]. This is improved in terms of elimination of two bias batteries which were inserted to insure that the diode-connected transistors operate in the linear region, while her theory is also improved. This improvement allows us to simplify the circuit from four transistors to two.

The circuit is presented in section II with resulting equations given in section III including substrate bias effects. In section IV design criteria for the two- and four-transistor circuits are derived. In section V, SPICE simulation results using MOSIS parameters for the two-transistor circuit are given.

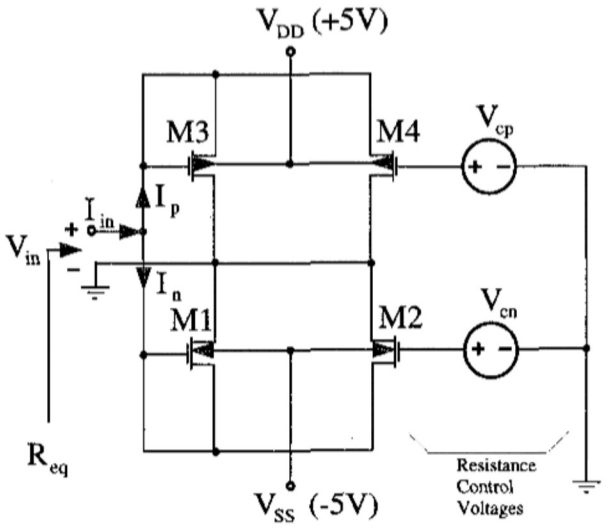

Fig. 1. The linear bilateral four-transistor CMOS resistor.

II. The Bilateral CMOS Resistor

The basic configuration of the linear bilateral CMOS resistor of Youssef [10], without the substrate offset bias voltage sources, is shown in Figure 1. It consists of four MOS transistors and two control voltage sources which could be voltage controlled sources (VCVS) for use in ANN weight adaptation. The pair of NMOS transistors M_1 and M_2 is connected as in the unilateral resistor of [8] to cover positive V_{in} while the other pair of PMOS transistors M_3 and M_4 is similarly connected to cover negative range of input voltage V_{in}. The resistance of the circuit is controlled by V_{cp} for the PMOS pair and by V_{cn} for the NMOS pair as illustrated in Figure 1. The substrates of the PMOS transistors are connected to $V_{DD}(+5V)$ and that of the NMOS transistors are connected to $V_{SS}(-5V)$.

The expression for the total input current I_{in} of the transistor circuit of Figure 1 is obtained by taking the sum of two currents through NMOS and PMOS pairs and

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is given by

$$I_{in} = I_n + I_p \tag{1}$$

where I_n is the current of the NMOS transistor pair and I_p the current of the PMOS transistor pair. The applied input voltage V_{in} can be either positive or negative in the range

$$V_{SS} \leq V_{in} \leq V_{DD} \tag{2}$$

and determines which of the NMOS or the PMOS transistors draw current. Note that when V_{in} is positive M_3 is turned off while the other transistors draw currents with M_1 in saturation. The presence of M_4 compensates for the substrate bias batteries used by Youssef and Moon. As in their cases, the nonlinearity of M_2 cancels that of M_1 but now also that of M_4 over an input voltage range determined by the control voltage V_{cn}. By symmetry the same effects occur for negative V_{in}.

III. Circuit Analysis

Here we analyze the circuit of Figure 1 for the case of positive input voltage V_{in}; the other case results by symmetry. From the start we will assume $V_{cp} < 2V_{th4}$ and $2V_{th2} < V_{cn}$ in order to guarantee the possibility of linearization. As this forces $V_{cp} < V_{th4}$ then M_4 is operating in the Ohmic region (see Appendix 1 for the proof). The drain of M_4 is at ground and its current, designated by I_{d4p}, for the Ohmic region of interest is

$$I_{d4p} = -\frac{KP_p}{2}\frac{W_4}{L_4}\left[V_{in}^2 - 2(V_{cp} - V_{th4})V_{in}\right](1 - \lambda_p V_{in}) \tag{3}$$

where W_4 is the transistor width, L_4 the length and λ_p the channel length modulation parameter of M_4. We also note the dependence of the threshold voltage V_{th4} of M_4 on the input voltage V_{in}

$$V_{th4}(V_{in}) = VTO_p - \gamma_p\left[\sqrt{\phi + V_{dd} - V_{in}} - \sqrt{\phi}\right] \tag{4}$$

Now Equation (1) becomes

$$I_{in} = I_{d1} + I_{d2} - I_{d4p} \tag{5}$$

where I_{d1} and I_{d2} are the drain currents of M_1 and M_2. There are three different regions based on the value of the input voltage V_{in} which determines the regions of operation for the NMOS transistors M_1 and M_2. The expressions for the total input current I_{in} for all three regions are rather complicated and space precludes to include the full equations for all the regions. Thus, we derive the expression for region I only in Appendix 2. Here we give the simplified forms suitable for design purposes by setting $\lambda_n = \lambda_p = 0$.

A. Region I: $0 \leq V_{in} \leq V_{th1}$

Here $V_{th1} = V_{th2}$ is the threshold voltage for the NMOS transistors M_1 and M_2 given as

$$V_{th1} = V_{th2} = VTO_n + \gamma_n\left[\sqrt{\phi - V_{ss}} - \sqrt{\phi}\right] \tag{6}$$

In this range of V_{in} M_1 remains in the cut-off region and M_2 is forced to the Ohmic region by assuming $V_{cn} > 2V_{th2}$. Their drain currents I_{d1} and I_{d2} are

$$\begin{aligned} I_{d1} &= 0 \\ I_{d2} &= \frac{KP_n}{2}\frac{W_2}{L_2}\left[2(V_{cn} - V_{th2})V_{in} - V_{in}^2\right](1 + \lambda_n V_{in}) \end{aligned} \tag{7}$$

where W_2 and L_2 are the channel width and length, KP_n is the transconductance parameter, λ_n the channel length modulation parameter and $V_{th2} = V_{th1}$ the threshold voltage for M_2 given by Equation (6). Dropping the λ_n dependence we get

$$\begin{aligned} I_{in} = &\left[\frac{KP_p}{2}\frac{W_4}{L_4} - \frac{KP_n}{2}\frac{W_2}{L_2}\right]{V_{in}}^2 \\ &+ \left[2\frac{KP_n}{2}\frac{W_2}{L_2}(V_{cn} - V_{th2}) - 2\frac{KP_p}{2}\frac{W_4}{L_4}(V_{cp} - V_{th4}(0))\right]V_{in} \end{aligned} \tag{8}$$

B. Region II: $V_{th1} \leq V_{in} \leq V_{cn} - V_{th2}$

For this region M_1 will be in saturation because the gate is connected to the drain and $V_{in} \geq V_{th1}$. Transistor M_2 will be in the Ohmic region for the assumed range of $V_{cn} > 2V_{th2}$. Thus, its drain current I_{d2} stays the same as in (7). Setting $\lambda_n = 0$ the drain current I_{d1} is written as

$$I_{d1} = \frac{KP_n}{2}\frac{W_1}{L_1}\left[(V_{in} - V_{th1})^2\right] \tag{9}$$

where W_1 and L_1 are the channel width and length.

The total input current I_{in} is

$$\begin{aligned} I_{in} &= \left[\frac{KP_n}{2}\left(\frac{W_1}{L_1} - \frac{W_2}{L_2}\right) + \frac{KP_p}{2}\frac{W_4}{L_4}\right]{V_{in}}^2 \\ &+ \frac{KP_n}{2}\frac{W_1}{L_1}{V_{th1}}^2 \\ &+ \left[-2\frac{KP_n}{2}\frac{W_1}{L_1}V_{th1} + 2\frac{KP_p}{2}\frac{W_2}{L_2}(V_{cn} - V_{th2})\right]V_{in} \\ &- \left[2\frac{KP_p}{2}\frac{W_4}{L_4}(V_{cp} - V_{th4})\right]V_{in} \end{aligned} \tag{10}$$

C. Region III: $V_{cn} - V_{th2} < V_{in}$

Transistor M_1 remains in saturation, therefore its drain current I_{d1} is the same as in (9). However M_2 goes into the saturation region and its drain current becomes

$$I_{d2} = \frac{KP_n}{2}\frac{W_2}{L_2}\left[(V_{cn} - V_{th2})^2\right] \tag{11}$$

TABLE I

Various SPICE simulated R_{eq} resistance values obtained with V_{cn} and V_{cp} = - V_{cn} + V_{thn} + V_{thp} as parameters, $L_2 = W_2 = L_4 = 10\mu$, $W_4 = W_2 * 2.646 = W_2 * \frac{KP_n}{KP_p}$, $V_{thn} = 1.173V$, $V_{thp} = -1.89V = V_{th4}(0)$.

Resistance Value R_{eq} in Ω	Control Voltage V_{cn} Parameter	Control Voltage V_{cp} Parameter
12.5K	12V	-2.16V
6.5K	3V	-3.16V
4.4K	4V	-4.16V
3.3K	5V	-5.16V

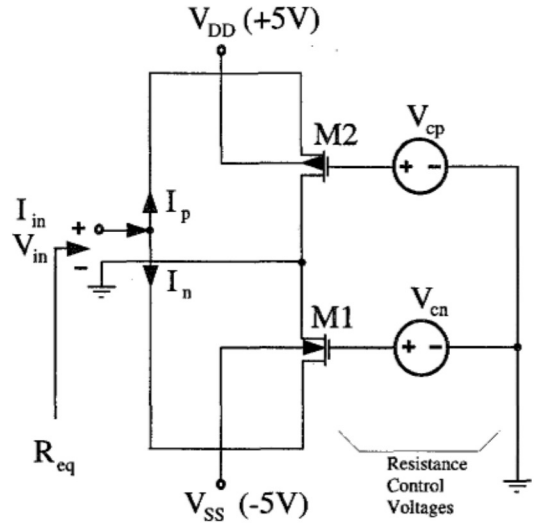

Fig. 2. The linear bilateral two-transistor CMOS resistor

Therefore the total input current can be written as

$$\begin{aligned} I_{in} &= \left[\frac{KP_p}{2}\frac{W_4}{L_4} - \frac{KP_n}{2}\frac{W_2}{L_2}\right] {V_{in}}^2 \\ &+ \frac{KP_n}{2}\left[\frac{W_1}{L_1}{V_{th1}}^2 + \frac{W_2}{L_2}(V_{cn} - V_{th2})^2\right] V_{in} \\ &+ \left[-2\frac{KP_n}{2}\frac{W_1}{L_1}V_{th1} - 2\frac{KP_p}{2}\frac{W_4}{L_4}(V_{cp} - V_{th4})\right] V_{in} \end{aligned} \tag{12}$$

IV. Design Criteria

By a proper choice of transistor parameters we show that almost linear relationships between the input voltage, V_{in}, and the input current, I_{in}, can be obtained in all regions. In order to reduce nonlinear effects, we eliminate the ${V_{in}}^2$ term in region II by forcing the following condition to hold

$$\frac{W_2}{L_2} = \frac{W_1}{L_1} + \frac{KP_p}{KP_n}\frac{W_4}{L_4} \tag{13}$$

At this point we note that if we choose $W_1 = 0$ we obtain linearity in all three regions and we have the advantage

TABLE II

Various SPICE determined R_{eq} values obtained with (L_2, L_4) and (W_2, W_4) as parameters and with V_{cn} = 5V and $V_{cp} = -V_{cn} + V_{thn} + V_{thp}$ = -5.16V

R_{eq} Ω	Parameter L_2	Parameter W_2	Parameter L_4	Parameter W_4
30K	90μ	10μ	90μ	26.46μ
25K	70μ	10μ	70μ	26.46μ
15K	50μ	10μ	50μ	26.46μ
10K	30μ	10μ	30μ	26.46μ
3.3K	10μ	10μ	10μ	26.46μ

that M_1 is deleted (and with it, by symmetry, M_3). Thus, the optimal design has

$$\frac{W_4}{L_4} = \frac{KP_n}{KP_p}\frac{W_2}{L_2} \quad and \quad W_1 = W_3 = 0 \tag{14}$$

The conductance for the two-transistor case in all three regions is

$$G_+ = KP_n\frac{W_2}{L_2}[(V_{cn} - V_{thn}) - (V_{cp} - V_{thp})] \tag{15}$$

Since V_{cn} and V_{cp} control the resistance in the first and third quadrant, respectively, we choose $V_{cp} = -V_{cn} + V_{thn} + V_{thp}(0)$ to balance the effect of differences in NMOS and PMOS threshold voltages over positive and negative ranges of V_{in}.

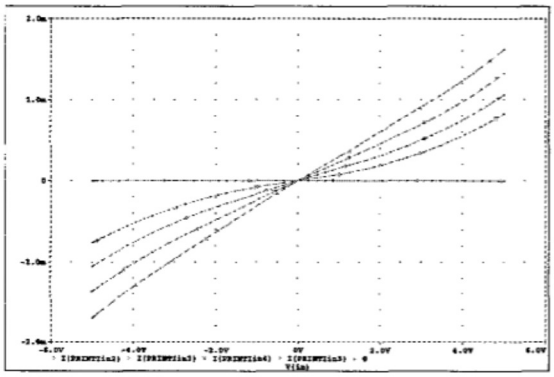

Fig. 3. PSPICE simulated curves for the two-transistor linear bilateral CMOS resistor of Figure 2 with the top right curve for V_{cn} = 5V and decreasing in 1V step to the bottom curve with V_{cn} = 2V.

V. Simulation Results

To verify the analysis, the two-transistor circuit of Figure 2 was simulated with PSpice. The input voltage V_{in} was swept from -5V to +5V and the total input current I_{in} is plotted in Figure 3. SPICE MOS level 2 parameters are used following MOSIS from run N21H of 04/28/93 for which the key parameters are

KP_n=5.048E-5, KP_p=1.908E-5, $VT0_n$=0.858, $VT0_p$=-0.889, λ_n=1.844E-2, λ_p=5.012E-2, ϕ=0.6, γ_n=0.198, γ_p=0.6289. The key design parameters used to get various resistor values are transistor length L and width W, as tabulated in Table II, and the controlling voltage V_{cn} which is varied from 3V to 5V in 1V steps as a global parameter (see Table I). As shown in Table II, resistance values from $R_{eq} = 3.3K\Omega$ to $30K\Omega$ are attained. The calculated value of resistance from equation (15) for $W_2 = 10\mu$, $L_2 = 10\mu$, $W_4 = 26.46\mu$ and $L_4 = 10\mu$ comes out to be $2.6K\Omega$ whereas the SPICE simulated value (from Table II) is $3.3K\Omega$. This discrepancy is due to the fact that the Early effect was neglected in the derivation of equation (15) for the purpose of simplification. Note also that for $V_{cn} = 2$V and 3V, at least one of the constraints $V_{cn} > 2V_{th2}$ and $V_{cp} < 2V_{th4}$ is violated, but the curves are very linear in region I.

VI. Conclusions

In this paper, we have presented a linear bilateral CMOS resistor for neural-type circuits. This resistor is an improved version of Youssef's resistor, which with the number of transistors now reduced to two (instead of four) has improved linearity. It offers an efficient usage of die area since area consumed by it is much smaller compared to similarly sized directly implemented polysilicon or diffusion strip based passive resistors. Also, it is voltage controllable over a suitable dynamic range. Although it is targeted for neural-type circuits to enable its use in both excitatory and inhibitory synapses, it can be used in other VLSI applications. Even though Equation (14) leads in theory to a linear circuit, the simulations show some nonlinear behavior. This nonlinear behavior is due to V_{th4} being a function of V_{in} and to the term $1+\lambda_n V_{in}$. The linear range of region II varies proportionally to $V_{cn} - V_{th2}$, as can be derived from Equation (10) by substituting $V_{cn} - V_{th2}$ for the maximum value of V_{in}, and, thus, region II linearity decreases with decreasing V_{cn}.

VII. Appendices

1) : Here we show that M_4 is in saturation for $V_{in} > 0$ and $V_{cp} < V_{th4}(0)$. Depending upon the value of V_{cp}, M_4 can be either in the Ohmic or in the saturation region. The gate to source voltage and drain to source voltage are given by

$$V_{gs} = V_{cp} - V_{in} \quad \text{and} \quad V_{ds} = -V_{in} \tag{16}$$

The condition for M_4 to operate in the Ohmic region is

$$0 \leq |V_{ds}| \leq |V_{gs}| - |V_{th4}| \tag{17}$$

which leads to

$$V_{cp} \leq V_{th4} < 0 \tag{18}$$

The condition for M_4 to operate in the saturation region is

$$0 \leq |V_{gs}| - |V_{th4}| \leq |V_{ds}| \tag{19}$$

which gives

$$V_{th4} \leq V_{cp} < 0 \tag{20}$$

But $V_{cp} < V_{th4}(0) \leq V_{th4}(V_{in})$ is needed to turn on the device for $V_{in} \geq 0$ (by Equation (4)), therefore M_4 cannot be in saturation.

2) : In terms of the full dependence upon V_{in}, the equation for the total input current I_{in} in region I is

$$\begin{aligned} I_{in} = & \left[\frac{KP_p}{2}\frac{W_4}{L_4} - \frac{KP_n}{2}\frac{W_2}{L_2}\right] {V_{in}}^2 + \left[2\frac{KP_n}{2}\frac{W_2}{L_2}(V_{cn} - V_{th2})\right] V_{in} \\ & - \left[2\frac{KP_p}{2}\frac{W_4}{L_4}\left(V_{cp} - (V_{th0} - \gamma_p\left[\sqrt{\phi + V_{dd} - V_{in}} - \sqrt{\phi}\right])\right)\right] V_{in} \\ & - \left[\lambda_p\frac{KP_p}{2}\frac{W_4}{L_4} + \lambda_n\frac{KP_n}{2}\frac{W_2}{L_2}\right] {V_{in}}^3 + \left[2\lambda_n\frac{KP_n}{2}\frac{W_2}{L_2}(V_{cn} - V_{th2})\right] {V_{in}}^2 \\ & - \left[2\lambda_p\frac{KP_p}{2}\frac{W_4}{L_4}\left(V_{cp} - (V_{th0} - \gamma_p\left[\sqrt{\phi + V_{dd} - V_{in}} - \sqrt{\phi}\right])\right)\right] {V_{in}}^2 \end{aligned} \tag{21}$$

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