Synchronization of Neural-Type Cells

A. Hodge, M. Zaghloul, and R.W. Newcomb
A. Hodge and R.W. Newcomb: University of Maryland College Park
Microsystems Laboratory, Electrical Engineering Department
M. Zaghloul: The George Washington University
Electrical Engineering Department

Abstract:

In this paper the synchronization of several neural-type cells is considered. Recently there has been considerable interest in the synchronization of chaos generators. Since the neural-type cells have been shown to support chaos, their synchronization for this purpose is introduced by using a synchronizer which acts to control the load lines on the synchronized cells. The resulting synchronization is discussed with special reference to synchronization of chaos in neural networks constructed from these CMOS cells.

I. Introduction

Use of the neural type cell (NTC) as the primary subcircuit for the generation of pulses in pulse coded neural networks has been of interest to many since its introduction [1] as the basic component in an integrable MOS neuristor. The NTC is an electronic circuit that produces pulse coded oscillations once a certain dc threshold level has been reached. The pulse-like oscillations are dependent upon nonlinear hysteresis characteristics generated through feedback [2]. To produce oscillations, it is necessary to drive the load line of the NTC through the vertical sides of its hysteresis. Driving the load line through the steep edges of the hysteresis causes the system to be unstable. This instability causes the neural type cell to oscillate. If the intersections do not occur at the steep edges, the neural type cell's driving point will stay at that intercept, and no oscillation will result. The NTC's load line is in no way affected by changes to the input voltage; however, the size and shape of the hysteresis varies with the input to the NTC [2]. As the input is increased, the width of the hysteresis shrinks as it moves to the left. The width of the hysteresis plot controls the range of voltages over which the output oscillates. As the hysteresis becomes more and more narrow, the oscillating range of voltages decreases over time.

Figure 1 represents the CMOS circuit for the basic Neural Type Cell (NTC). This circuit is made up of three transistors, three resistors, and a load capacitor. As the input voltage of the NTC increases above a certain dc threshold level, the output voltage signals begin to oscillate. This resulting oscillation is nonlinearly proportional to the input level [3]. Thus, the neural type cell can be said to encode input stimuli (voltage) into pulse rates of an output signal.

There are a number of limitations to the basic neural type cell. As such, various changes to the design of the neural type cell have been made [3][4][5]. One design limitation is that the resistors used in the basic NTC make the circuit extremely large. The size limitation is overcome by using MOS transistors in lieu of resistors. A second limitation is that the range of oscillations for the basic NTC is relatively small. To increase the range of oscillations, a nonlinear resistor made up of three transistors is used to replace the load resistor, Rl, of figure 1. These three transistors are a combination of 2 p-type transistors and one n-type transistor on the right of Figure 2. The n-type transistor determines which p-type transistor will operate in the triode region or the saturation region. Although the shape of the hysteresis continues to change with varying inputs, the oscillating range of the NTC is increased since the load line can be made to pass horizontally through the steep edges easily. The resulting modified neural type cell is made up of nine MOS transistors [3].

Modifications to the NTC have been made which allow for coupled NTCs to generate chaotic behavior [5]. The philosophy of these modifications is as follows: the production of chaotic behavior can be realized by modulating the oscillations of one NTC by those of another, but in such a way that the coupling is always different. This can be controlled by output capacitance and the differences in pulse repetition rates of the two NTCs' self oscillations. The chaos that is shown to

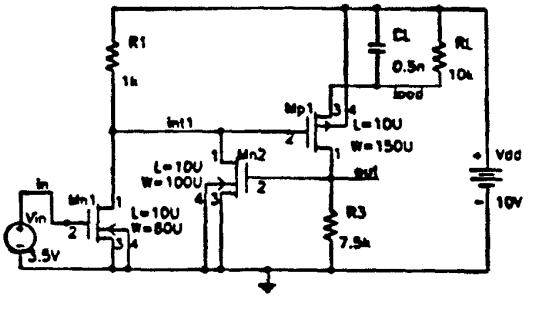

Figure 1. The Basic Neural Type Cell.

exist in the coupled neural type cells occurs in the number of pulses occurring in repetition intervals rather than in amplitude changes normally used to describe chaos. Figure 2 shows the design of one Neural Type Cell as described by [5]. Here, we use CMOS transistors which can be fabricated by VLSI techniques via the MOSIS facility. The Spice parameters for the transistors we use are as follows: Kpn= 5.048E-5, Kpp= 1.908E-5, VTOn= 0.858, VTOp= -0.889, LAMBDAn= 1.844E-2, and LAMBDAp= 5.012E-2. These parameters were obtained from transistor data received after the MOSIS run N21H of 04/28/93.

In this paper, using the modified circuit of Figure 2 introduced in [5], we show a scheme of synchronizing the chaotic neural type cell. Section II and Figure 4 describe the synchronization technique. Section III shows the simulation results. The conclusion is given in section IV.

II. Synchronizing the Neural Type Cells

Figure 3 shows the design of one pair of coupled neural type cells. The coupled pair of NTCs give the chaotic responses described in section (I). Here, the output of each cell is connected to the control node, gate Mn5, of the load, RL, of the other NTC. The two neural type cells are identical with the exception that CL1 = 0.5 nFd and CL2 = 0.05 nFd and dynamics is added at the output node via Cout. Figure 5 shows the chaotic like response of the pair of coupled NTCs.

Three pairs of coupled Neural Type Cells are used in emulating the synchronization technique. Figure 4 shows the scheme by which the 3 pairs of NTCs are connected. Each pair of coupled NTCs is made up of two all MOS Neural Type Cells as shown by Figure 3. In total, six Neural Type Cells are used in the design of this circuit. Each Neural Type Cell is similar to that shown in figure 2. The first pair of coupled Neural Type Cells is identical to that shown in Figure 3. It is made up of 2 NTC's labeled cell #1 and Cell #2 respectively. The second and third pairs of coupled Neural Type Cells differ from the first in only one transistor, Mn5. These pairs of NTCs are connected via the Mn5 transistors, of cells 4 and 5, which are half the size of the equivalent transistor in the original design of the coupled NTC. The neural type cells in the second pair are labeled cell #3 and cell #4. The NTCs in the third pair act as the synchronizer for the circuit. They are labeled cell #5 and cell #6. The second pair of NTCs differ from the first and third in that the capacitor of cell #3 has a value of .1nFd instead of the .5 nFd value used for the equivalent capacitors of cells #1 and #5. This change serves to alter the frequencies between the NTCs.

The philosophy behind the synchronizer is that it adjusts the load line of cell #4 in such a way that it will trigger pulses in synchronism with the chaotic oscillations of cell #1. The output of cell number 2 is connected to the voltage inputs of cells 3 and 5. The Mn5 transistors of cells 4 and 5 are connected in parallel from source to ground. When the input voltages of all cells are equal, the current flowing through the parallel transistors is equal to that flowing through the equivalent Mn5 transistors of the other cells. Changes to the amount of current flowing through these transistors are made by altering the input voltage of Cell #6. When all of the circuit's neural-type cells have equal input voltages, all pairs of NTCs operate and produce the chaotic oscillations described in section (I).

III. Simulation Results

Figures 5a and 5b show the output oscillations of the two coupled neural type cells described in [5] and shown in Figure 2. In these figures, we see that chaotic-like oscillations occur in the output of the second neural type cell shown in Figure 2. The oscillations of the second NTC are strongly driven by those of the first.

Figures 6a - 6e present the outputs of the neural type cells arranged in the manner described by figure 4. Figures 6a, 6b, and 6c show the oscillations produced in cell #1, cell #3, and cell #5, respectively. Figures 6d, 6e, and 6f show the oscillations of cell #2, cell #4, and cell #6 respectively. In the synchronized neural type cells shown in figure 4, the output of cell 2 (as shown by figure 6d) is used to drive cells 3 and 5. The outputs of cells 3 and 5 (as shown by figures 6b and 6c respectively) are used to drive cells 4 and 6. The resulting outputs in cells 4 and 6 are chaotic. The chaos said to exist in these cells is like that described by [5].

IV. Discussion

In the above we have presented a series of chaos supporting neural type cells that can be used for the purpose of instituting the synchronization of chaos generators. The philosophy is that by varying the input voltage of cell #6, the pair of neural type cells created by cells 5 and 6 can act as a synchronizer that adjusts the load line of cell #4. This allows cell 4 to trigger pulses that are in synchronism with the chaotic oscillations of cell

#1. The chaos that apparently exists in the outputs of cell 4 and cell 6 occurs in the number of pulse repetition rates. However, it remains to be proven whether or not chaos is actually generated.

By investigating the synchronization of neural-type cells, we have made further advances to the creation of neural-type pulse coded devices. Further studies involve creating the inverse to this system. The inverse of the neural type cell synchronizer can be used to decode an original signal passed through the non-inverted device. Lastly, the circuit is set up for VLSI optimization. Future work involves determining the circuit's size optimization and fabricating its VLSI chip.

V. References

[1] C. Kulkarni-Kohli and R.W. Newcomb, "An Integrable MOS Neuristor Line", Proceedings of the IEEE, Vol. 65, No. 11, November 1976, pp. 1630 - 1632.

[2] N. El-Leithy and R.W. Newcomb, "Hysteresis in Neural-Type Circuits", Proceedings of the 1988 International Symposium on Circuits and Systems, Espoo, Finland, June 1988, pp. 993 - 996.

[3] Suan Tsay, M. De Savigny, N. El-Leithy, and R. Newcomb, "An all MOS Neural Type Cell", Proceedings of the 34th Midwest Symposium on Circuits and Systems, Monterey, CA, May 1991, pp. 776-779.

[4] G. Moon, M. Zaghloul, R. Newcomb, "VLSI Implementation of Synaptic Weighting and Summing in Pulse Coded Neural-Type Cells", IEEE Transactions on Neural Networks, Vol. 3, pp. 394 - 403, may 1992.

[5] A. Hodge and R.W. Newcomb, "VLSI Chaos Generation, Hysteresis, and the Neural Type Cell", The World Congress on Neural Networks, Vol. 1, pp. 250 - 253, July 17 - 21, 1995.

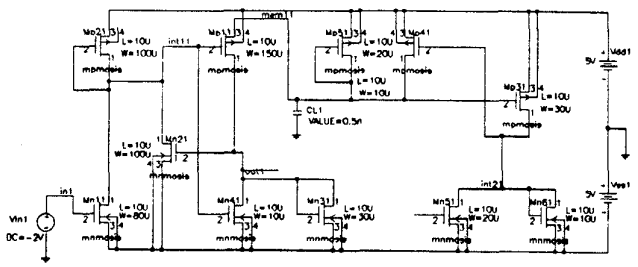

Figure 2. An all MOS Implementation of the Neural Type Cell.

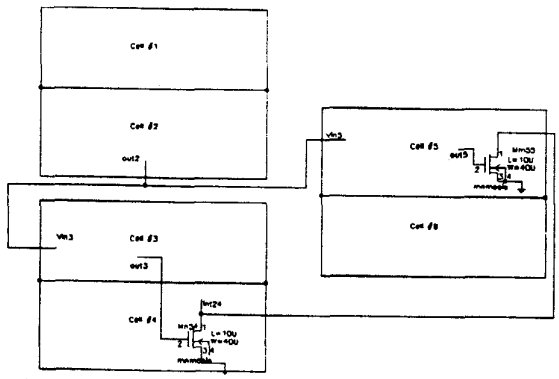

Figure 4. Diagram of two pairs of Neural Type Cells with a synchronizer.

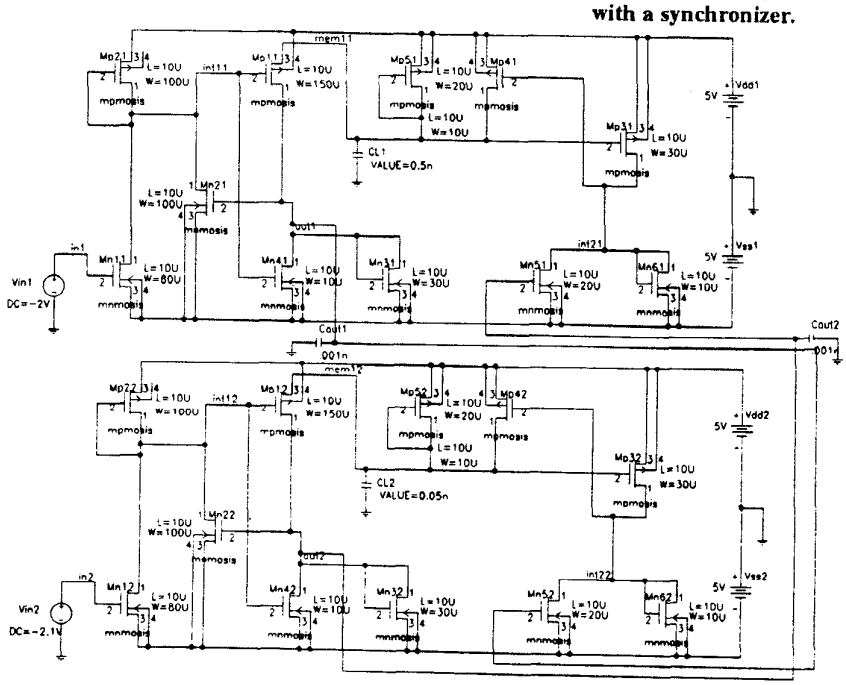

Figure 3. The coupled Neural Type Cell.

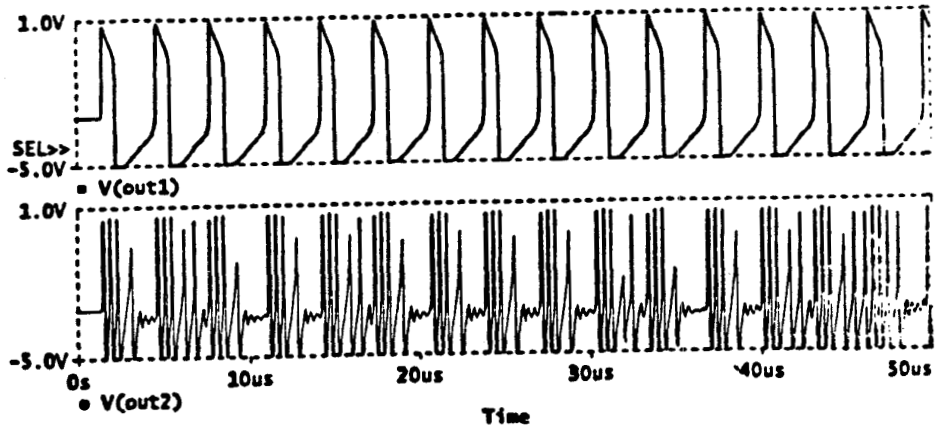

Figure 5. Chaotic-like response from the coupled Neural Type Cells of Figure 3.

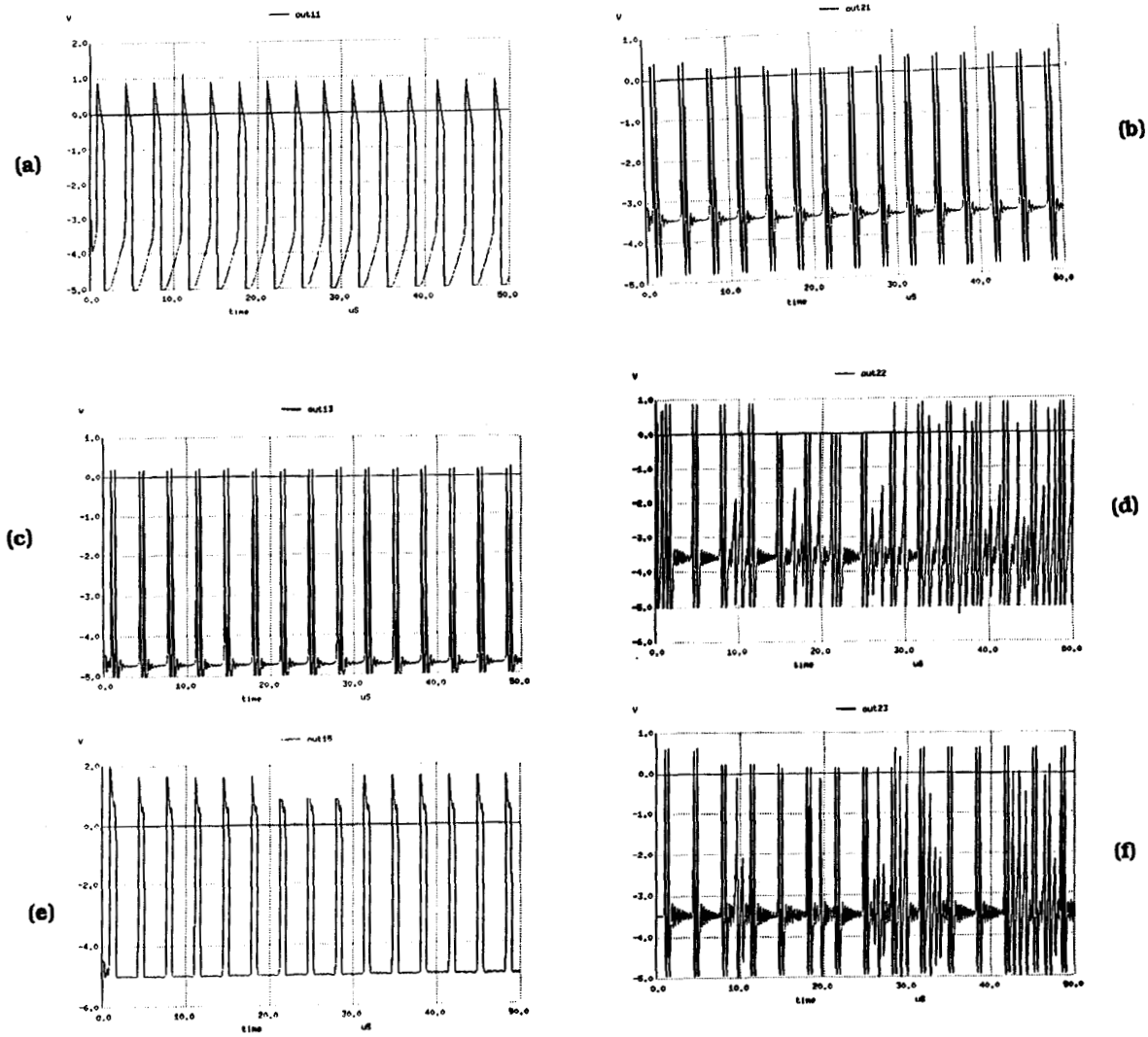

Figure 6. **Output oscillations for the synchronized Neural Type Cells of Figure 4. (a) Output oscillations for Cell 1 (b) Output oscillations for Cell 2, (c) Output oscillations for Cell 3, (d) Output oscillations for Cell 4, (e) Output oscillations for Cell 5, (f) Output oscillations for Cell 6.**