A CMOS PWL Fuzzy Membership Function

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Abstract: The membership function, classically constructed from piecewise linear (PWL) functions, is one of the most important components in fuzzy neural systems. Here we give an improved current mode CMOS circuit suitable for design of fuzzy membership PWL functions. The circuit with bi-directional input is based upon an improved current mirror and is suitable for VLSI fabrication via the MOSIS CMOS process.

1 Introduction

Fuzzy theory was introduced in the literature thirty years ago by L.A. Zadeh [1]. Since then, Fuzzy concepts, have been successfully applied in many fields of technology. Fuzzy logic and the machine that uses it, brings human made systems closer to men's way of thinking and it reminds us that "gray is O.K." and "everything is a matter of degree" [2, pp. 235]. However, missing from this human (fuzzy) logic system is the learning process. In this regard, a neural net can act like the eyes and ears of a fuzzy system whose rules change (learn) with experience [2, pp. 203]. An important part of this fuzzy neural system is an analog fuzzifier, more in tune with neural net systems than digital computers, to classify analog input signals [3]. This classification of analog input signals is done by membership functions. In this regard an analog membership function, based upon an improved current mirror [4], is presented here in a piecewise linear form suitable for the fuzzy-neural systems [5].

2 Objective and Principle Idea

2.1 Piecewise Linear Function

The principle objective is to construct a PWL function (**Io**) with arbitrary domain, range, and number of Break Points. It is also desired to be able to alter this PWL function by changing the slope of the linear segments as well as by changing the break points along the domain (**Ii**), independently of each others. Furthermore, it is desired to be able to shift the entire PWL function to anywhere in the plane without changing it's shape.

The principle idea in constructing this PWL function is to algebraically superimpose several elementary functions together. These elementary functions are themselves PWL functions with only one break point that separates itself into two linear segments, a linear segment with zero slope and another one with nonzero slope. The building blocks for the construction of any PWL functions are the four elementary functions, where m>0.

$$E_R^+(I_i,I_b,m) \equiv 0 \cup m(I_i - I_r) = \begin{cases} 0 & I_i \le I_b \\ m(I_i - I_b) & otherwise \end{cases} \quad (1)$$

$$E_L^-(I_i,I_b,m) \equiv 0 \cap m(I_i - I_b) = \begin{cases} m(I_i - I_b) & I_i \le I_b \\ 0 & otherwise \end{cases} \quad (2)$$

$$E_L^+(I_i,I_b,m) = -E_L^-(I_i,I_b,m) \quad (3)$$

$$E_R^-(I_i,I_b,m) = -E_R^+(I_i,I_b,m) \quad (4)$$

The graphical presentations of the four elementary functions are given in Fig. 1(a)-(d). When N of the above elementary functions are superimposed together, it is the position of the break points (Ib) and the slope (±m) of the slanted piece of these N elementary functions that decides the shape and the form of the final composed PWL function. Furthermore, the maximum number of the break points in the composed PWL function can be chosen equal to the number of the elementary functions being used.

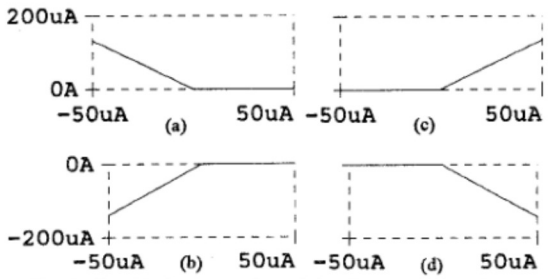

Fig. 1. Graphical presentation of the elementary functions, (a) E(+L), (b) E(-L), (c) E(+R), (d) E(-R); Ib=0

2.2 Piecewise Linear Membership Function

Fuzzy membership functions are customarily constructed from PWL functions with bipolar or unipolar input domain, depending on the application, and a range that extends from zero to one on the output axis. Therefore, by restricting the output range of any circuit that produces a PWL function with arbitrary

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domain, range, and break points to the set of zero to one will make it a PWL fuzzy membership function generator.

3 Circuit Construction of Elementary Functions

3.1 Current Mirrors

Current mirrors are the building blocks of the circuits for elementary functions. Figure 2 (a1,a2) shows the simple PMOS and NMOS current mirrors while parts (b1,b2) shows the same current mirrors in a cascode form that decreases minimum output voltage and increases the output resistance for a higher performance [6, p.224, 232]. Finally in the same figure parts (c1,c2) present Regulated Cascode Current Mirrors that have, in comparison to the standard cascode current mirrors, the minimum output lowered by about 30 to 60 percent while the output conductance and feedback capacitance are lowered by about 100 times [4].

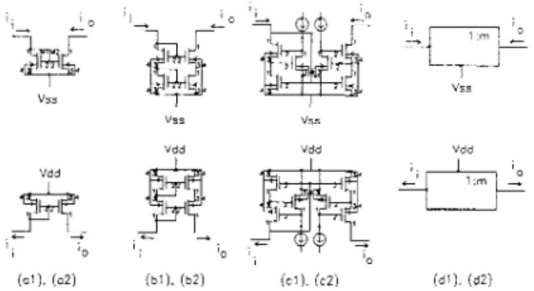

Fig. 2. Current Mirrors, NMOS (top) and PMOS (bottom), (a) simple, (b) cascode, (c) regulated cascode, (d) symbols used for NMOS and PMOS Current Mirrors (CM)

3.2 Block Diagram and Current Analysis

The block diagram constructions of the elementary functions E(+R) and E(-L) using current mirror symbols and current sources are shown in Fig. 3 (a) and (b). The design considers a bipolar input current (Ii). In Fig. 3(a), the bias current (Ibias) is added to the bi-directional input current (Ii) to produce I1a (=Ii+Ibias). Current I1a is a monodirectional current suitable to go through the first stage NMOS current mirror to produce an equal output current (I2a) on the opposite side. Subsequently, an equal bias current (Ibias) and a break point current (ib_a) are subtracted from the output current I2a to produce I3a=Ii-Ib_a . This current (I3a) is the same as the bi-directional input current Ii shifted down by Ib_a (break point current) though it would shift upward if Ib_a is negative. Note, that only the positive component of this shifted bi-directional current (I3a) will go through the next stage PMOS current mirrors and produces an output current that is an E(+R) elementary function with the break point equal to Ib_a and a slope of m, which is the transistors aspect ratios of the PMOS current mirror. Similarly, in Fig. 3(b) the current is I3b=-(Ii-Ib_b), and only the negative component of Ii-Ib_b, will go through the next stage's NMOS current mirrors and produces an output current E(-L). Equations (3),(4) show that the two elementary functions, E(+L) and E(-R), can be obtained from the other two E(+R) and E(-L) simply by reversing the direction of the currents. This is done in Fig. 3(c),(d) by adding the third stage current mirrors to obtain elementary functions E(-R) and E(+L), respectively.

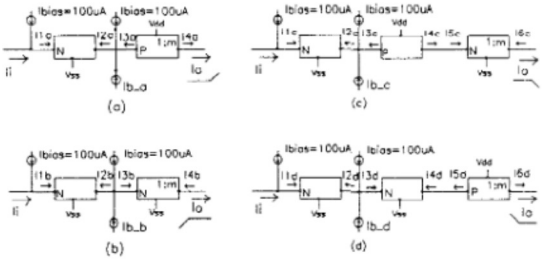

Fig. 3. The Block diagram for construction of elementary functions, (a) E(+R), (b) E(-L), (c) E(-R), (d) E(+L)

3.3 Effect of Different Current Mirrors in Building an Elementary Function

The elementary function E(-L) given by Eq. (2) and Fig. 3(b) is constructed in three different forms using the three different NMOS current mirrors presented in Fig. 2. The schematic CMOS transistor circuits are presented in Fig. 4 . These are compared using the two error indices: the magnitude of the offset output current from zero when the input current is equal to the set break point Ib (set to zero in this case) and the magnitude of the offset input current from the set breakpoint Ib when the output current reaches zero magnitude. These two error indices are called Io-offset and Ib-offset, respectively. The comparison between the results, Table. 1, shows that the circuit using the regulated cascode gives much less output current offset at the breakpoint (Io-offset), and much less input current offset for the break point itself (Ib-offset), when compared with the other two cases.

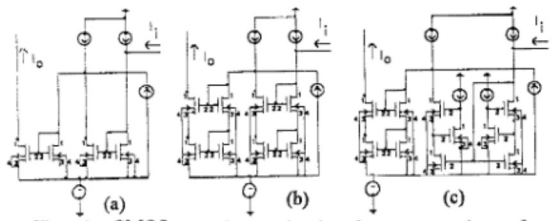

Fig. 4. CMOS transistor circuits for construction of elementary function E(-L), using (a) simple CM, (b) cascode CM, (c) regulated cascode CM

	Simple CM	Cascode CM	Regulated Cascode CM
Io-offset	3.8 uA	1.1 uA	.45 uA
Ib-offset	12.5 uA	4.9 uA	1.9 uA

Table 1. Performance comparison of an elementary function circuit using three different current mirrors

4 PWL Functions Circuit Using Elementary Functions

Figure 5 shows the block diagram of the four elementary functions, given earlier, integrated together in a parallel form. Since all four elementary functions share some of the same components, such as input current (Ii), bias current (Ibias), and an NMOS current mirror, at their input stage, therefore, the input stage of all four elementary functions has been integrated into one. This single common stage for all four elementary functions uses an NMOS current mirror with four output stages, supplied to each elementary function block. Furthermore, all bias currents (Ibias) are provided through a PMOS current mirror with multiple outputs. In this figure (5), beside the block diagrams of the four elementary functions, there are also current sources Ishift(x) at the input stage and Iref(y) at the output. These two current sources are respectively responsible to shift the entire PWL function along the x-axis (Ii) as well as the y-axis (Io), equal to the magnitude of their current values. The four current sources Ib_a, Ib_b, Ib_c, and Ib_d may be set independently to determine the position of the break points in the PWL function. The position of these breakpoints will be the magnitude of the current of these four sources. The slope of each linear segment can be determine by the transistor aspect ratios of the last current mirror of each elementary function block diagram. A PWL function with four multiple linear segments of different slopes is obtained by the CMOS transistor circuit of Fig. 4 and is given in Fig. (6).

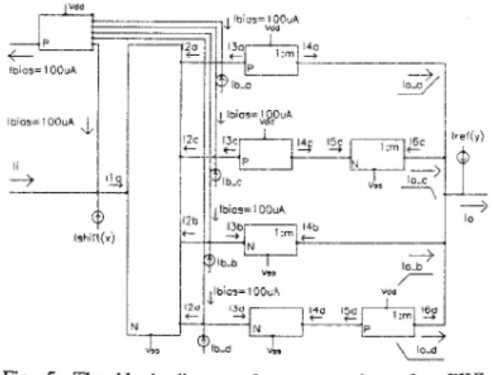

Fig. 5. The block diagram for construction of a PWL function

5 PWL Fuzzy Membership Functions With Single Slope

The continuous fuzzy membership functions that are considered here are the triangular and the trapezoidal type with domain that can have positive and/or negative values. These fuzzy membership functions can be classified as NB, NM, NS, ZO, PS, PM, and PB (P=positive, N=negative, S=small, M=medium, B=big, ZO=zero) depending on the position of the fuzzy subset in the domain [7, p.160]. All the above PWL fuzzy membership functions can be created by using only two of the elementary functions presented in the previous section. Figure 7 gives a block diagram similar to the one used in the previous section with two of the unneeded elementary function blocks omitted and a diode added in series to the output to avoid the membership function to go negative. The slopes of the side lines of the membership function are determined by the transistor aspect ratios used in the last current mirror of the corresponding elementary function. The break points are decided by the values of the Ib_b, and Ib_c current sources. Each break point position can be kept free to be changed by keeping the current source that controls it or be fixed in the transistor designed circuit by eleminating the controling current source while integrating it's current amount into the bias current of that node. The triangular and trapezoidal fuzzy membership functions produced by the CMOS transistor circuit of Fig. 7 are presented in Fig. 8. The NB, and PB membership functions are produced by shifting the ZO membership function to the far left and the far right by changing the value of the current source Ishift(x). The NM, NS, etc. membership functions can be produced similarly by shifting ZO.

6 PWL Fuzzy Membership Functions with Selectable Slopes

The last current source in each elementary function block diagram decides the slope of the slanted linear piece. In order to have multiple slopes to select from, the last output current mirror is replaced with a current mirror with multiple output where each output has a different aspect ratio in the block diagram of Fig. 9. Note that by having only three outputs on each last

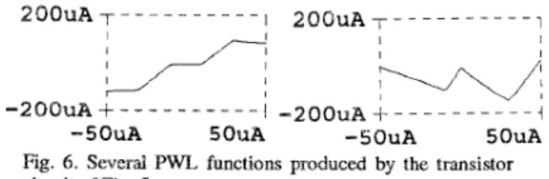

Fig. 6. Several PWL functions produced by the transistor circuit of Fig. 5.

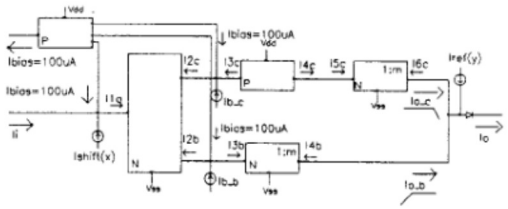

Fig. 7. the block diagram for construction of PWL fuzzy membership function (triangular and trapezoidal)

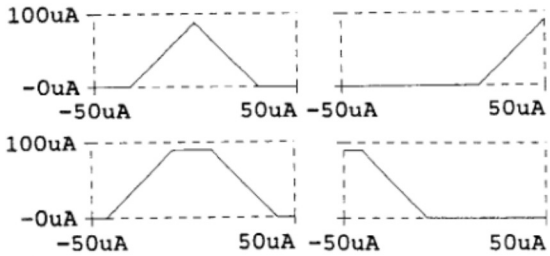

Fig. 8. Several PWL Fuzzy membership functions produced by the CMOS transistor circuit of Fig. 7. NB and PB are produced by shifting ZO to the left and right, respectively

current mirror with different aspect ratios, one can configure up to 8 (2 power 3) different slopes on each side of the fuzzy member and the total of 64 (8 times 8) different fuzzy members (combination of different slopes on both side). Considering the shifting ability of these 64 ZO membership functions that can produce NB, PB, etc., as well as changing between the trapezoid and triangular form by changing the Ib current sources, one can see the unlimited number of Π, Δ, Ø, I, S, Z, /, \, U type [3], [5], [8] membership functions this circuit is capable of producing with a high accuracy. Some assorted membership functions produced by the transistor circuit of Fig. 9 are given in Fig. 10.

7 Conclusions

In this paper, an improved current mode CMOS circuit suitable for design of fuzzy membership PWL functions is presented. This circuit utilizes an improved current mirror with lower output conductance and feedback capacitance. Some of the special features associated with these designs are generation of PWL membership functions with multiple slopes, decoupled slope and break point settings, arbitrary shifting along x-axis, reduced output error, and bi-directional input current. In general, the proposed circuit can be used to generate any four quadrant PWL function with all the mentioned features in addition to the arbitrary shifting along the y-axis.

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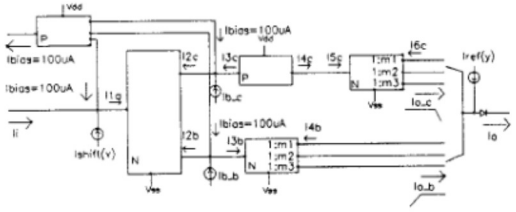

Fig. 9. The block diagram for construction of PWL fuzzy membership function with selectable slopes

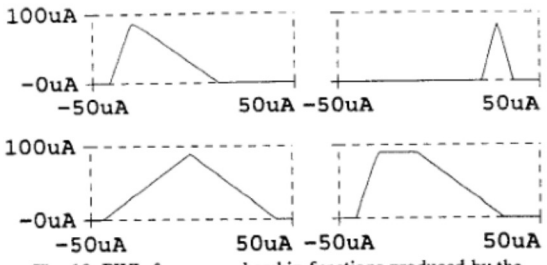

Fig. 10. PWL fuzzy membership functions produced by the CMOS transistor circuit of Fig. 9 with multiple slopes and shifted positions