A BiCMOS Binary Hysteresis Chaos Generator

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Abstract:

A previous op-amp RC circuit which was proven to give chaotic signals is converted to a BiCMOS design more suitable to integrated circuit realization. The structure results from a degree two differential equation which includes binary hysteresis as its nonlinearity. The circuit is realized by differential (voltage to current) pairs feeding two capacitors, which carry the dynamics, with the key component being a (voltage to current) binary hysteresis circuit due to Linares.

I. Introduction

One of the fascinating application areas of chaos is in coding for secure communication in which chaos is synchronized between sender and receiver [1]. Hardware implementation of this coding rests upon having hardware that consists of accurately reproducible chaos generators [2][3]. And although our experience is that it is rather easy to modify oscillator and related circuits to obtain chaos it is more difficult to obtain good design formulations. Thus there has recently been an interest in circuits for generating chaos and this has led to a sequence of special issues of the IEEE devoted to the topic [4]. Much of the circuit results rest upon a study of the circuit due to Chua and first presented by Matsumoto [5]. However, there have been other philosophies, promising ones among which are those for which designs are based upon hysteresis [6][7][8]. A primary one among this class is our previous circuit using binary hysteresis [9][10]. This circuit has the advantages that it is only degree two, readily proven to give chaos, with its principles of operation conceptually easy to grasp. Previous realizations used operational amplifiers and could be considered voltage-mode. But for VLSI realization current-mode structures are usually more convenient, so here we give a different realization that is essentially current-mode, being dependent upon differential pair current outputs. Key to this is the design of the binary hysteresis with a current-mode device; fortunately for our designs such a device has recently been introduced by Linares [11].

In the following we review the principle of operation of the generic degree two binary hysteresis chaos generator, review the reason it yields chaos and then give circuit realizations in the form suitable for VLSI construction using the most recent fabrication technology of BiCMOS (Bipolar-Complementary Metal Oxide Silicon). For this latter we first introduce an ideal normalized realization of the describing equations and then denormalize to values that correspond to devices constructable by the standard MOSIS VLSI analog circuit BiCMOS fabrication process. The circuit diagrams and curves

presented were all obtained using the Design Center CAD package associated with PSpice [12] and, consequently, adhere to its drawing conventions as well as to the standard SPICE nomenclature for labeling circuit components (in particular D represents a diode, F a bidirectional current mirror, G a voltage controlled current source; M and Q denote MOS and bipolar transistors, respectively).

II. The Basic Binary Hysteresis Chaos Generator

The basic philosophy of the binary hysteresis chaos generator can be seen by observing Fig. 1 where there are two half-planes that overlap and are separated by binary

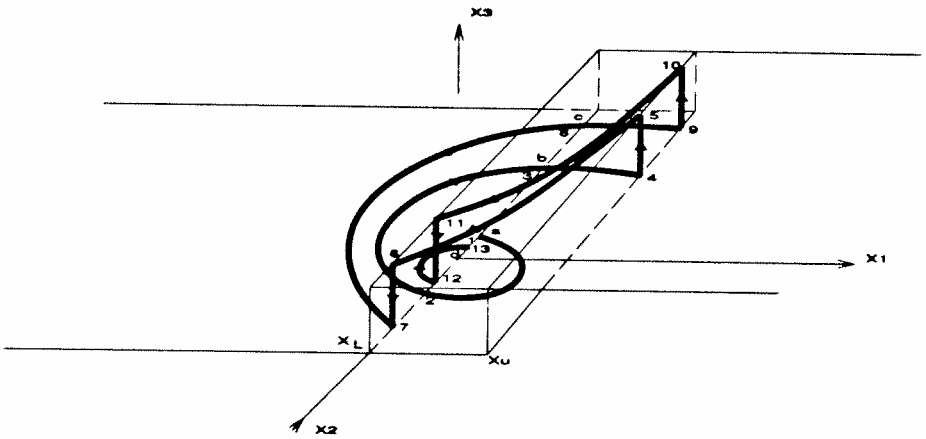


Figure 1
Trajectories in the Hysteresis Planes Illustrating a Set of Returns Satisfying d<a<b<c

hysteresis. In each plane are a set of spiral trajectories arising from a degree two unstable linear system. These two sets of trajectories are connected through the binary hysteresis to form the chaos generator's full set of trajectories. As an example of a tracing we can start at point 1, which is also labeled a, spiral in the lower plane through the points 2 and 3 (also labeled c) to 4 at which point a jump via the hysteresis is made to 5 and along an upper plane trajectory to 6 and then jump down to 7, spiral to 8=c to 9, jump up to 10, spiral to 11, jump down to 12 and on to 13=d, continuing on and on forever. A very important point is that the two sets of trajectories are, rather easily, designed to force d<a<b<c so that there is a return on the upper half of the x_2 axis inside of the start point in such a way that a period three return map is obtained for the maximum of the x_2 axis projection of the trajectory. The system stems from an idea mentioned by Rössler [13] and was earlier proven to be chaotic [10, p. 330] by direct application of the basic Li-Yorke theorem on "period three implies chaos" [14]. An important practical, as well as theoretical, aspect of the system is that the same degree two subsystem can be used to

generate the spirals in the upper and the lower hysteresis half-planes with the binary hysteresis parameter serving to change the origin of the spirals in the upper half-plane from those in the lower. Thus, rather than using degree four, or even three, this system can be realized as a degree two system!

Although there are uncountably many choices of parameters which will yield chaos, in normalized form the following two differential equations have been rigorously proven to give chaos.

$$\frac{dx_1}{dt} = x_2 + a_1 h(x_1) \tag{1a}$$

$$\frac{dx_2}{dt} = -x_1 - 2\sigma x_2 + a_2 h(x_1) \tag{1b}$$

where the binary hysteresis is characterized by

$$h(x) = \begin{cases} 1 & \text{for } x_L < x \\ 0 & \text{for } x < x_U \end{cases} \tag{1c}$$

and the constants are chosen to be

$$x_L = 0, \quad x_U = 0.3, \quad \sigma = -0.2, \quad a_1 = -1, \quad a_2 = -1.34996673232527... \tag{1d}$$

In Eqs. (1) x_1 and x_2 are the two dynamicel (state-like) variables and x_L and x_U the hysteresis jump points (to the lower and to the upper half lines, respectively). And, although Eq. (1c) indicates a double valued function, we consider true hysteresis which is single valued by requiring that h(x(t+)) retains the value of h(x(t)) unless x hits a jump point (practically in electronic circuits this is usually a consequence of the small parasitic capacitors [15]). The strange value of a_2 is chosen to give a continuous return map (the map of next crossings of the $x_2>0$ axis) in order that the Li-Yorke Theorem (which requires continuity) is satisfied; however continuity is not really necessary and the system is rather robust and the choice of a_2=-1.35 works well.

As was proven in [10] using the Li-Yorke Theorem, given appropriate initial conditions the system of Eqs. (1) will yield chaos.

III. Ideal DVCCS Realization

In this section we give a realization of Eqs. (1) using ideal components based upon voltage controlled current devices rather than the op-amps previously used. This will be done in such a manner as to conveniently allow denormalizations to practical VLSI circuits. Especially we will use the differential voltage controlled current source (DVCCS), using it to obtain all of the terms on the right hand side of Eqs. (1), including the hysteresis, while realizing the left had sides as currents in unit capacitors. The key

subcircuit which makes this possible is that for the hysteresis for which we use the circuit presented by Linares in his dissertation.

Since the left hand sides of Eqs. (1a,b) are capacitor currents, the variables x_1 and x_2 are voltages. These are turned into currents for the right hand side of these equations, this being done by the use of a DVCCS for each nonhysteresis term and by a hysteresis DVCCS with a current mirror on the output to feed the same current, $h(x_1)$, with two different weights, a_1 and a_2, to the current summing nodes used to obtain Eqs. (1) by Kirchhoff's Current Law (KCL).

First we present the hysteresis circuit of Linares but as a preliminary, in Fig. 2(a), define the notation and symbolism for the ideal DVCCS, of SPICE symbol G, and in Fig. 2(b) the ideal current mirror. The output of the DVCCS is a current, i_o, whose value

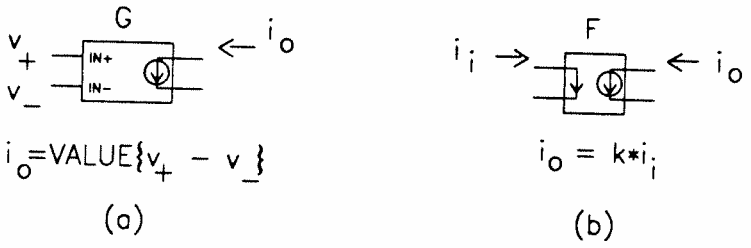


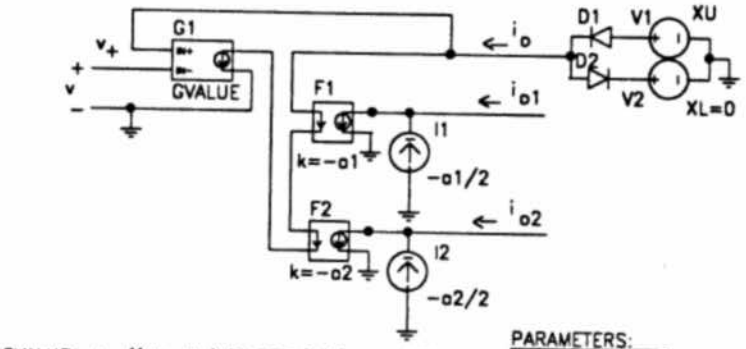
Figure 2
PSpice Symbols for Ideal Controlled Sources
(a) DVCCS, labeled G in SPICE (b) Current Mirror, labeled F in SPICE

depends upon the difference of the two input voltages, v_+ and v. both measured with respect to ground. This output may be nonlinear (as needed here for hysteresis), in which case it is read into PSpice as a function through the VALUE{·} statement; if this is a linear function, $i_o=g_m(v_+-v_-)$, only the (mutual) transconductance g_m is read in. The ideal current mirror, of SPICE symbol F, is assumed linear with current gain k, $i_o=ki_i$, where i_o is the output and i_i the input currents.

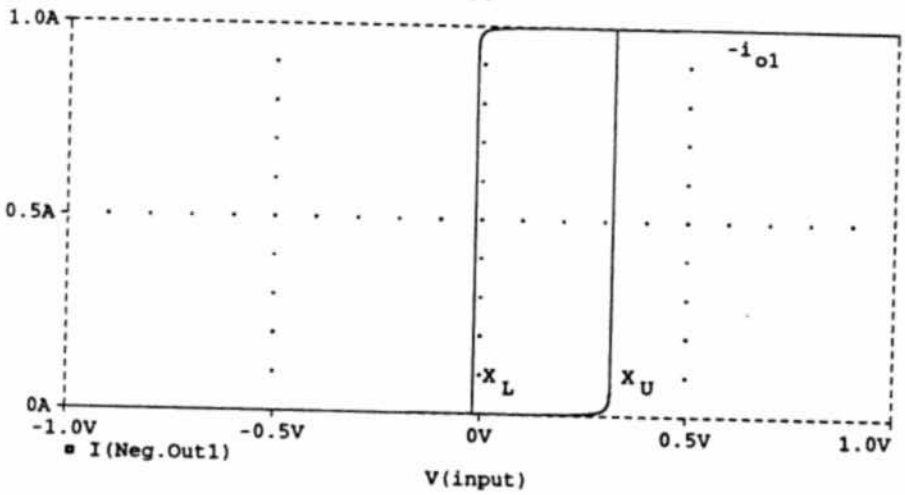
With the DVCCS in hand we present in Fig. 3(a) the (slightly modified) basic ideal DVCCS binary hysteresis circuit of Linares [11, p. 76] with a printout of the binary hysteresis obtained in its DC input-output characteristic shown in Fig. 3(b). The operation of the circuit is as follows. The ideal diodes D1 and D2 conduct the output current, io, of G1 in i_o's positive and negative directions, respectively, to obtain the two branches of the hysteresis and necessitating that the GVALUE function of G1 takes on positive and negative values; let these latter be constant and designated I_o and $-I_o$, respectively. Then when i_o is postive D1 is forward biased and $v_+=X_U$ and $v_+-v>0$, that is $v<X_U$ while when io is negative then $v_+=X_L$ and $v_+-v<0$, that is $X_L<v$. Thus if $X_L<X_U$ we have a double valued response given by

$$i_o(v) = \begin{cases} I_o & v < X_U \\ -I_o & X_L < v \end{cases} \qquad (2)$$

In Fig. 3(a) this current is mirrored in the current mirrors, F1 and F2, to give the currents to be fed to the circuit, after a shift of the curve, by current sources I1 and I2, to bring



(a)



(b)

Figure 3
DVCCS Binary Hysteresis Following Linares
(a) Circuit Diagram (b) DC Characteristics

the lower branch to zero for $v<X_U$. For realization of G1 by a transistorized DVCCS we have chosen $I_o=I_o$ and to obtain the (normalized) binary value we have chosen $I_o=1/2$ which yields the binary valued hysteresis after the shift by the current source I1 to give $i_{o1}=-h(v)$. A PSpice print out of $-i_{o1}$ is given in Fig. 3(b) where it is seen that the binary hysteresis has been well realized. To obtain Fig. 3(b) we used the approximation to a step function needed for G1 by way of the arctangent function, as indicated in Fig. 3(a); to obtain convergence we also had to insert very large resistors at certain nodes and replaced the ideal diodes by G devices connected as diodes with values set to VALUE=gd*((v+-v.) +abs(v+-v.)) with gd=10 chosen. Further a parasitic capacitor is needed to guarantee action as hysteresis, this being added at the dotted i_o node.

With the binary hysteresis in hand we can turn to a suitable configuration for realization of Eqs. (1). Figure 4(a) gives the resulting circuit realization of Eqs. (1) using these ideal components. The voltages on the unit capacitors are the state variables, x_1 and x_2, with the first term, x_2, on the right side of Eq. (1a) being the output current of the unit transconductance DVCCS G3; that current is also multiplied by -2σ via the current mirror F3 to obtain the second term on the right side of Eq. (1b). All the other terms of Eqs. (1a,b) similarly result from Fig. 4(a). Because this is used for PSpice simulations, the initial conditions, that is the initial capacitor voltages, are easily chosen via the software. However, the initial conditions can also be set by inserting current sources across the

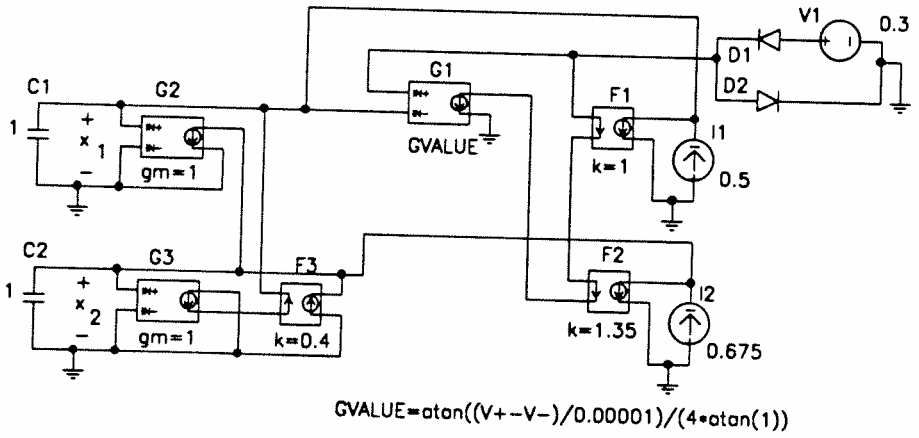


Figure 4
PSpice Ideal DVCCS Realization of Binary Hysteresis Chaos Generator
(a) Circuit Diagram

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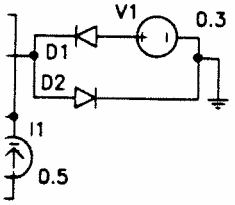

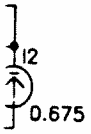

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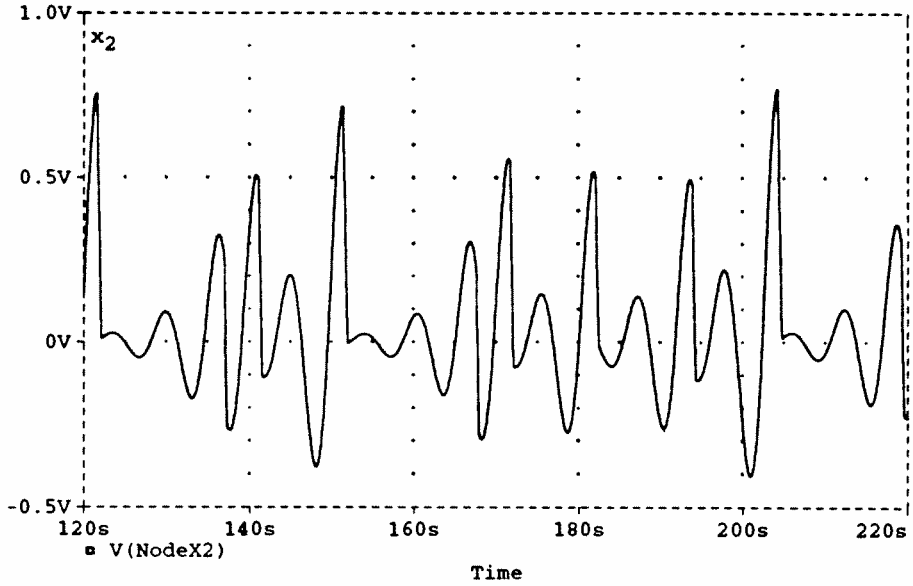

Figure 4 (b) Chaotic Response, Zero Initial Conditions

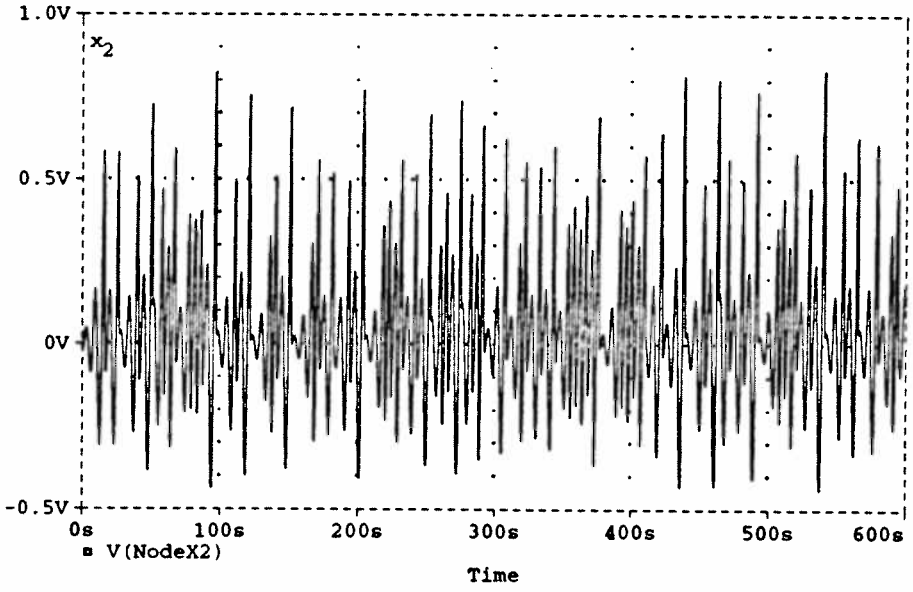

Figure 4 (c) Longer Time Span of Trajectory of (b)

capacitors with their currents being large but short pulses that drop to zero (to act as impulses); DVCCSs can also be used for realizing these initial condition current sources with these DVCCS inputs being pulses of voltage (which practically are easier to obtain than the pulses of current). However, in our case we have been able to achieve a design that uses zero initial conditions, by proper placement of the spirals in Fig. 1. In parts (b) & (c) of the figure are given a short time span and a long time span, respectively of a typical trajectory for x_1, this resulting from our choice of zero initial conditions.

IV. Practical DVCCS Realization for VLSI

Having the normalized circuit of Fig. 4 it remains to replace the ideal devices indicated there by transistorized components, something which is easily done using the work horses of analog VLSI, the CMOS current mirrors and differential pairs. In the case of the current mirrors, they are realized in VLSI form [16, p. 346] as shown in Fig. 5(a) for an NMOS structure and in Fig. 5(b) for a PMOS structure. The circuits of Fig. 5(a1) & (b1) are the basic current mirrors, but these are improved upon to obtain higher output

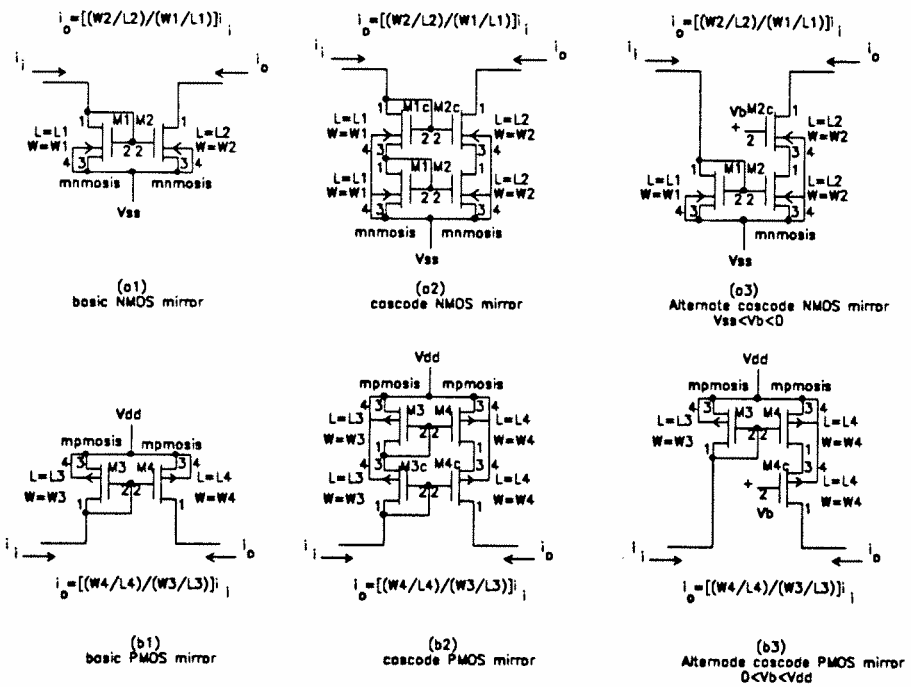

Figure 5
Basic Transistorized Devices
(a) NMOS & (b) PMOS Basic and Two Cascade Forms of Current Mirrors

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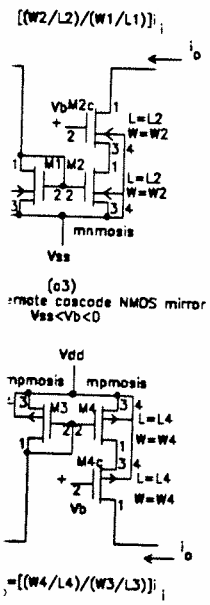

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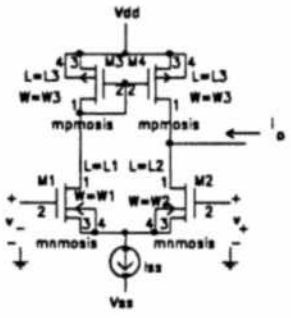


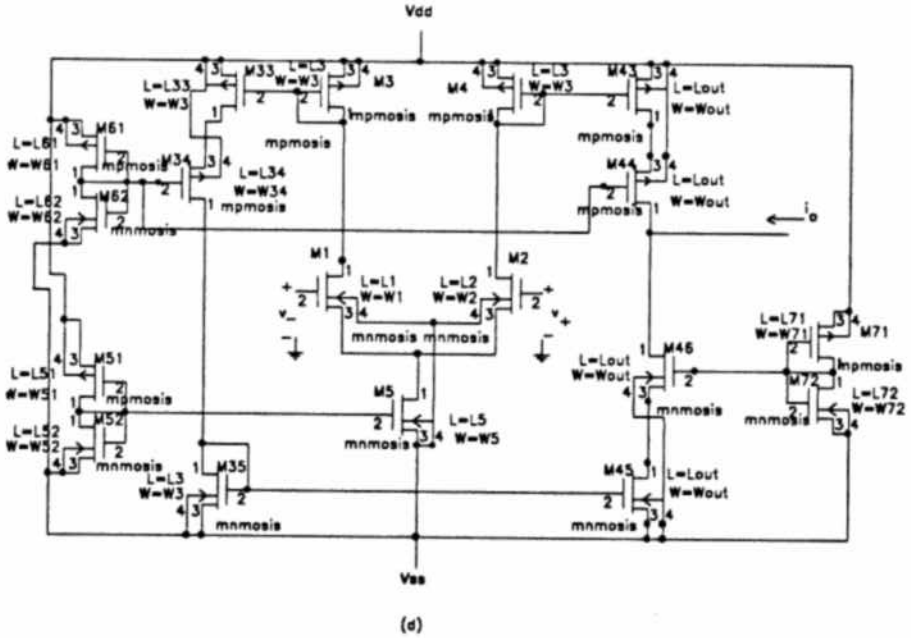


Figure 5
Basic Transistorized Devices
(c) Basic and (d) Practical Differential Pairs

impedance by use of the standard cascode connection of Fig. 5(a2) & (b2), this being important for the design of circuits sensitive to parameter changes, as is the case in chaos circuits. Figures 5(a3)(b3) show an alternate cascode connection [17, p. 404] which in our case is more effective since the output drive transistors, M2c & M4c, are held in saturation for almost all loads via the bias voltage Vb; although these are better for very sensitive structures, they do require the extra bias source. The current mirrors of Fig. 5 are actually uni-directional, the NMOS one giving a nonzero output current, i_o, only when the input current, i_i, is positive while the PMOS one yields only a nonzero output current when its input current is negative. But by placing the two types of current mirrors in parallel, a bidirectional current mirror is obtained. Both types of current mirrors work by transferring the voltage of the gate-source, V_{GS}, of the input transistor to the output transistor to force the drain currents of the two transistors to be equal (when $|V_{GS}|>|V_{threshold}|$ so the output transistor is turned on). The DVCCSs are readily constructed from differential pairs, often called differential amplifiers, with both MOS [16, p. 436] and bipolar [16, p. 446] transistor versions being available. For the chaos generator to be constructed in VLSI form, the MOS version is preferable (since pnp transistors and base current loading can be avoided) for which reason we use here MOS differential pairs, as given in Fig. 5(c). The basic differential pair shown in Fig. 5(c) has the source bias current Iss steered between the input transistors M1 & M2 by the difference, v+-v-, between the two input voltages with the difference of the two resulting drain currents taken as the output current formed by using a current mirror, M3-M4, on the M1 drain current. The circuit of Fig. 5(c) is the standard one, but it suffers from some defects which lead to deterioration of the output current especially when operating in a linear region. Consequently, we improve upon it by the circuit of Fig. 5(d) where the input transistors' drain currents are mirrored slightly differently by feeding that of M1 back around though M35-M45-M46 while also using the cascode connections of Fig. 5(a3)(b3). The current source Iss of Fig. 5(c) is realized by applying a fixed voltage to the gate of M5 biased in its saturation region (by a negative enough Vss). The bias voltages for M34-M44, M46, and M5 are obtained by the voltage divider connected N-PMOS pairs, M61-M62, M71-M72, and M51-M52, respectively. The voltages of these dividers being readily set by width to length ratios and the supply voltages Vdd & Vss as calculated by setting the drain currents of the two transistors in a pair to be equal in magnitude (on assuming the transistors are in the saturation region, which they will be for reasonable supply voltages). In the case of G1 and G2 two output currents are needed; these are simply obtained by mirroring the M1-M2 drain currents in another set of output current mirrors (similar to M43-M44-M46-M45) for which a different Wout/Lout is chosen. There remains the diodes of the binary hysteresis circuit. These can be realized as diode connected MOS transistors, in which the gates are tied to the drains. However, better diode characteristics result from junction diodes and, since our hysteresis needs sharp corners, we, consequently, construct the diodes from bipolar npn transistors, as are available in the BiCMOS process, by shorting bases to the collectors.

Before designing the fully transistorized circuit it is necessary to carry out a denormalization so that practical values of components can be used, in particular for gm of

the differential pairs, capacitances, and hysteresis parameters. Since our anticipated fabrication is through the MOSIS facility we will use the MOSIS BiCMOS transistor parameters as given in the Appendix. For our designs, to be discussed below, we found by simulations of the circuits outlined above, a base gm=5.3 micro Amp/Volt, an upper hysteresis jump point of X_U=0.81 Volts and an hysteresis upper amplitude of H^+=15.7 micro Amp (along with a lower amplitude of 0).

To match these practical values obtainable by physical components we perform a denormalization of Eqs. (1) as follows. To adjust for the transconductance value we multiply Eqs. (1a) and (1b) by a constant K1. Then we adjust for the hysteresis amplitude by multiplying and dividing h(x1) by K2. To adjust the upper jump point of the hysteresis we scale x_1 to z_1 by setting $x_1=Xz_1$ and to keep similar labeling set $x_2=z_2$. Finally to adjust the capacitors, the time scale is next changed by naming $t=t_{old}$, replacing t_{old} by $t_{old}=t_{new}/C$ and renaming $t_{new}=t$ to get

$$CK_1X\frac{dz_1}{dt} = K_1z_2 + \frac{K_1}{K_2}K_2a_1h(Xz_1) \tag{3a}$$

$$CK_1\frac{dz_2}{dt} = -K_1Xz_1 - 2\sigma K_1z_2 + \frac{K_1}{K_2}K_2a_2h(Xz_1) \tag{3b}$$

Consequently, we choose K_1= gm=5.3 microA/V, $K_2=H^+$=15.7 microA, X=0.3/0.81=0.37 and $C=0.25\times10^{-3}$ to give capacitors C1=0.49 nanoFd and C2=1.325 nanoFd. Most width to length ratios are chosen to be unity for convenience, for which we used L=10 micron=W. But in the case of the linear DVCCS's we used a ratio of W/L=2/24 for their input transistors to achieve a larger region of linearity. Also the width to length ratios were appropriately adjusted in the case of the nonunity current ratios of F2 and F3.

Putting everything together Figure 6 results to show the total circuit. Although this looks rather formidable it is formed in a straightforward manner described above from Fig. 4(a). In Fig. 6 we have used a numbering consistent with the ideal circuit of Fig. 4(a) by using the numbers in Fig. 4(a) in the hundreds position of the transistors of Fig. 6. Also in Fig. 6 there are three ideal current sources to compensate for offset currents of the differential pairs; these can be realized in the same manner as Iss in Fig. 5(d) but are kept as current sources to prevent further clutter of the figure. Similarly there are two voltage sources to set the hysteresis jump points, which can be realized by voltage dividers similar to those setting the biases on the cascode current mirrors. In the figure we also include two copies of the supply sources, of values Vdd=+5 and Vss=-5, in order to avoid further crossing of lines, but only one of each is actually to be used.

The substitutions between the ideal devices of Fig. 4(a) and the transistorized circuit of Fig. 6 are catalogued in Table 1. Figure 7 shows the zero initial condition trajectory obtained from Fig. 6 with part (a) and (b) giving the time traces of the capacitor voltages and part (c) giving the phase plane plot of z_2 versus z_1. It is clearly seen when and where z_1 hits the hysteresis jump point to the upper half plane at 0.81 Volt. By capturing

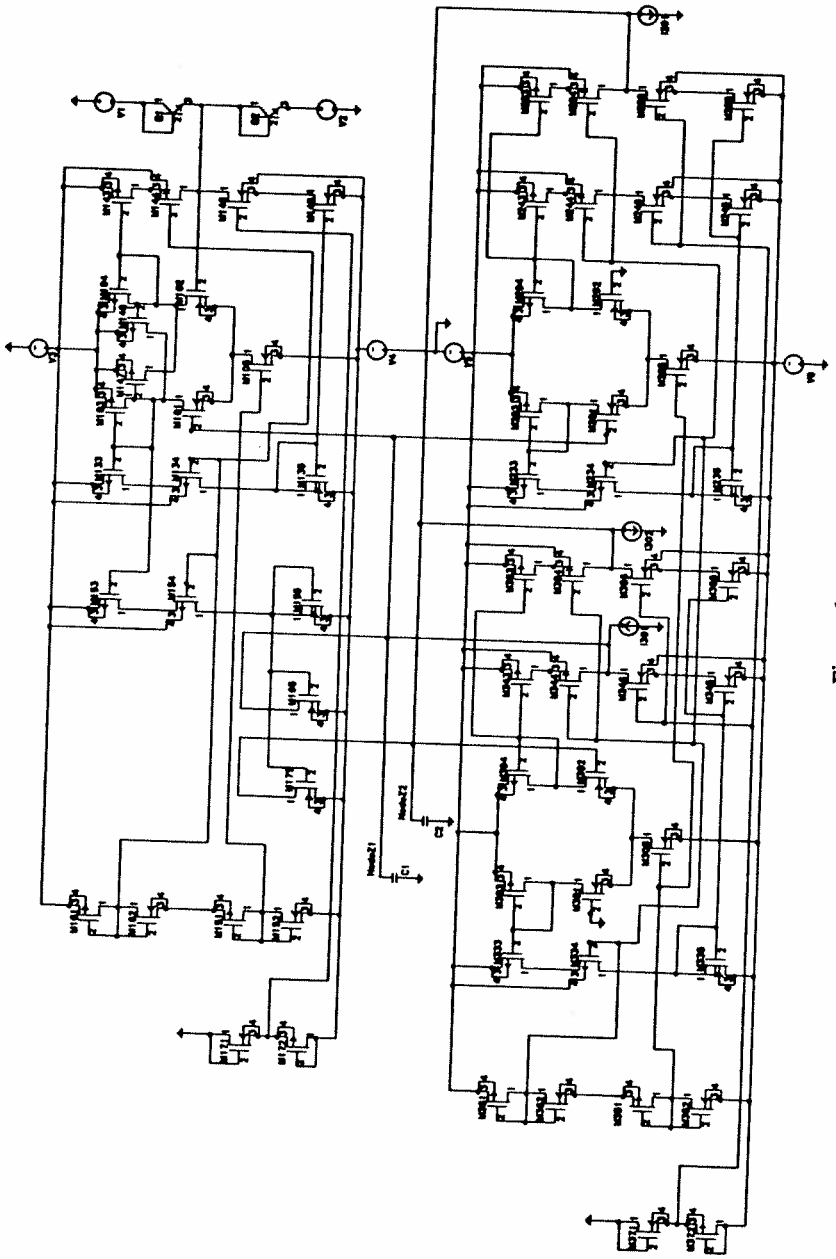


Figure 6
Practical DVCCS Realization

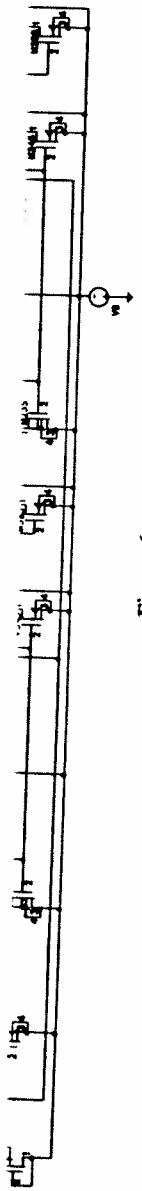


Figure 6
Practical DVCCS Realization

Table 1
Correspondences of Components of Figure 4(a) with Figure 6
all non listed L=10U, W=10U; x=0 through 9; U=10E-6

Fig. 4(a) Device	Fig. 6 Device	Purpose	Parameter	Comments
C1, C2	C1, C2	dynamics	C1=0.49n C2=1.325n	improvewith capacitor mult
D1-V1	Q1-V1	diode connected npn, X_U	V1=-0.6	Q1=diode connected npn
D2	Q2-V2	diode connected npn, X_L	V2=-0.2	Q2=diode connected npn V2 handles offsets
F1-I1	M165, 15x	for a_1 term	W165=3U	I1=0 due to mirror diode action
F2-I2	M175, 15x	for a_2 term	W175=4U	I2=0 due to mirror diode action
F3	M38x	for σ term	W383=4U W385=4U	
G1	M101, 102	input to differential pair for hysteresis		
	M103, 104 M13x, 14x	current mirrors		
	M16x & 17x	Vb	+2 & -2	
	M105, 15x	Iss of Diff. Pair	Iss gate vg=-3	
G2	M201, 202	input to linear differential pair	L=24U W=2U	
	M28x	current mirrors for z_1 term in (3b)	W283=3.7U W285=3.7U	
	M203, 204 M23x, 24x	current mirrors		
	M36x & 37x	Vb	+2 & -2	
	M205, 35x	Iss of Diff. Pair	Iss gate vg=-3	
	I201	offset current src		1 output
G3	M301, 302	input to linear differential pair	L=24U W=2U	
	M303, 304 33x, 34x	current mirrors M34x for z_2 term in (3a)		
	M36x & 37x	Vb	+2 & -2	
	M305, 35x	Iss of Diff. Pair	Iss gate Vg=-3	
	I301, 302	offset current srcs	I301=0.4U I302=0.6U	2 output currents
Vdd Vss	V3, V4, V5, V6	V3=V5=Vdd V4=V6=Vss	Vdd=+5 Vss=-5	Power Supply

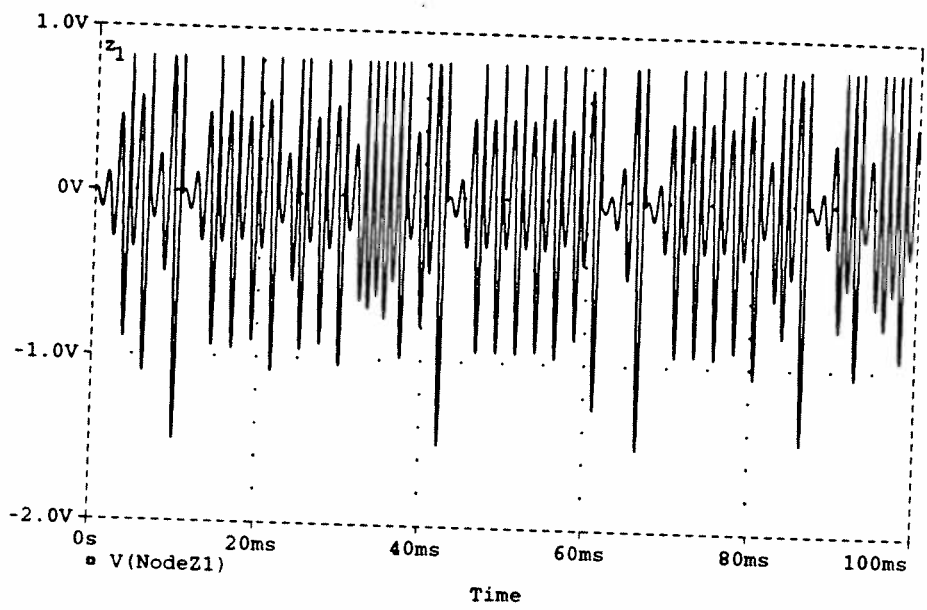


Figure 7 (a) Zero Initial Condition Responses of Practical Circuit, z_1 versus time

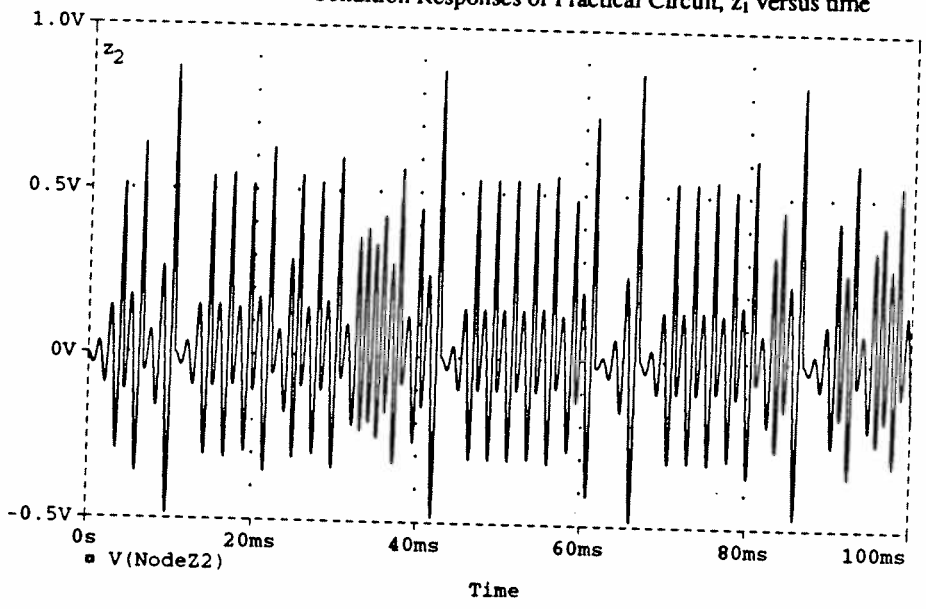
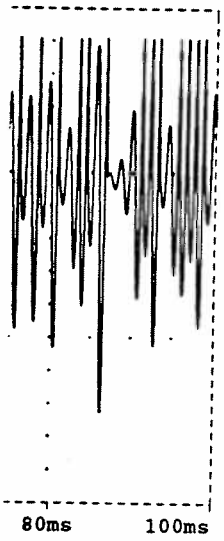
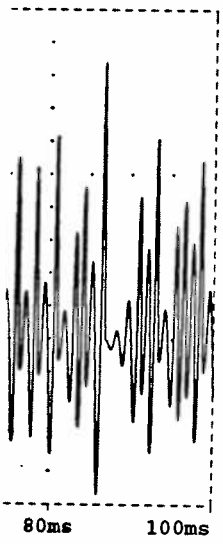


Figure 7 (b) Zero Initial Condition Responses of Practical Circuit, z_2 versus time



t, z_1 versus time



it, z_2 versus time

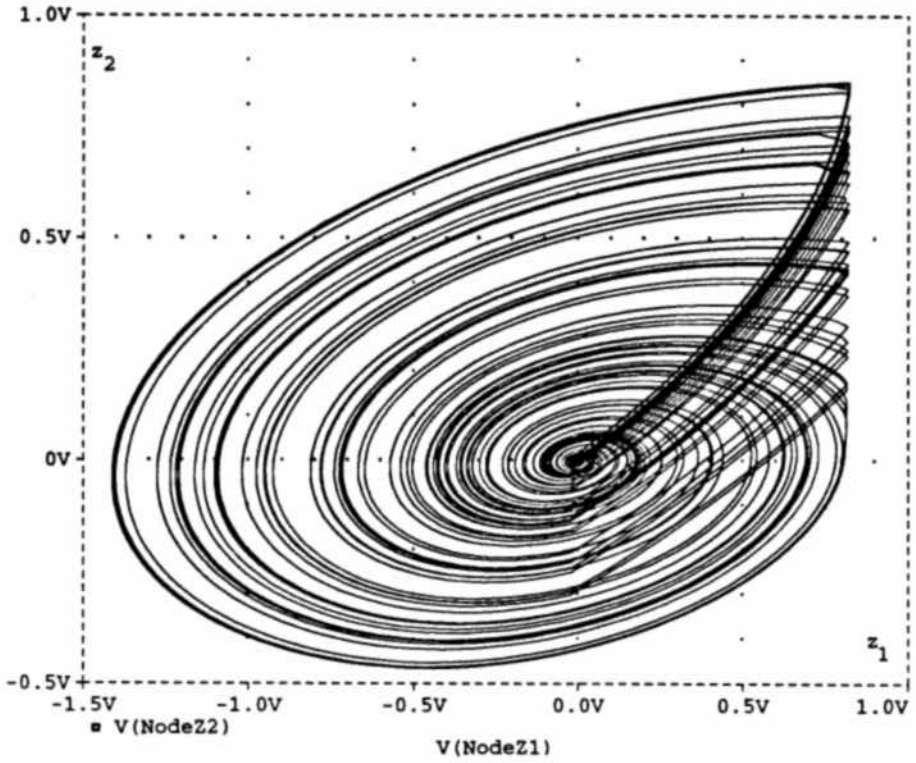


Figure 7 (c) Zero Initial Condition Responses of Practical Circuit, z_2 versus z_1 Plot

the times when these jumps occur one may be able to obtain some useful properties of this type of chaos.

The nature of responses of the circuit are quite dependent upon initial conditions. Although we have designed the circuit such that it gives a chaotic response with zero initial conditions, it may be desirable to allow for nonzero initial conditions. Such is easily accomplished by feeding the capacitors with a pulse of current which effectively acts as an impulse. Thus, by placing an MOS transistor's drain-source across a capacitor and feeding the gate-source with a short voltage pulse of appropriately large amplitude, desired nonzero initial conditions can be set.

On observation of the circuit of Fig. 6 it is seen that many components are present. Overall, however, the circuit presents no problem for integrated circuit fabrication. But the capacitors are larger than we would like and we feel that some optimization could be done to cut down on the number of transistors. To handle the capacitors, the sizes of which are needed to swamp parasitics, we would like to incorporate capacitor multipliers, with suitable ones possibly being available in the literature [18]. As for the number of

transistors, by optimal choices of W/L ratios, it appears that the current mirrors of Fig. 5(a1)(b1) or (a2)(b2) could be used. In any event the circuit of Fig. 6 is a working circuit suitable for small chip fabrication, though we do feel with time it can be improved upon.

V. Discussion

For lumped circuit constructions the previous realization of a binary hysteresis chaos generator is convenient since it used readily available operational amplifiers in an analog computer type of circuit. However, for integrated circuit realizations operational amplifiers, which are very high gain voltage controlled voltage sources, are nowhere near as convenient as voltage controlled current sources. Consequently, we have presented here a redesign which is ready to be put into layout for VLSI fabrication.

The binary hysteresis chaos generator is particularly appealing since it is only of degree two and uses hysteresis which is readily made using standard available transistors. It should be noted that we are able to get away with a degree two system since the describing differential equations contain discontinuous functions. Because the electronic realization of the hysteresis relies upon capacitive parasitics it might be fair to believe that really this is a degree three system, the parasitic capacitor giving the third derivative. However, this parasitic can be vanishingly small so in practice we ignore it in the design. Further, if one were to use other means of realizing the binary hysteresis, for example by magnetic amplifier cores, then one need not rely on the parasitics to insure operation; all that is needed is to obtain the operation represented by Fig. 1 and Eqs. (1).

Chaos generating circuits are presently becoming a dime a dozen since by introducing appropriate return feedback almost any degree two or higher circuit can be made to create chaotic signals. However, obtaining desired characteristics of the chaos is another story since, as yet, there is not available a satisfactory design theory which takes into account the nature of the chaos. But it does seem that the binary hysteresis chaos generator is something like the basic element from which arbitrary chaos can be built by concatenations and other combinations, just as arbitrary vectors are constructed from basis vectors.

Finally we comment that the speed of hardware particularly shows up in working with chaos generators. Whereas it takes hours to obtain results with software the same is obtained in milliseconds with hardware.

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References:

[1]. W. L. Ditto
August
[2]. T. L. Carro
Circuit
[3]. J. Neff and
No. 2,
[4]. L. O. Chua
Parts A
Octobe
[5]. T. Matsumc
and Sys
[6]. R. Newcom
Circuits
[7]. T. Saito, "A
Transac
[8]. T. Saito, "R
Circuits
[9]. R. W. Newc
the 1984
pp. 856
[10]. R. W. New
Systems
[11]. B. Linares-
dissertati
[12]. PSpice and
[13]. O. E. Rössl
Academy
[14]. T.-Y. Li an
Monthly,
[15]. R. W. Newc
Systems,
[16]. R. L. Geige
Digital C
[17]. P. E. Allen
New Yor
[18]. I. A. Khan a
Multiplie

References:

[1]. W. L. Ditto and L. M. Pecora, "Mastering Chaos," Scientific American, Vol. 269, No. 2, August 1993, pp. 78 - 84.

[2]. T. L. Carroll and L. M. Pecora, "Synchronizing Chaotic Circuits," IEEE Transactions on Circuit and Systems, Vol. 38, No. 4, April, 1991, pp. 453 - 456.

[3]. J. Neff and T. L. Carroll, "Circuits that Get Chaos in Sync," Scientific American, Vol. 269, No. 2, August 1993, pp. 120 - 122.

[4]. L. O. Chua and M. Hasler, Editors, "Special Issue on Chaos in Nonlinear Electronic Circuits," Parts A, B, C, IEEE Transactions on Circuits and Systems, Vol. 40, No. 10, I and II, October 1993 and Vol. 40, No. 11, November 1993.

[5]. T. Matsumoto, "A Chaotic Attractor from Chua's Circuit," IEEE Transactions on Circuits and Systems, Vol. CAS-31, No. 12, December 1984, pp. 1055 - 1058.

[6]. R. Newcomb and S. Sathyan, "An RC-Op-Amp Chaos Generator," IEEE Transactions on Circuits and Systems, Vol. CAS-30, No. 1, January 1983, pp. 54 - 56.

[7]. T. Saito, "An Approach toward Higher Dimensional Hysteresis Chaos Generators," IEEE Transactions on Circuits and Systems, Vol. CAS-37, No. 3, March 1990, pp. 399 - 409.

[8]. T. Saito, "Reality of Chaos In Four Dimensional Hysteretic Circuits," IEEE Transactions on Circuits and Systems, Vol. CAS-38, No. 12, December 1991, pp. 1517 - 1524.

[9]. R. W. Newcomb and N. El-Leithy, "A Binary Hysteresis Chaos Generator," Proceedings of the 1984 IEEE International Symposium on Circuits and Systems, Montreal, May 1984, pp. 856 - 859.

[10]. R. W. Newcomb and N. El-Leithy, "Chaos Generation Using Binary Hysteresis," Circuits Systems Signal Processing Journal, Vol. 5, No. 3, 1986, pp. 321 - 341.

[11]. B. Linares-Barranco, "Analog Neural Network VLSI Implementations," doctoral dissertation, Texas A&M University, December 1991.

[12]. PSpice and Design Center, Version 6.0, MicroSim Corporation, Irvine, CA, January 1994.

[13]. O. E. Rössler, "Continuous Chaos - Four Prototype Equations," Annals of the New York Academy of Science, Vol. 316, February 28, 1979, pp. 369 - 392.

[14]. T.-Y. Li and J. A. Yorke, "Period Three Implies Chaos," The American Mathematical Monthly, Vol., 82, No. 10, December 1975, pp. 985 - 992.

[15]. R. W. Newcomb, "Semistate Design Theory, Binary and Swept Hysteresis," Circuits, Systems, Signal Processing, Vol. 1, N. 2, 1982, pp. 203 - 216.

[16]. R. L. Geiger, P. E. Allen, and N. R. Strader, "VLSI Design Techniques for Analog and Digital Circuits," McGraw-Hill Publishing Co., New York, NY, 1990.

[17]. P. E. Allen and D. R. Holberg, "CMOS Analog Circuit Design," Holt, Rinehart and Winston, New York, 1987.

[18]. I. A. Khan and M. T. Ahmed, "OTA-Based Integrable Voltage/Current-Controlled Ideal C-Multiplier," Electronics Letters, Vol. 22, No. 7, March 27, 1986, ppl 365 - 366.

Appendix - SPICE Parameters for MOSIS Analog, BiCMOS, VLSI Fabrication

These are the MOSIS run parameters for run N21H SPICE LEVEL 2 parameters recorded 04/28/93 which were used for the simulations in order to design the circuit for VLSI fabrication.

A. The N Channel MOS Transistor Model

```
.MODEL MNMOSIS NMOS LEVEL=2 LD=0.250000U TOX=418.000008E-10
+ NSUB=9.236187E+14 VTO=0.858153 KP=5.048000E-05 GAMMA=0.198
+ PHI=0.6 UO=596.729 UEXP=7.029586E-02 UCRIT=10266.7
+ DELTA=2.7371 VMAX=65701.4 XJ=0.250000U LAMBDA=1.843384E-02
+ NFS=1.086360E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=28.760000 CGDO=3.097916E-10 CGSO=3.097916E-10 CGBO=3.838441E-10
+ CJ=8.997900E-05 MJ=0.783638 CJSW=5.524800E-10 MJSW=0.285064 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.24 um
```

B. The P Channel MOS Transistor Model

```
.MODEL MPMOSIS PMOS LEVEL=2 LD=0.250000U TOX=418.000008E-10
+ NSUB=9.309300E+15 VTO=-0.889271 KP=1.908000E-05 GAMMA=0.6289
+ PHI=0.6 UO=216.28 UEXP=0.218144 UCRIT=62664
+ DELTA=0.164572 VMAX=100000 XJ=0.250000U LAMBDA=5.011626E-02
+ NFS=9.266623E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=66.820000 CGDO=3.097916E-10 CGSO=3.097916E-10 CGBO=3.727276E-10
+ CJ=2.981300E-04 MJ=0.556944 CJSW=3.002100E-10 MJSW=0.243045 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.17 um
```

C. The NPN Bipolar Transistor Model

```
.MODEL BN2X1 NPN
+ BF=82 IS=1.588E-16 NF=9.9563E-01 NE=1.3356 VAF=57.1
+ IKF=2.3067E-02 ISE=1.267E-16 RE=12.7 RC=420.00 RB=1.213E+03
+ RBM=7.53 ISC=3.363E-15 NC=1.0202
+ CJE=0.1952E-12 MJE=0.5050 VJE=0.85 CJC=0.18815E-12 MJC=0.4990 VJC=0.80
+ CJS=0.2326E-12 MJS=0.2033 VJS=0.70
* AREA OF TRANSISTOR
* AE=128 um^2  PE=64 um  AB=644 um^2 PB=102 um AC=2064 um^2 PC=182 um
```

NONLINEAR DYNAMICS IN CIRCUITS

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