A VLSI Optoelectronic Receiver Neural Circuit for Generating Kohonen Learning Neighborhood[1]

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Abstract This paper presents a novel approach to implement an optoelectronic receiver circuit to generate a learning neighborhood in Kohonen feature maps. This proposed circuit has a size of 170x520 μm^2, power dissipation about a milliwatt, bandwidth from 100 Hz to 100 KHz, delay time of a microsecond, and voltage noise density in the order of 10^{-15} V^2/Hz. Temperature effect is also simulated. Detailed SPICE simulation results are given, along with circuit layout. A rough mathematical proof is appended.

I. Background

Kohonen feature maps have their greatest potential in areas such as image recognition, speech, and vector quantization. A rigorous theory was given by Kohonen [1]. The topology of a Kohonen map is defined by means of its lateral interconnections. The learning process that leads to self-organization involves the defining of a neighborhood around the maximally winning units. The neuromorphic approach uses a lateral excitation-inhibition coupling function which looks like a Mexican hat [2, pp. 232–246]. In the learning process [3], a variable size of neighborhood [3] is generated as illustrated in Fig. 1. A practical Kohonen algorithm is provided in [2, pp. 232–246] which specifies a learning neighborhood function $\exp(-r^2/2\sigma^2(t))$, where r is the metric distance between the light emitter of the winning neuron and the receiver of another neuron, $\sigma(t)$ is a width parameter that is gradually decreased in learning time t. However, there is a difference between the learning neighborhoods shown in Fig. 1 [3] and the learning neighborhoods defined by a function $\exp(-r^2/2\sigma^2(t))$. The former (Fig. 1) shows that only those neurons located inside the neighborhoods update their weights in the learning process, while the latter updates all neurons with weights according to the magnitude of a function $\exp(-r^2/2\sigma^2(t))$. Here, we will implement the latter.

Unfortunately, very few hardware implementation circuits for the Kohonen learning algorithm can be found in the literatures [4]. In Heim's research [4], a simple CMOS analogue nonlinear network is used. However, it still has the drawbacks of high power dissipation, and a very limited number of interconnections.

Consequently, a circuit dissipating low power and having maximal interconnections is desired. We note that optoelectronic neural networks can provide massive interconnectivity and high parallelism among neurons [5] while transistors operating in the subthreshold region can save power [6]. This paper proposes an optoelectronic Kohonen learning neighborhood circuit which uses photoreceptors for detecting the metric distances between the transmitter of the winning neuron and a receiver of another neuron, and has PMOS transistors operating in the subthreshold region. In this paper, each neuron has its own transmitter (LED) and receiver. Figure 2 shows a diagram of an optoelectronic system which can generate the learning neighborhood of Kohonen feature maps. Figure 2 consists of two layers, transmitter and receiver. Here we will not treat the transmitter. But it can be considered to be a chip configured as an LED array which has only one winner unit shining light on receivers at a time. Receivers generate voltages V_{out} exponentially proportional to the distance between the shining LED and each receiver (as proven in the Appendix, see Eqs. (23–24)). Therefore, we can define the Kohonen learning neighborhood by the value of V_{out}. By changing the light intensity of an LED, which in effect changes $\sigma(t)$, we change the size of its neighborhood (see Fig. 1). This proposed circuit is theoretically proven and verified by SPICE simulation.

II. Circuits

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Appendix — Analysis of Network Diagram

In this section, we prove that the proposed circuit of Fig. 3a can meet the demand for generating the learning neighborhood of a Kohonen feature map. Circuit equations and formulas will be derived.

The function we desire to implement is proportional to $\exp(-r^2/2\sigma^2(t))$, where r is the metric distance between the transmitter of the winning neuron and a receiver of another neuron and $\sigma(t)$ is a width parameter that is gradually decreased in learning time t. Noting the output of Fig. 3a, $V_{out}=R_5 i_3$ will prove that i_3 (see Fig. 3a) is equal to $F\exp(-Hr^2)$, where F and H are constants (see Eqs. (22–23)). First of all, the output voltage V_3 of the first stage will be proven to be $A(-\log(1/r^2))+B$, where A and B are also constants (Eq. (13)). Then, we will find the second and third stages have similar I-V curves. For the convenience of implementation, we can change the form of $\exp(-r^2)$ to $\exp(-\exp(-\log(1/r^2)))$ because stage 1 implements the inner $A(-\log(1/r^2))+B$ function (=F1), stage 2 implements exp(F1), and stage 3 implements exp(-exp(F1)).

The first stage in the Fig. 3a is also called a photoreceptor which was first given by Mead [9, p. 261]. So, we will get a current i_1 proportional to the light intensity while the light intensity is proportional to the inverse square of distance (r) (Eq. (13)). Following is the proof.

Subthreshold transistor models are given in references [6, 11, 12]. Looking at a simple model given by [6, p. 644, Eq. (1)] for the n-channel subthreshold transistor drain-source current but changing the reference point of gate voltage to the source instead of bulk Fermi level used in [6], we get

$$I = I_0 e^{\frac{\kappa}{V_T} V_{gs}} e^{\frac{V_{sb}}{V_T}(\kappa-1)} \left(1 - e^{-\frac{V_{ds}}{V_T}} + \frac{V_{ds}}{V_o}\right) \tag{1}$$

where V_{gs} is the gate-source voltage.

V_{sb}= source voltage with reference to bulk Fermi level,

V_{ds}=drain-source voltage, I_0=constant current,

κ=the effectiveness of the gate voltage in determining the surface potential. The value of κ can vary considerably among processes but is typically near 0.7.

V_o=absolute value of the Early voltage, V_T=kT/q, k=Boltzmann's constant, T=absolute temperature, q=magnitude of charge on an electron.

From Eq. (1), assuming operation in the saturation region, where V_{ds}/V_T is large, and large Early voltage, we can rewrite Eq. (1) into

$$I_{NMOS} = I_0 e^{\frac{\kappa}{V_T} V_{gs}} e^{\frac{V_{sb}}{V_T}(\kappa-1)} \tag{2}$$

For a completely complementary p-channel device, which we assume for simplicity, the signs of all voltages and currents in Eqs. (1–2) are reversed, and we get

$$I_{PMOS} = -I_0 e^{-\frac{\kappa}{V_T} V_{gs}} e^{-\frac{V_{sb}}{V_T}(\kappa-1)} \tag{3}$$

Noting that the substrates are tied to V_{dd} for PMOS, applying Eq. (3) to transistors M2 and M3 (see Fig. 3a) and using V_{sb} as 0 for M2 & (V_2-V_{dd}) for M3, we obtain

$$i_1 = I_0 e^{-\frac{\kappa}{V_T}(V_2 - V_{dd})} \qquad (for \quad M2) \tag{4}$$

$$= I_0 e^{-\frac{\kappa}{V_T}(V_3 - V_2)} e^{-\frac{(V_2 - V_{dd})}{V_T}(\kappa-1)} \qquad (for \quad M3) \tag{5}$$

Solving Eqs. (4–5) by taking logarithms of the last two terms, we get

$$V_3 = \frac{V_2(1+\kappa) - V_{dd}}{\kappa} \tag{6}$$

$$V_2 = \frac{\kappa V_3 + V_{dd}}{1+\kappa} \tag{7}$$

which on plugging Eq. (7) into (5) gives

$$i_1 = I_0\, e^{\frac{\kappa^2}{V_T}\left(\frac{V_{dd}-V_3}{1+\kappa}\right)} \tag{8}$$

$$\log\frac{i_1}{I_0} = \frac{\kappa^2}{V_T}\left(\frac{V_{dd}-V_3}{1+\kappa}\right) \tag{9}$$

$$V_3 = V_{dd} - \frac{V_T(1+\kappa)}{\kappa^2}\left[\log\frac{i_1}{I_0}\right] \tag{10}$$

Next, we derive that i_1 is a function of distance (r). When the base terminal of NPN transistor (Q1) is floating, light shone on the phototransistor Q1 will contribute a photocurrent i_1 in the collector. From [7, pp. 745–789], the average photocurrent i_1 due to the optical signal is

$$i_1 = q\eta P_{opt}/h\nu \tag{11}$$

In addition, it is pointed out in [8, p. 29–2] that the number of photons per unit area is proportional to $1/r^2$.

$$i_1 = \frac{q\eta}{h\nu}\frac{I_n\Lambda}{4\pi r^2} \tag{12}$$

where q= magnitude of charge on an electron, P_{opt}= incident optical power, $h\nu$= photon energy at frequency ν, η= quantum efficiency = the number of electron-hole pairs generated per incident photon. Λ is the phototransistor collecting light area, and I_n is the power of a point light source.

It is evident in Eq. (10) that V_3 is proportional to $-\log i_1$ while in Eq. (12), we get i_1 is proportional to the number of photons in per unit time. In short, we get V_3 proportional to negative $\log(1/r^2)$.

$$V_3 = A\left(-\log\left(1/r^2\right)\right) + B \tag{13}$$

where $A=(1+\kappa)V_T/\kappa^2$ and $B=V_{dd}-[(1+\kappa)V_T/\kappa^2]\log[(q\eta I_n\Lambda)/(4\pi h\nu I_0)]$ are constants.

In order to insure that all of the four NMOS transistors M4–M7 of the second stage operate in the subthreshold region, V_3 is passed to the level shifter. As we have done for the p-channel transistors of the first stage, and noting that the NMOS substrates are tied to ground, we can write i_2 in terms of V_{31} and V_7 from Eq. (3) and solve for i_2 as given by Eq. (15).

$$i_2 = I_0 e^{\frac{\kappa(V_{31}-V_7)}{V_T}} e^{\frac{V_T(\kappa-1)}{V_T}} = I_0 e^{\frac{\kappa V_7}{V_T}} \tag{14}$$

$$i_2 = I_0\, e^{\frac{1}{V_T}\frac{\kappa^2}{1+\kappa}V_{31}} \tag{15}$$

$$V_{31} = V_3 - C \tag{16}$$

where C= a constant level shifting voltage about 1.9v.

Now plug Equations (10) and (16) into (15),

$$\begin{aligned} i_2 &= I_0\, e^{\frac{1}{V_T}\frac{\kappa^2}{1+\kappa}(V_3-C)} \\ &= I_0\, e^{\frac{1}{V_T}\frac{\kappa^2}{1+\kappa}\left[\left(V_{dd}-\frac{V_T(1+\kappa)}{\kappa^2}\log\frac{i_1}{I_0}\right)-C\right]} \\ &= I_0\; e^{-\log\frac{i_1}{I_0}+D} \\ &= I_0\, e^D\,\frac{I_0}{i_1} \\ &= \frac{E}{i_1} \end{aligned} \tag{17}$$

where

$$D = \frac{1}{V_T}\frac{\kappa^2}{1+\kappa}[V_{dd} - C]$$
$$E = e^D I_0^2 \tag{18}$$

So, the voltage V_{12} is

$$V_{12} = R_4 i_2$$
$$V_{10} = MV_{12} + N \tag{19}$$

Where M is the gain (~1) of the differential amplifier and N is the constant voltage (~153mv) according to our simulation due to nonzero offset voltage of the differential amplifier.

Finally, we can also express i_3 in terms of V_8 to V_{11} as above.

$$\begin{aligned} i_3 &= I_0 e^{\frac{-\kappa}{V_T}(V_{10}-V_{11}) - \frac{(V_{11}-V_{dd})}{V_T}(\kappa-1)} \\ &= I_0 e^{\frac{-\kappa}{V_T}(V_{11}-V_9) - \frac{(V_9-V_{dd})}{V_T}(\kappa-1)} \\ &= I_0 e^{\frac{-\kappa}{V_T}(V_9-V_8) - \frac{(V_8-V_{dd})}{V_T}(\kappa-1)} \\ &= I_0 e^{\frac{-\kappa}{V_T}(V_8-V_{dd})} \end{aligned} \tag{20}$$

Similarly, we can solve

$$\begin{aligned} i_3 &= I_0 e^{\frac{\kappa^4}{V_T}\left(\frac{V_{dd}-V_{10}}{\kappa^3+\kappa^2+\kappa+1}\right)} \\ &= I_0 e^{\frac{1}{V_T}\frac{\kappa^4(V_{dd}-N)}{\kappa^3+\kappa^2+\kappa+1}} e^{\frac{-1}{V_T}\frac{\kappa^4}{\kappa^3+\kappa^2+\kappa+1}M(E/i_1)R_4} \\ &= F e^{\frac{-G}{i_1}} \end{aligned} \tag{21}$$

where

$$F = I_0 e^{\frac{1}{V_T}\frac{\kappa^4(V_{dd}-N)}{\kappa^3+\kappa^2+\kappa+1}}$$
$$G = \frac{\kappa^4 MER_4}{V_T(\kappa^3+\kappa^2+\kappa+1)} \tag{22}$$

Remember that i_1 is proportional to $1/r^2$ to see that Eq. (21) gives

$$i_3 = F e^{-Hr^2}$$
$$H = \frac{q\eta I_n \Lambda}{4\pi h\nu} G \tag{23}$$

Equation (23) is the form we desire and yields the voltage V(20) as the desired output voltage which defines the learning neighborhood.

$$\begin{aligned} V_{20} &= R_5 i_3 \\ &= R_5 F e^{-Hr^2} \end{aligned} \tag{24}$$

When compared Eq. (23–24) with $\exp(-r^2/2\sigma^2(t))$, we see that $H=1/(2\sigma^2(t))$. One way to decrease σ is to increase the power (I_n) of shining LED (see Eq. (23)).

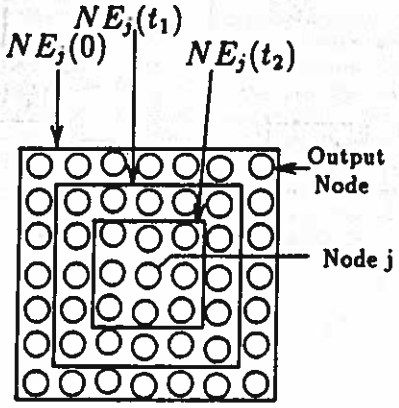


Figure 1. Topological neighborhoods at different times as feature maps are formed. $NE_j(t)$ is the set of nodes considered to be in the neighborhood of node j at time t. The neighborhood starts large and slowly decreases in size over time. In this example, $0 < t_1 < t_2$ [3, p. 19].

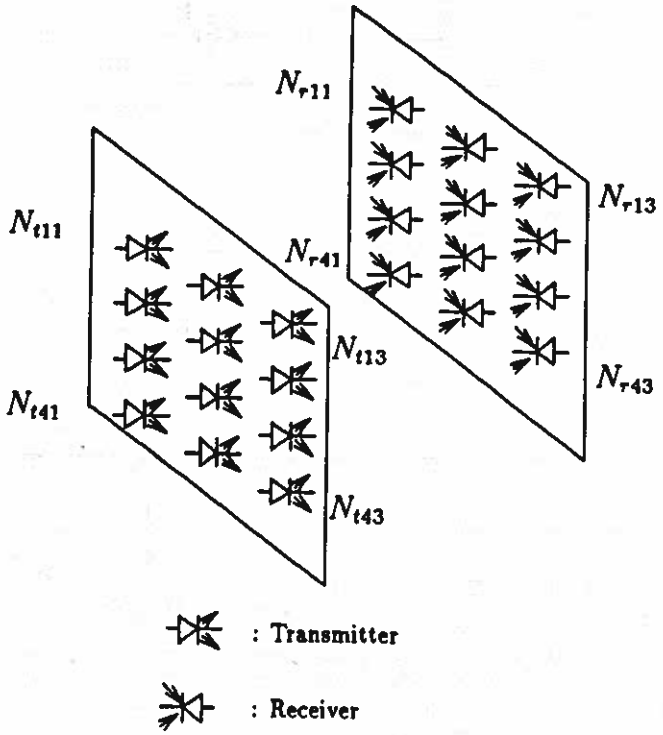


Figure 2. The system diagram of the optoelectronic neural circuit for generating the Kohonen learning neighborhood. It consists of transmitter layer and receiver layer.

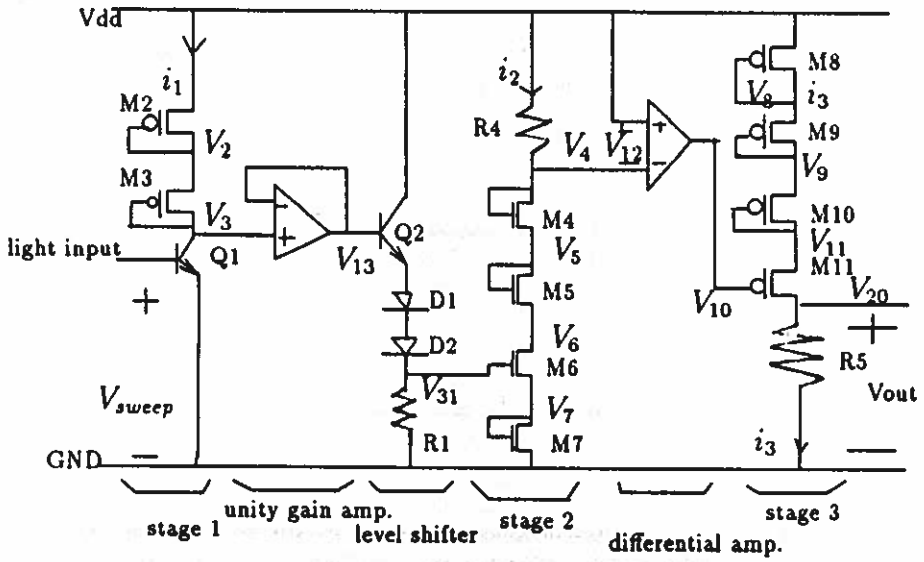
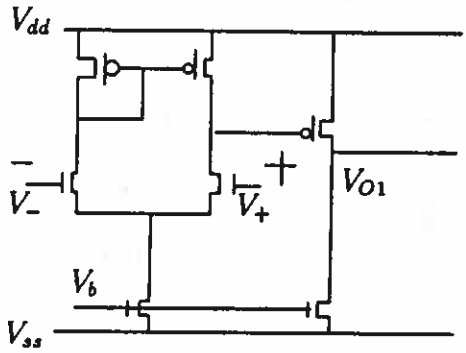
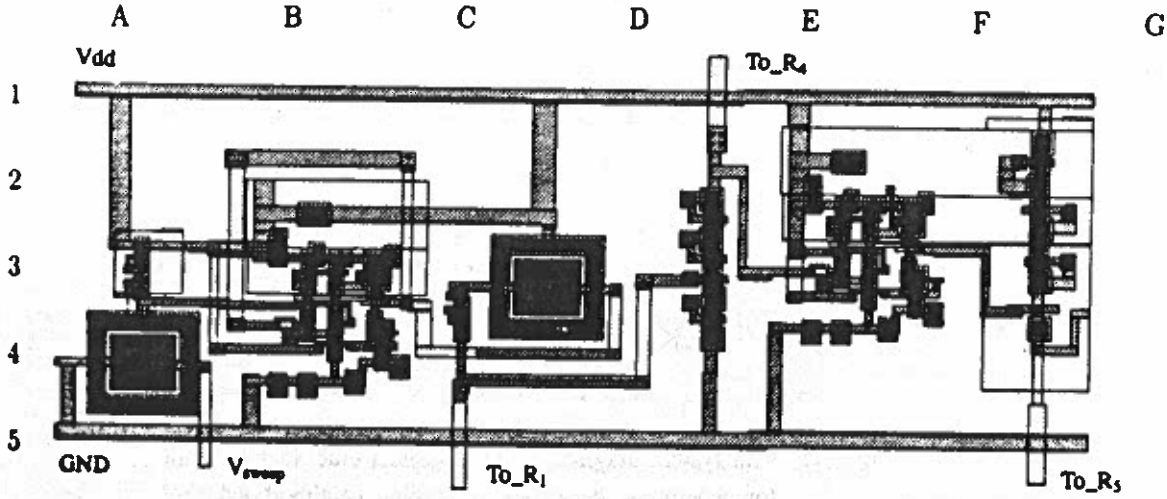


Figure 3a. The receiver circuit diagram which can generate the learning neighborhood of Kohonen feature maps.



3b. The realization of a differential amplifier (used in figure 3a).



3c. A Magic tool layout of Figure 3a. The size is about 170 x 520 μm^2.

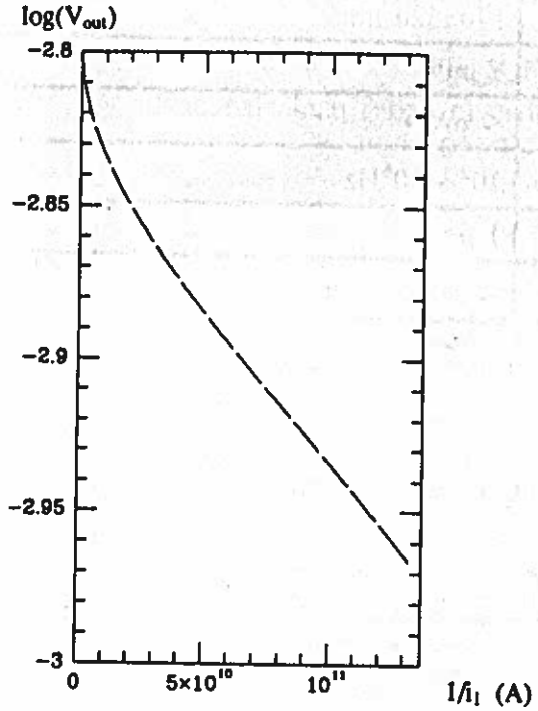


Figure 4. The SPICE circuit simulation of Fig. 3a. It shows the relationship of $\log(V_{out})$ versus the inverse of i_1.

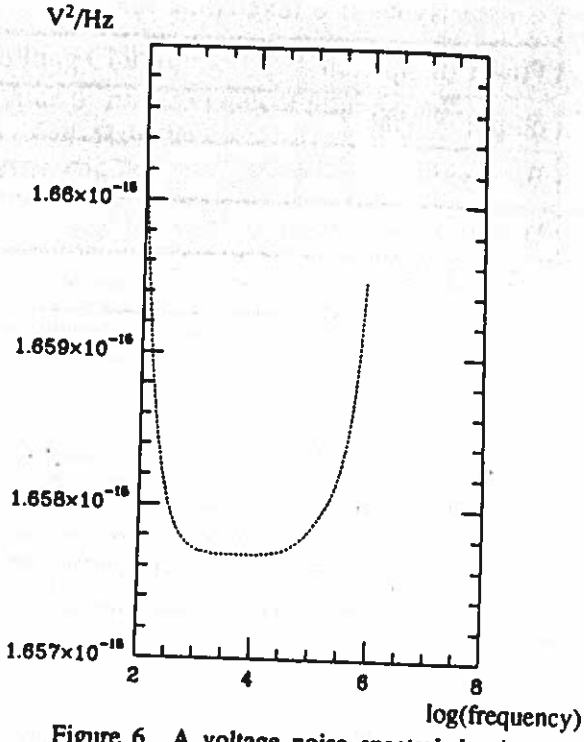


Figure 6. A voltage noise spectral density of Fig. 3a at 27°C.

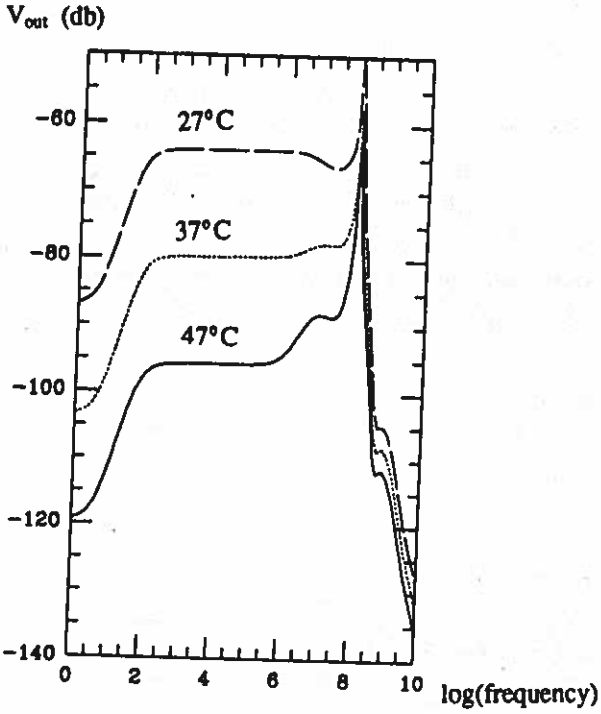


Figure 5. An AC response of Fig. 3a for temperatures at 27°C, 37°C, and 47°C.

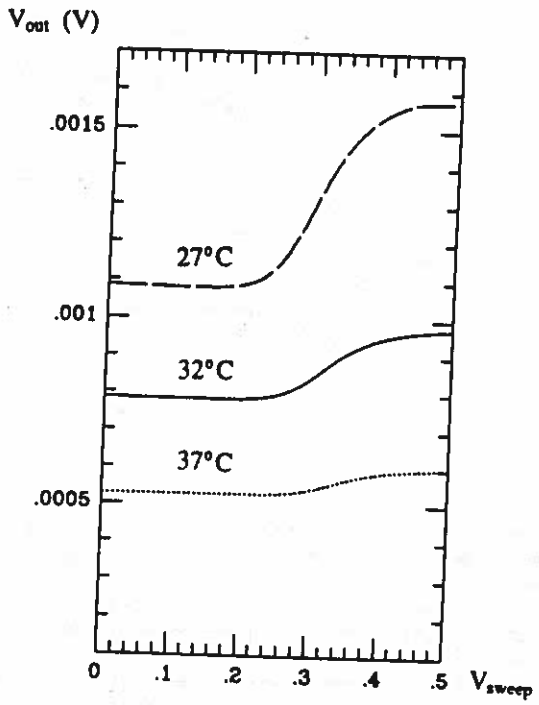


Figure 7. Output voltages (V_{out}) versus input voltage ($V_{sweep}=V_{BE}$) of the NPN transistor (Q1) at 27°C, 32°C, and 37°C

Circuit layout size (excluding resistors)	170x520 μm^2
Power dissipation	$\sim$ mw
output voltage	$\sim$ mv
Bandwidth	10^2 - 10^6Hz
Delay	1 μs
Noise density	$\sim 10^{-15}$ v^2/Hz

Table 1. A summary of the receiver circuit of Fig. 3a.

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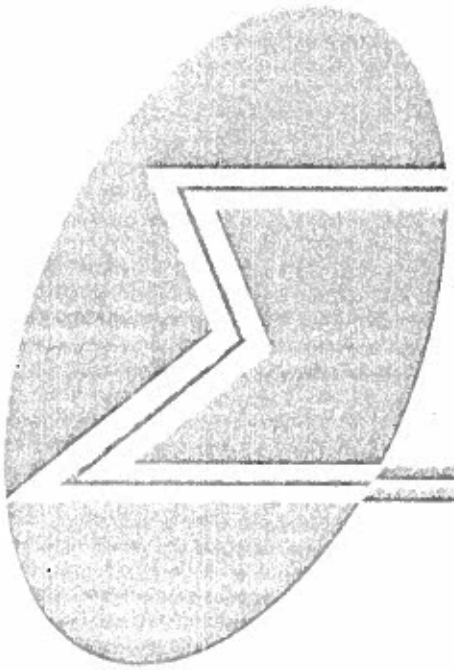

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