VLSI Circuits for Optoelectronic Neural Network Weight Setting[1]

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Abstract A VLSI optoelectronic implementation of matrix multiplication, which is useful for image-processing applications using neural networks, is presented. BiCMOS NPN and PNP phototransistors generate excitatory and inhibitory synapse currents when light shines on them. These synapse currents are controlled by complementary MOS transistors which allow us to program real valued weights. Differential amplifiers are used to sum the synapse currents while transmission gates are used as resistors. We present an example for digital weight interconnections with 5 bits resolution plus a sign. Circuit diagrams, SPICE3e1 circuit simulations, a NPN phototransistor magic layout, and a phototransistor measurement are also given.

I. Introduction

Matrix multiplication between input vector and weight matrix is the key operation for neural networks [1–4]. For hardware implementation, this has been done in electronic circuits which use floating gates, CCDs, or capacitors as weights [5–10]. Optoelectronic neural circuits, however, have advantages of providing massive interconnectivity and high parallelism which are useful for image-processing applications.

In Caudell's research [11–12], he proposed an electro-optical neural system, mainly built by photodetectors, miniature electro-optical cells, and laser diodes. Low resolution holographic mirrors are used to direct the global structure of network architecture [11]. In addition, Caudell uses a low cost filter, known as the binary phase-only filter (BPOF), and accompanied by a spatial light modulator (SLM) to implement the adaptive resonance neural network (ART1) [12]. Currently, holograms have been of interest in the implementation of optoelectronic neural networks because optoelectronic neurons fabricated from semiconductor materials can be connected by holograms [13–16]. However, these circuits are not easily integrated into a VLSI chip.

Some photoreceptors, based on CMOS technology, have been described by Mead [17]. A few VLSI oriented weight circuits are presented in references [18–22]. However, previous optoelectronic neural networks [19–22] have the limitations such as (1) only ±1 synapses are available and (2) synapses are not programmable.

Therefore, in this paper, we present a VLSI optoelectronic real valued matrix multiplication circuit which can be fabricated by ORBIT Analog 2.0 μ BiCMOS process.

II. Network Architectures and Circuit Diagrams

For simplicity, we build a digital weight interconnection with a resolution of b (b=5) bits plus a sign. Assume we have n input neurons (index j=1,...,n), and m output neurons (index k=1,...,m) (see Fig. 1). Let

$$\begin{aligned} X &= (x_1, \ldots, x_j, \ldots, x_n) \\ W_k &= (w_{k1}, \ldots, w_{kj}, \ldots w_{kn}) \\ V &= WX^T \end{aligned} \tag{1}$$

where X stands for a n-vector input, X^T is the transpose of X, W is a mxn weight matrix for output neurons, and V is a m-vector output. The notation, w_{kj}, is the weight value from input neuron j to output neuron k.

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We are going to do the matrix multiplications

$$v_k = \sum_{j=1}^{n} w_{kj} x_j \tag{2}$$

where v_k is the weighted sum of output neuron k.

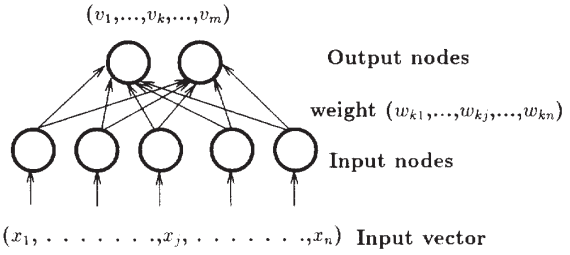


Figure 1: A Grossberg layer neural network [2,3].

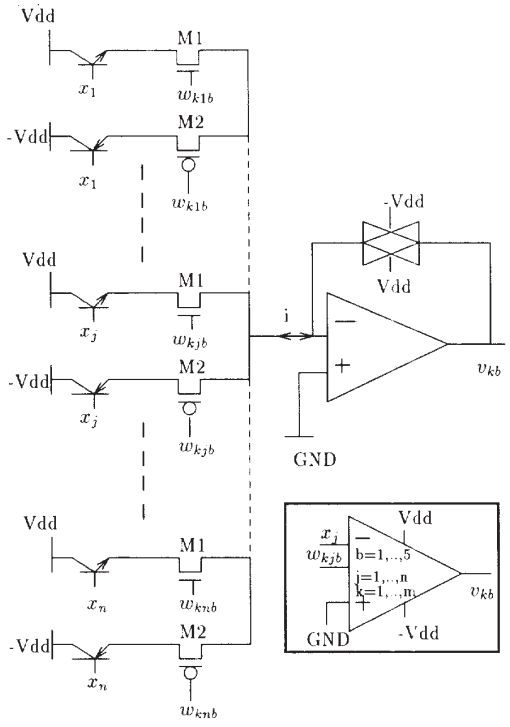


Figure 2: A circuit does a bit sum of products of an optoelectronic input vector and one bit of a digital weight vector W_k.

Figure 2 shows a bit multiplication between an optoelectronic input vector and one bit of a digital weight vector. A NPN phototransistor is responsible for the excitatory synapse current which flows into the summing node while a PNP phototransistor is for inhibitory synapse current which flows out of the summing node. Complementary MOS transistors (M1 & M2) are used to switch among excitatory synapse (when w_{kjb}= 5v, k=1,2,..,m, j =1,2,..,n, b=1,2,..,5), inhibitory synapse (when w_{kjb}= −5v), and 0 weight value (w_{kjb}= 0v), where w_{kjb} decides the bth bit (including sign) of weight w_{kj}. The optical input x_j has the binary value (0 or 1). Transmission gates are used as resistors. Therefore, we get the sum of products of weight (w_{kjb}, j=1,..,n) and input vector (x_j, j=1,..,n) for each bit line. Let us denote this bit line summation voltage as v_{kb}. The symbol for this circuit is shown in the inset.

Figure 3 shows the summation of all the 5 bit line voltages v_{kb} of Fig. 2. The input transmission gates are weighted by different L/W ratios from 1:1 to 1:16 while the output transmission gate has a 1:1 L/W ratio. Thus, we get an output voltage v_k for each output neuron k.

For operation, we use optical illumination (x_j from input neurons) (light on for logic 1, off for logic 0) applied to phototransistors on each bit (w_{kjb}) of weight value. If a bit weight is positive (negative), we apply 5v (-5v) to the bases of M1 & M2. If a bit weight is 0, the bases of M1 & M2 are grounded.

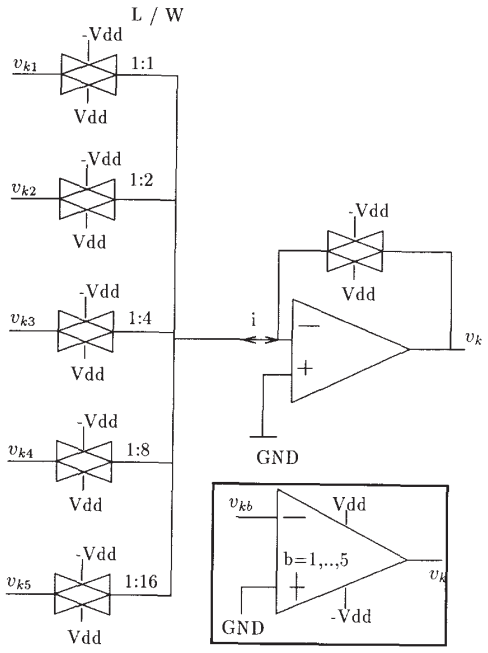


Figure 3: A circuit does the summation of 5 bit outputs from Fig. 2.

Figure 4 shows the differential amplifier we use in Figs. 2–3. Figure 5 is the transmission gate we use in Figs. 2–3.

Magic layouts of a NPN phototransistor and a summing amplifier are shown in Figs. 6 & 7 which have been fabricated by ORBIT Analog 2.0 μ BiCMOS process.

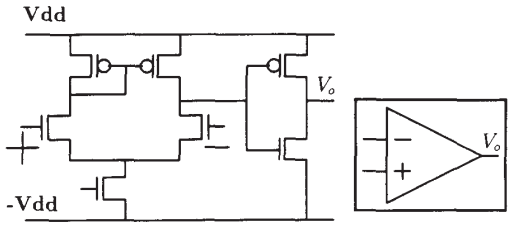


Figure 4: A differential amplifier circuit.

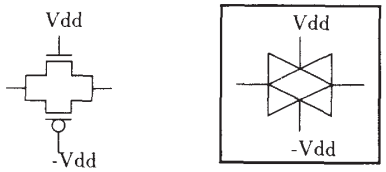


Figure 5: A transmission gate circuit.

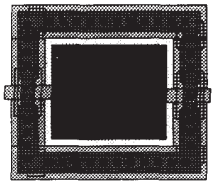


Figure 6: A magic layout of NPN phototransistor.

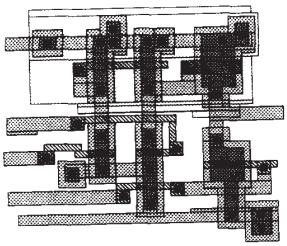
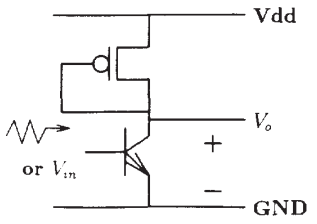


Figure 7: A magic layout of Fig. 4.

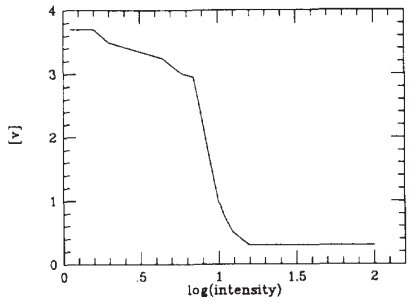
III. Simulations and Experiments

In this section, circuit simulation results obtained by SPICE3e1 are presented. In addition to simulation results, we present the characteristic curve of our photoreceptor.

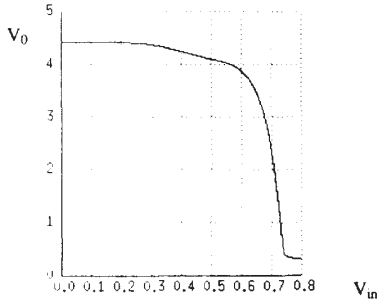
A test photoreceptor shown in Fig. 8a is considered. Figure 8b is the measured characteristic curve when light shines on the base of NPN phototransistor. Figure 8c is our SPICE3e1 simulation where we apply electric voltages on the base of NPN phototransistor. The consistency between our measurement and simulation is apparent. According to our measurement, when light shines on this NPN phototransistor, it generates a maximum current in the order of hundreds of microampere.



(a). A photoreceptor circuit.



(b). the measurement curve of Fig. 8a.

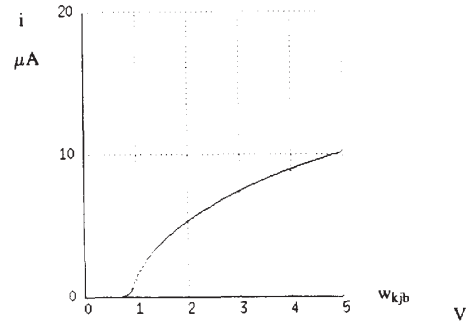


(c). the SPICE3e1 simulation result of Fig. 8a.

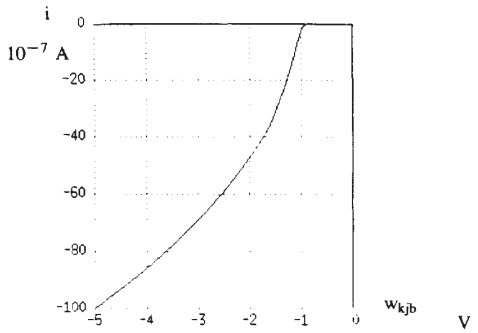
Figure 8: A photoreceptor circuit, a measurement curve, and a simulation curve.

Figure 9 shows the circuit simulations of Fig. 2. In our simulation, we apply electric voltages (0.667v for NPN and -0.732 for PNP) to the bases of phototransistors instead of optical illuminations. In Fig. 9a, we get an I-V curve by varying the input voltage of transistor M1 from 0 to 5v. In Fig. 9a, we get 10 μA current when the input to M1 is 5v. Similarly, we vary the input voltage of M2 transistor from -5 to 0v. In Fig. 9b, we obtain -10 μA when the input to M2 is -5v. In addition, we find that both M1 and M2 transistors are turned off when inputs are 0v (see Figs. 9a & 9b). Therefore, we get 10 μA excitatory current when the gate voltages of M1 & M2 are 5v, -10 μA for -5v gate voltages, and 0 μA for 0v gate voltages. The feedback transmission gate resistance is about 41 kΩ. Thus, we get each bit sum voltage V_{kb} (see Fig. 2) via a differential amplifier.

Figure 10 shows the characteristic I-V curves for 5 different L/W ratios of transmission gates. From Fig. 10, we ensure we can use those transmission gates as resistors. Figure 11 is the 5 bit summation of Fig. 3. In Fig. 11, each bit input voltage ranges from -1.5v to 1.5v. The result shows the summation is linear when inputs are all in the range of -1.5v to $+1.5$v. This range is easily obtained by controlling the value of feedback resistance in Fig. 2.



9a: An I-V curve for an excitatory synapse. When we vary the input voltage (w_{kjb}, k=1...,m, j=1,...,n, b=1,...,5) of transistor M1 from 0 to 5v, we get the current (i) which flows through M1.



9b: An I-V curve for an inhibitory. When the input voltage (w_{kjb}, k=1,...,m, j=1,...,n, b=1,...,5) of transistor M2 is varied from -5v to 0v, we get the current (i) which flows through M2.

Figure 9: The circuit simulation of Fig. 2. We apply 0.667v and -0.732v to the bases of NPN and PNP phototransistors respectively.

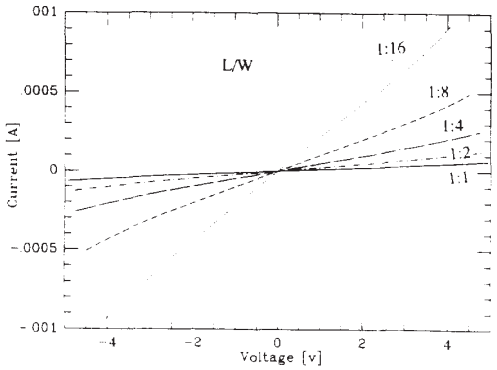


Figure 10: An I-V curves of 5 different ratios of transmission gates.

IV. Discussion & Conclusions

In our paper, a fabricated NPN phototransistor is presented along with measurements on the chip and SPICE3e1 simulations. A VLSI circuit for optoelectronic weight setting is designed and simulated. Magic layouts of the NPN phototransistor and a differential amplifier are shown. However, some points still need to be mentioned.

1. Our PNP phototransistor is a lateral bipolar transistor (see Fig. 12) because PNP transistor is not directly available in the MOSIS process. Due to a wide n-base and a low doping concentration in the n-base region, a lower gain than a NPN transistor is expected. However, it is still good enough for our circuits.

2. In our paper, we assume PNP and NPN phototransistors will generate equal amounts of photocurrents under moderate illuminations. In practice, we adjust the illumination areas of the PNP & NPN phototransistors to compensate for differences in the excitatory and inhibitory currents at a specific optical input level.

3. In order to guarantee the phototransistors operating properly, we maintain the correct voltage priority across the phototransistors.

4. In Fig. 11, the summation characteristic curve is not linear if all input voltages are not in the range of -1.5v to $+1.5$v. This is because we use a low gain differential amplifier instead of an ideal operational amplifier.

5. The optical input can be guided by waveguides or pass through a mask [23] to avoid interference.

In this paper, a VLSI optoelectronic circuit for weight setting is presented. Circuit diagrams are shown. Circuit simulations and experiments demonstrate this optoelectronic circuit theoretically works well.

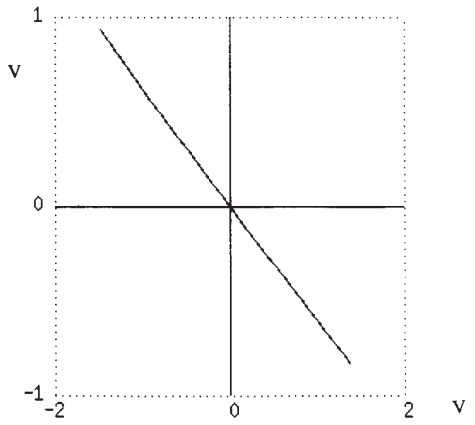


Figure 11: The simulation results of Fig. 3. Here, we assume v_{kb} (b=1,..,5) are equal and varied from -1.5v to 1.5v.

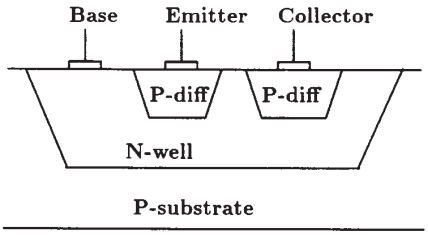


Figure 12: A lateral PNP phototransistor structure.

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