Guest Editorial
Neural Network Circuit Implementations

This is the third issue of the IEEE TRANSACTIONS ON NEURAL NETWORKS soley dedicated to the promising field of neural network hardware implementations. Again this time more than 50 potential manuscripts were originally submitted. The final 15 selected papers plus one invited on Fuzzy Logic went through a meticulous review process to keep high quality and practicality levels. Just for simplicity we have arrayed the articles in five groups.

The *Digital Neural Networks* group consists of three papers, the first, by Watanabe, Kimura, Aoki, Sakata and Ito dealing with a low voltage digital chip architecture for a 10^6—synapse neural network. Then, Wawrzynek, Asonović, and Morgan discuss the design of a neuro-microprocessor, these authors see this neuro-microprocessor as an intermediate step in the development of a connectionist network supercomputer. Lehmann, Viredaz, and Blayo describe a generic systolic array building block for neural networks with on-chip learning. A complete board dedicated to Hopfield's model is presented.

The *Pulse Coding* group includes a paper by Clarkson, Ng, Christodoulou, and Guan, introducing an adaptive probabilistic RAM chip. A small net of pRAM's performing a pattern-recognition task using reinforcement training is discussed. This pRAM generates a spike-train output waveform and differs from "pulse-stream" neurons. Donald and Akers discuss an adaptive neural processing node. The proposed analog VLSI processing chips use pulse coded signals for communication between processing nodes and analog weights.

The Components and Elements group represents a paper by Levy and McGill reporting a feedforward artificial neural network based on quantum effect vector-matrix multipliers. This approach is theoretically capable of densities and speeds far beyond anything that conventional VLSI in silicon could ever offer. Benson and Kerns discuss an ultraviolet photoinjection mechanism for programming analog, nonvolatile memories in CMOS circuits. The technique requires no special processing technology.

In the *Analog Neural Networks* group, Lansner and Lehmann present an analog CMOS chip set for neural networks with arbitrary topologies. The chip set consists of a neuron chip and a synapse chip. This last chip is a cascadable 4×4 matrix–vector multiplier. Linares-Barranco, Sánchez-Sinencio, Rodríguez-Vázquez, and Huertas present the extension of a modular approach capable to implement any neural network architecture by including on-chip learning and weight refreshing. To illustrate the approach a BAM IC prototype is shown. The next two papers discuss the analog implementation of a Kohonen neural network. Macq, Verelysen, Jesper, and Legat introduce a Kohonen implementation emphasizing on the storage of analog synaptic weights, based on the principle of current copiers. He and Çilingirogulu also present a Kohonen with on chip learning but using charge-mode techniques which yield a reduced silicon area.

In the *Applications* group, five illustrative articles are broached. Yuh and Newcomb describe a multilevel neural network for A/D conversion. A reformulated energy function with removed local minima problems for A/D conversion is presented. Choi, Bang, and Sheu present a programmable analog VLSI neural network processor for communication receivers. A channel equalizer was implemented with the proposed chip configured as a four-layered perceptron network. Yamakawa introduces analog-mode fuzzy inference and defuzzification hardware implementation. This Invited Paper is a tutorial introducing beginners on the usefulness of fuzzy systems and their analog hardware implementations. Lazzaro, Wawrzynek, Mahowald, Sivilotti, and Gillespie report an IC mode of temporal adaptation in the auditory nerve, that functions as a peripheral to a workstation with UNIX operating system. The last paper, by Delbrück, describes an analog VLSI predictive visual motion computation. This approach is focused at the use of motion-shear information for solving the structure-from-motion problem.

It is worthwhile to notice the current trends in neural network hardware implementations from this special issue here presented. *On-Chip learning* is becoming a reality, as shown by seven papers in this issue. There are still many practical problems to implement on-chip learning, but preliminary results are encouraging. Large size NN architectures using *modular* and *programmable blocks* are yielding practical implementations. No single hardware implementation suitable for any application has surfaced.

We want to thank many unselfish reviewers involved in this issue, specially Dr. B. Linares-Barranco and Professor Bing J. Sheu who helped us from the preliminary screening to the final selection of papers. Also, we wish to announce that the next Special Issue on Neural Networks Hardware Implementations is scheduled to appear in two years (May 1995).

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Guest Editors

Edgar Sánchez-Sinencio (S'72–M'74–SM'83–F'92) was born in Mexico City on October 27, 1944. He received the M.S.E.E. degree from Stanford University, Stanford, CA, and the Ph.D. degree from the University of Illinois at Champaign-Urbana, in 1970 and 1973, respectively.

Currently, he is with Texas A&M University as a Professor. He is the coauthor of Switched-Capacitor Circuits (Van Nostrand-Reinhold, 1984), and co-editor of *Artificial Neural Networks: Paradigms, Applications, and Hardware Implementation* (IEEE Press). His interests are in the area of solid-state circuits, including CMOS neural network implementations and computer-aided circuit design.

Dr. Sánchez-Sinencio was the General Chairman of the 1983 26th Midwest Symposium on Circuits and Systems. He has been Associate Editor for *IEEE Circuits and Systems Mag.* (1982–1984), for *IEEE Circuits and Devices Mag.* (1985–1988), for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS (1985–1987), and for the IEEE TRANSACTIONS ON NEURAL NETWORKS (1990–present). He is Guest Co-Editor for the IEEE TRANSACTIONS ON NEURAL NETWORKS Special Issue on Neural Network Hardware Implementation (1991, 1992, 1993). He was a Committee Member of the Scientific Committee of the Sixth, Eighth, and Ninth European Conference on Circuit Theory and Design (ECCTD), Committee Member of the Technical Program: *IEEE International Symposium on Circuits and Systems (ISCAS)* in 1983, 1987, 1989, 1990, 1992, and Chairman, *IEEE CAS Technical Committee* on Neural Systems & Applications (1990–1991). He was a member of IEEE CAS Board of Governors (1990–1992). He was appointed CAS Liaison Representative, IEEE Press. In 1992 he became a Fellow of the IEEE for contributions to monolithic analog filter design.

Robert W. Newcomb (S'52–M'56–F'72) was born in Glendale, CA in 1933. he received the B.S.E. degree from Purdue University in 1955, the M.S. degree in electrical engineering from Stanford University in 1957, and the Ph.D. degree from the University of California at Berkeley in 1960.

Afetr serving on the tenured faculty at Stanford, he joined the University of Maryland to update the graduate program. He has held visiting appointments in Belgium, Malaysia, and Spain, and currently directs the Microsystems Laboratory at the University of Maryland. He has been a member of a number of IEEE group, including the Neural Networks Council and the Society for Social Implications of Technology. During the 1960's he began research on micromotor fabrication and pulse-coded neural network circuit design. His recent research has concentrated on circuit realizations of neurophysiologically realistic neural-type systems, semistate theory and it use in nonlinear and neural systems design, and the determination of autoacoustic emission parameters for the ear.

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