VLSI Implementation of Neural-Type Cell with MOS Linear Resistor

G. Moon+, M. E. Zaghloul+, R. W. Newcomb*

+Electrical Engineering and Computer Science Department
George Washington University
Washington, DC 20052 USA
phone: (202) 994-3772

*Microsystems Laboratory
Electrical Engineering Department
University of Maryland
College Park, MD 20742 USA
phone: (301) 454-6869

Abstract

A CMOS integrated circuit for the weighted synapse and the summation of the synaptic signals is presented. Neural-Type Cells (NTC) are employed as the processing elements along with the voltage-controlled linear MOS resistor. This variable resistor is used to control the synaptic weights as pulse densities, and, thus, the weights are controlled by the gate control voltage. By adding buffered inverter stages, the output signal of the NTC is converted into the normalized pulse stream of $5V_{p-p}$ signal for easy handling. The summation is executed by a capacitor integration circuit where the currents from different NTCs' are accumulated. Simulation results are included.

I. INTRODUCTION

The behavioral characteristics of the electronic Neural-Type Cell have been studied in previous works [1,2]. This NTC, with its hysteresis characteristics [3,4], has the capability of coding the information into pulse streams whose frequency as well as pulse width are controlled by the input voltage level [5,6]. Based on this processing element, we now need to find a way to build up a network. For this, as the first step, the weighted synapses and their summation are investigated. A weighted synapse is realized by controlling the pulse density [7] of the pulses through a voltage-controlled resistor. The summation is done with a simple capacitor integrator. Although these arithmetic processes are not exactly linear, the resultant structure takes the full advantage of the inherent properties of the Neural-Type Cell.

II. THEORY

The circuit of the NTC is shown in Fig. 1. V1 is the input node and V3 is the output node. As the input increases above a certain level, the output will start to oscillate with a frequency which is roughly proportional with the input level. Simulation results for this are shown in Fig. 2. Here, we will replace the passive resistor R6 with the enhancement-type MOS voltage-controlled equivalent linear resistor [Fig. 3] with equivalent resistance value of the form [8]

$$R_{eq} = [K(V_{c2}-2V_t)]^{-1} \qquad (1)$$

where R_{eq} is the equivalent resistance, K is transistor gain factor, V_t is threshold voltage of the transistor.

Combining Figs. 1 and 3, the circuit of interest is shown in Fig. 4, which is composed of one NTC and three buffered inverters. Three buffered-inverter stages are added at the output node [Fig. 4], generating $5V_{p-p}$ excitatory and inhibitory signals. Notice also that R6 is replaced with the MOS linear resistor. Thus, as the gate control voltage of R6 changes, the equivalent resistance value of R6 will also change according to equation (1). The changes in R6 will result in variation of pulse width as well as pulse frequency. In this work, synaptic weights are defined in terms of pulse density of the output pulse. The buffered inverters are used to convert the the variations in the pulse width and frequency into pulse density modulation. It follows that we can use the gate control voltage of the equivalent resistor, R6, as a weight control signal. To illustrate this point further, we note that with a fixed input voltage level, the output V3 is oscillating around a certain dc offset voltage level. This offset voltage of the output signal V3 is controlled by the resistance value R6, resulting in variable pulse densities (duty cycles) at the output of the buffered inverter. The offset voltage of V3 can be simply represented as

$$V_{offset} = R5/(R6_{eq} + R_{M2} + R5) \qquad (2)$$

where $R6_{eq}$ is in (1) and R_{M2} is the average small signal equivalent resistance of the transistor M2 in Fig. 1.

From equations (1) and (2), we can find that as V_{c2} increases, R_{eq} decreases and V_{offset} increases, which will result in a change in pulse density of buffered signals. If we choose V_{c2} within a range such that the pulse density changes monotonically, then this range of Vc2 will be a maximum weight range.

+ Supported by NSF Grant MIP-90-01658
* Supported by NSF Grant MIP-89-21122

For the summation of several signals, a capacitor integrator is used. The charge will be accumulated across the capacitor with time and the amount of charge at a specific moment depends on the pulse density. We use different switches in parallel so that the currents will be summed in one capacitor, whose RC time constant is much larger (roughly 10 times) than the maximum pulse width.

III. SIMULATION RESULTS

The CMOS circuit diagram for simulations is shown in Fig. 5. Figure 6 shows the pulse density changes for (a) V_{c2}=-6.25V and (b) V_{c2}=-5V. The pulse densities (duty cycles) of the two cases for inhibitory signals are found as 73% and 51%, respectively. Figure 7 shows the corresponding charge accumulations across the 50pF capacitor using the excitatory signals. Notice that we acquired different slopes of accumulation, for the same input (4V), due to the pulse density difference. The current summation for the above two figures is shown in Fig. 8, which shows a reasonable result.

IV. CONCLUSIONS

In the above, we have described a technique to realize the synaptic weight and the summation using the NTC in CMOS integrated circuit form. This structure will be well applied with inhibitory function if we use the different polarity signal from three inverter stages. Voltage-controlled equivalent linear resistor is used to control the pulse density of the output of the NTC. A capacitor integrator is used to accumulate the charge and thus summing the pulsed signals. This structure could be used in an adaptive pulse coded neural type system.

REFERENCES

[1] R.W. Newcomb, "Neural-type Microsystems Circuit Status", Proc. of the IEEE, International Symposium Circuits and Systems, Newport Beach, CA 1983, pp 97-100.

[2] R.W.Newcomb, "MOS Neuristor Lines", in Constructive Approaches to Mathematical Models, edited by Cliffman and G. Fix, Academic Press, 1979.

[3] M. Savigny, N. El-Leithy, R. Newcomb, G. Moon, M. Zaghloul, "Hysteresis Turn-On-Off Voltages for a Neural-Type Cell", Proc. of 1990 IEEE CAS Mid-western conference, Calgery, Canada, pp.35-37, August 1990.

[4] N. El-leithy, and R.W. Newcomb, "Hysteresis in Neural-Type circuits", Proceedings of the 1988 IEEE International Symposium Circuits and Systems,Espoo, Finland, June 1988, pp.993-996.

[5] G. Moon, "VLSI Implementation of a Neural Type Cell", Master thesis, Dept. of Electrical Engineering and Computer Science, The George Washington University, September, 1990.

[6] G. Moon, M. Zaghloul, R. Newcomb, "IC Layout for an MOS Neural Type Cell," Proc. of IEEE CAS Mid-western conference, Urbana, Illinois, pp.482-484, August, 1989.

[7] J. E. Tomberg, K. K. Kaski, "Pulse-Density Modulation Technique in VLSI Implementation of Neural Network Algorithms", IEEE J. Solid-State Circuits, vol. 25, no. 5, pp.1277-1286, October 1990.

[8] G. Moon, M. Zaghloul, R. Newcomb, "An Enhancement-Mode MOS Voltage-Controlled Linear Resistor with Large Dynamic Range", IEEE Trans. on Circuits and Systems, pp. 1284-1288, Vol. 37, no. 10, October 1990.

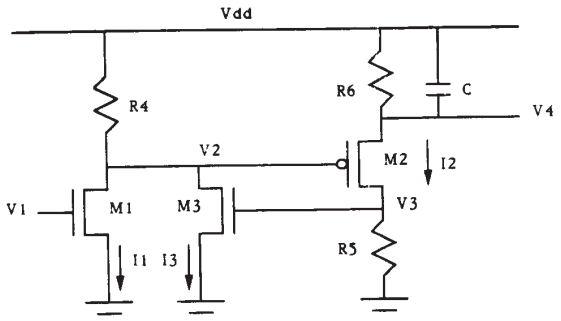


Fig. 1. Neural Type Cell.

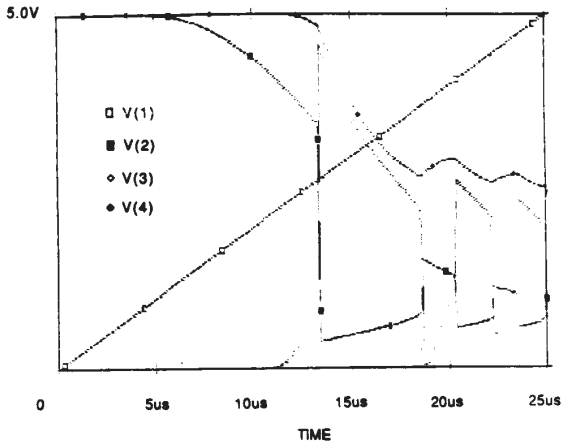


Fig. 2. SPICE output of NTC.

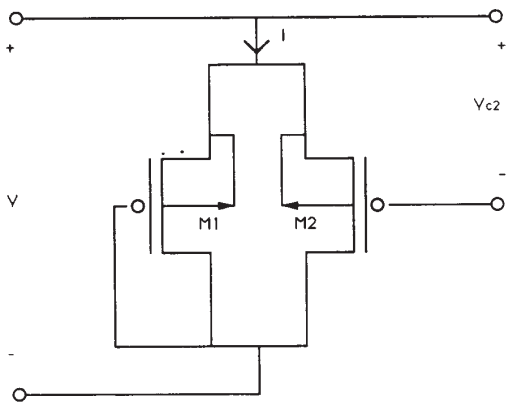


Fig. 3. Enhancement-type PMOS linear resistor.

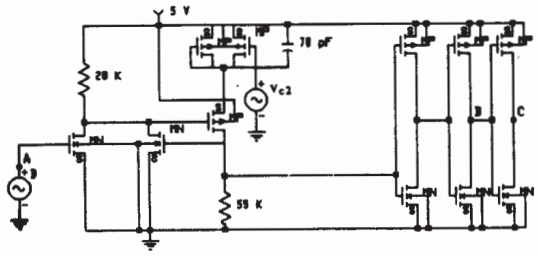


Fig. 4. NTC with a MOS resistor and buffered inverters.

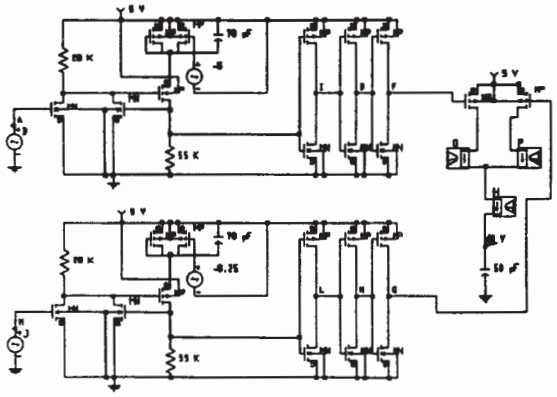
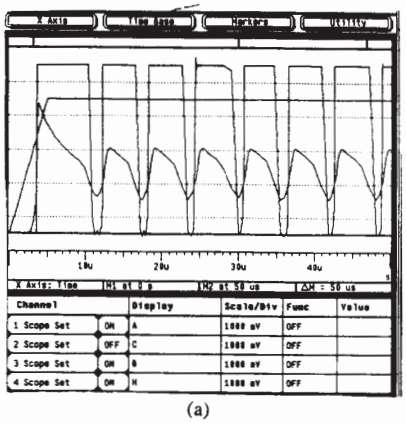
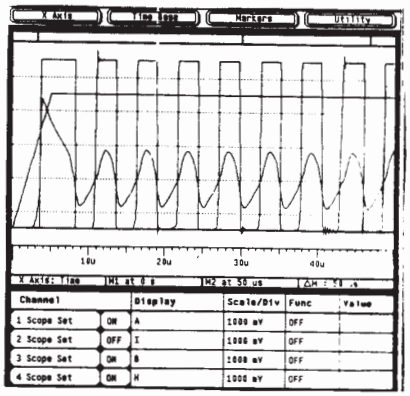


Fig. 5. CMOS circuit diagram for weighted summation.

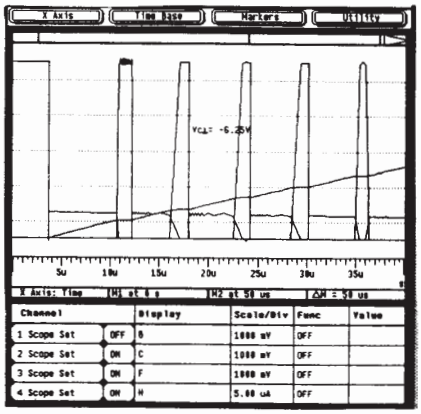


(a)

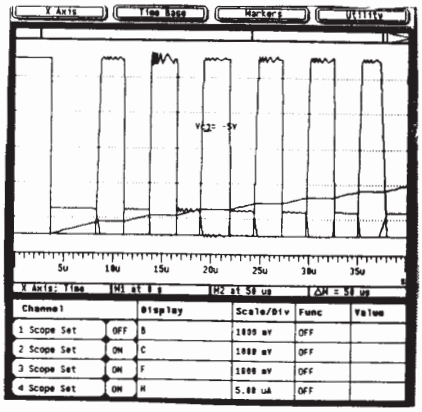


(b)

Fig. 6. Duty cycle changes with (a) V_{c2}=-6.25V, (b) V_{c2}=-5V.



(a)



(b)

Fig. 7. Charge accumulation of (a) V_{c2}=-6.25V, (b) V_{c2}=-5V.

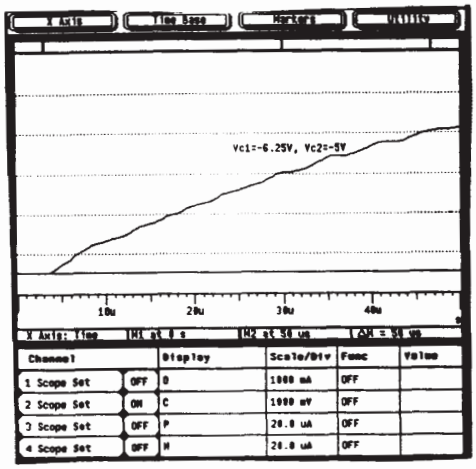


Fig. 8. Current summation of the two cases in Fig. 7.