A Novel Counter Circuit Using A Multi-level Neuron With A Self-Feedback Weight*

Jen-dong Yuh and Robert W. Newcomb
Microsystems Laboratory
Electrical Engineering Department
University of Maryland, College Park
Maryland 20742
e-mail: yuh@eng.umd.edu newcomb@eng.umd.edu

Abstract— In this paper, we use a single positive weight feedback multi-level neuron to design a multi-level counter. An energy function for this self-feedback weight neuron is shown. We design this neuron in the way that discrete neuron outputs are minimal points of the energy function. A circuit for the multi-level neural counter is demonstrated with Spice3e1 simulations included to show how this counter works.

I. INTRODUCTION

"A counter, by definition, is a device that records the number of events which have occurred" [1]. The input to an electronic counter usually consists of sequence of pulses, and the counter records the number of pulses which have happened during a given time. Normally, a number of logic gates and memory devices are used but here we show that a counter can be realized by a multi-level neuron. If we design the multi-level neuron appropriately, we can get an useful device. The multi-level neuron [2] has a self-feedback weight which connects the neuron output with the very input of the neuron. We propose an energy function for designing this neural counter. It turns out that we can design the neuron such that the minimal energy points are discrete neuron output levels. A circuit for a multi-level neural counter is shown in sections 3 and 4. This circuit counts the number of current input pulses. To lead into VLSI realization, Spice3e1 circuit simulations using MOSIS BiCMOS parameters are shown. Since neuron outputs can settle at any one of the discrete neuron outputs, the neuron can be used as a memory device too.

II. MULTI-LEVEL NEURON NONLINEARITIES

In the literature [3, 4, 5], most popular neuron nonlinearities are the hard-limiter, saturating linear elements,

and sigmoidal functions. These nonlinearities can be considered as two-level nonlinearities since there is only one sharp transition region of the neuron characteristic transfer function. Here, we use a nonlinearity that is different from others in the sense that neuron outputs have more than one sharp transition region [2]. This gives us certain advantages when we use it in some applications [6]. For illustration, an equation for the multi-level neuron nonlinearity is expressed as

$$M(x) = \sum_{j=1}^{b} a_j f_j(x - \theta_j) \qquad (1)$$

where M(.) is a multi-level nonlinearity which consists of b, $b > 0$, basis functions weighted by real nonnegative coefficients a_j. f is a monotonically nondecreasing step-type function, examples being tanh(.), 1(.), etc., and θ_j is a threshold. As a whole, M(.) is a monotonically nondecreasing step-type function. This monotonically nondecreasing property gives a base to propose an energy function for designing a multi-level neural counter. To design our multi-level neural counter, we choose f to be $\frac{1}{1+e^{-\lambda(x-\theta)}}$ and $a_j = 1$; then the multi-level nonlinearity, $M_b(.)$, is

$$M_b(x) = \sum_{j=1}^{b} \frac{1}{1 + e^{-\lambda(x-\theta_j)}} \qquad (2)$$

where λ is the gain factor for the nonlinearity.

III. A MULTI-LEVEL NEURON

A circuit diagram of a simple multi-level neuron with a self feedback weight is shown in Fig. 1, and described by,

$$C\frac{dx}{dt} = wv - xG + I_p \qquad (3)$$
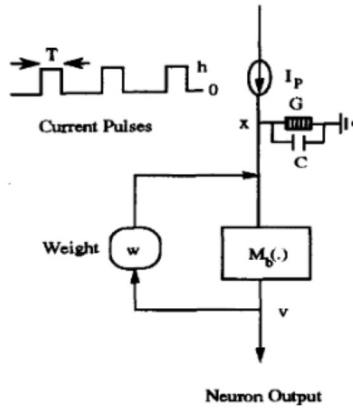
$$v(x) = M_b(x) \qquad (4)$$

Figure 1: A Self-Feedback Multi-Level Neuron Circuit

where C is the input capacitance, x is the voltage across the capacitor, w is the self-feedback weight, v is the neuron output, G is the input conductance, and I_p is a current pulse source with pulse height h, base value 0, and pulse width T. $M_b(.)$ is the multi-level neuron nonlinearity of Eq.(2). By appropriate design, we will see that this self-feedbeck neuron functions as a multi-level counter.

A. A Multi-level Nonlinearity Circuit for Neural Counters

A circuit for $M_b(.)$ is given in Figures 2 and 3. To implement a multi-level neuron nonlinearity, a Nonlinearity Building Block(NBB) circuit is demonstrated first. A NBB is implemented by a bipolar emitter coupled pair and CMOS transistor current mirrors. The output current of this NBB is a sigmoidal function of the difference input voltage $(x - \theta)$ as given in Fig. 2. By tying together outputs of b NBBs with different threshold points, we have a mutli-level nonlinearity circuit from which we design a neural counter. In Fig. 3, the output function in terms of the input, x, is given as

$$wM_b(x) = \alpha_F I_{EE} \sum_{j=1}^{b} \frac{1}{1 + e^{-\frac{(x-\theta_j)}{2V_T}}} \qquad (5)$$

We use a current mirror of I_{EE} to design a neuron weight for Fig. 2 of value $\alpha_F I_{EE}$. The input capacitance is just the parasitic capacitance. A more detailed circuit study about multi-level nonlinearties is given in [2].
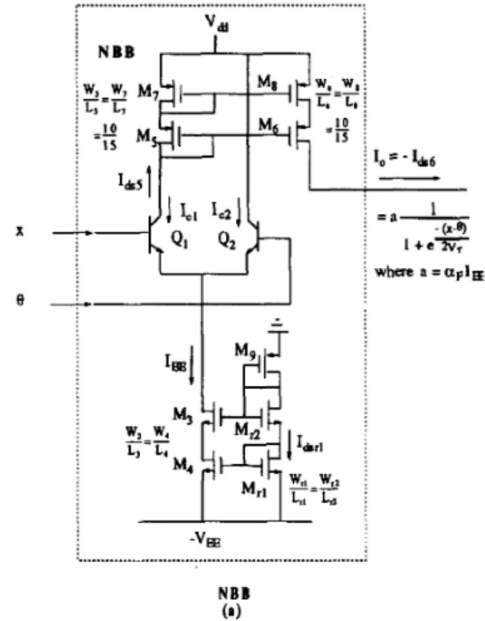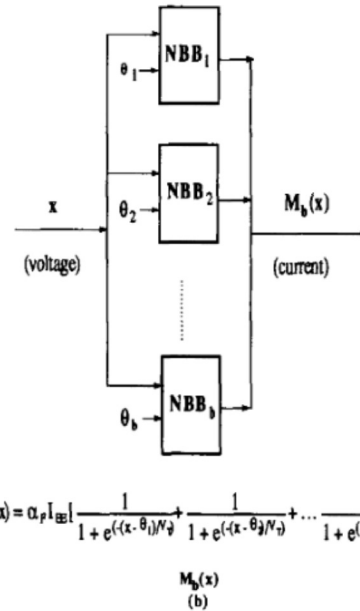

Figure 2: A Nonlinearity Building Block Circuit

$$M_b(x) = \alpha_F I_{EE} [\frac{1}{1 + e^{(-(x-\theta_1)/V_T)}} + \frac{1}{1 + e^{(-(x-\theta_2)/V_T)}} + \ldots \frac{1}{1 + e^{(-(x-\theta_b)/V_T)}}]$$

$M_b(x)$
(b)

Figure 3: A Multi-level Neuron Nonlinearity

IV. An Energy Function For Neural Counters

An energy function for a self-feedback multi-level neuron is

$$E_c = -(\frac{1}{2}wv^2 - G\int_0^x zdv(z) + I_p v) \qquad (6)$$

Here, w is the self-feedback weight, v is the neuron output, G is the input conductance, z is a dummy variable for integration of x, and I_p is sequence of current pulses with pulse width T and height h.

$$
\begin{aligned}
\frac{dE_c}{dt} &= \frac{dE_c}{dv}\frac{dv}{dx}\frac{dx}{dt} \\
&= -(wv - Gx + I_p)\frac{dv}{dx}\frac{dx}{dt} \\
&= -\frac{1}{C}(wv - Gx + I_p)^2\frac{dv}{dx} \qquad (7)
\end{aligned}
$$

Here, C is assumed to be positive, and $\frac{dv}{dx}$ is positive since $v = M_b(x)$ and the multi-level nonlinearity $M_b(.)$ we choose is a monotonically increasing function. Therefore, the above equation is an energy function since it is bounded for bounded v and decreases with time [6]. Assuming that the λ of $M_b(.)$ is large, and $I_p = 0$, an energy function vs the neuron output v is shown in Fig. 4 with $\theta_1 = 0.5, \theta_2 = 1.5, \theta_3 = 2.5, a = 1, w = 1, G = 1, b = 3$, and $\lambda = 40$. As we can see, there are $b + 1$ minima in Fig. 4. If we think of the neuron dynamics as for a ball rolling around this energy landscape, then when we input the current pulses, I_p, the input potential, x, will change and then the neuron output will change accordingly. I_p will push the neuron output, the ball, from one minimum to across a peak and then settle to another minimum. If we inject the proper amount of current, then each current pulse will only trigger a neuron advance of one output level each time. A positive current will move the ball to the right hand side of the x-axis and a negative current will move the ball to the left hand side of Fig. 4, since a positive current pulse increases the potential across the capacitor C and negative current does the opposite. To reset the counter, we ground the input, x = 0, so that the neuron output will return to the initial state. Therefore, this self-feedback neuron functions as a counter.

V. Circuit Simulations for Neural Counters

SPICE3e1 simulations for the neuron counter of Fig. 1 are shown in Figures 5 and 6 with BiCMOS parameters obtained from MOSIS. Current pulses of h = 4-μA of 1 MHz with pulse width T = 0.3 μ sec are the I_p for this counter. We can see in Fig. 5 that the neuron output is transitioning from one level to the next higher level after the occurrance of an input current pulse. The neuron output reaches the bth level after b-1 pulses. A negative current pulse will pull down one output level of the neuron
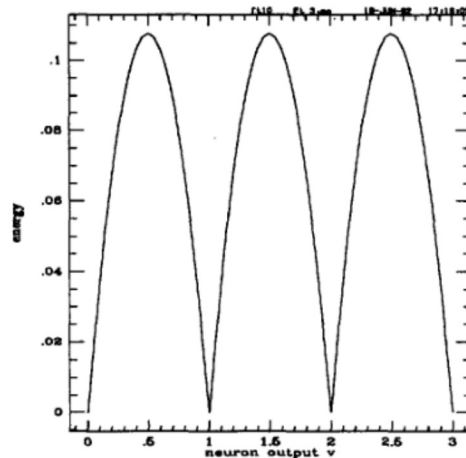

Figure 4: An Energy Function Plot Vs. the Neuron Output
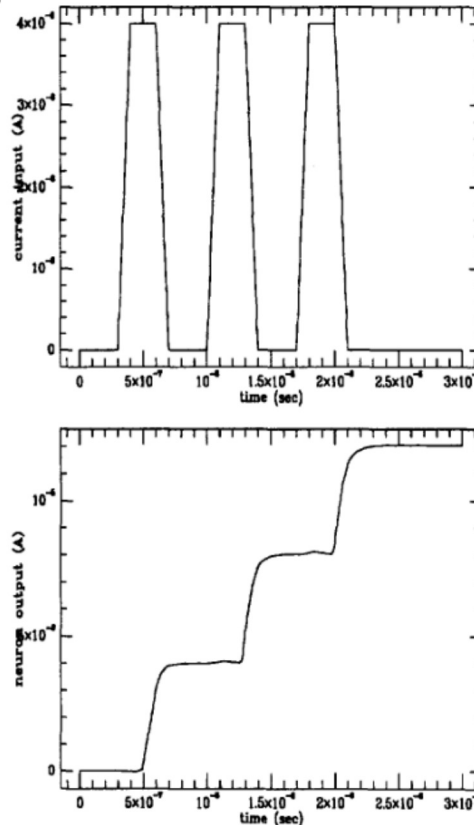

Figure 5: Input Current Pulses (Top) vs. Neuron Output Current (Bottom)

719

output current, as is demonstrated in Fig. 6. The neuron output is stable at any one of the possible levels since they are minimum points in the energy function we have shown above. The pulsewidth of I_p should be tuned so that each pulse will only trigger one output transition. The logic one is represented by a 4-μA neuron output current.
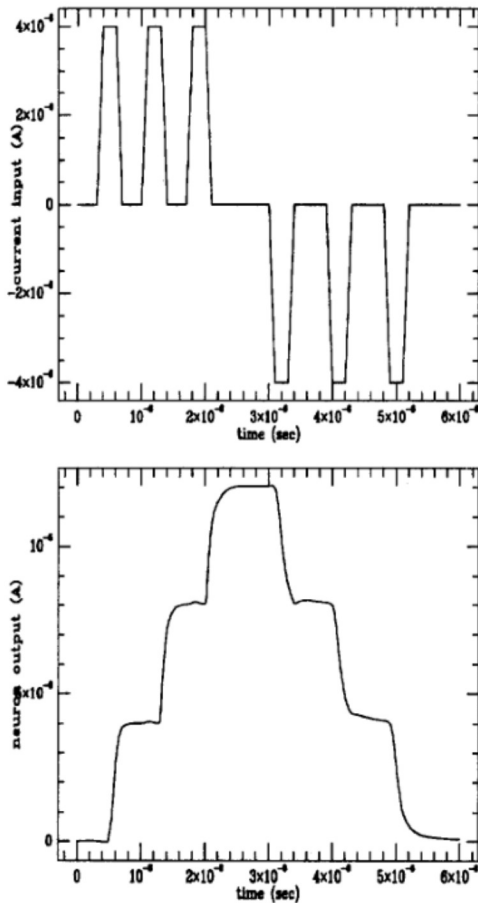

Figure 6: Input Current Pulses (Top) vs. Neuron Output Current (Bottom).

VI. Discussion and Conclusions

Instead of using a number of logic gates and memory devices, we have demonstrated a novel multi-level counter by using a single multi-level neuron. An energy function for this single multi-level neuron is shown in this paper. We design this neuron in the way that discrete neuron outputs are minimal points in the energy function. By providing a series of current pulses to the input of the neuron, the neuron functions as a counter. The circuit implementation of this multi-level neuron counter is shown in this paper. Spice3e1 simulations with MOSIS BiCMOS parameters demonstrate the successful design of the multi-level neuron counter. This simple neuron can be also used as a multiple-valued memory device, since it is stable at $b + 1$ minimum energy points.

References

[1] Thomas C. Bartee. *Digital Computer Fundamentals*. McGraw-Hill inc, 1966.

[2] J.D. Yuh and R.W. Newcomb. Circuits for multi-level nonlinearities. In *Proceedings of the International Joint Conference on Neural Networks*, volume 11, pages 27–32, June 1992.

[3] J.J. Hopfield. Neural networks and physical systems with emergent collective computational abilities. In *Proceedings of National Acadamy of Science USA*, pages 2554–58, April 1982.

[4] R.P. Lippmann. An introduction to computing with neural nets. In *IEEE ASSP Magazine*, volume 4, pages 4–21, April 1987.

[5] J.J. Hopfield. Neuron with graded response have collective computational properties like those of two-state neurons. In *Proceedings of National Acadamy of Science USA*, volume 81, pages 3088–3092, May 1984.

[6] J.D. Yuh and R.W. Newcomb. A multi-level neural network for A/D conversion. *IEEE Transactions on Neural Networks, in press*, May 1993.