AN ADJUSTABLE THRESHOLD MOSFET *

Suan-Wei Tsay and Robert W. Newcomb
Microsystems Laboratory
Electrical Engineering Department
University of Maryland
College Park, MD 20742 USA
Phone: (301) 405-3662
Fax: (301) 314-9281

Abstract

A circuit which is equivalent to a voltage adjustable threshold MOSFET is presented. This adjustable threshold MOSFET uses the voltage adder from a neural arithmetic unit which is based on the describing equations of the neural chemical pools that occur in biological neurons. The threshold voltage of this adjustable threshold MOSFET is linearly modulated by an external control voltage.

1 Introduction

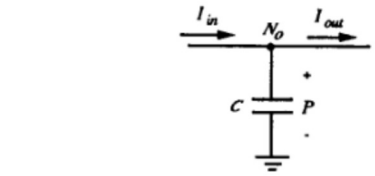
An adjustable threshold MOSFET is of interest because it can be used as the adaptive weight in neural network systems. Using the chemical modulation functions in biological neurons we can build a voltage adder and, as we show here, this leads to the construction of the adjustable threshold MOSFET. To realize the chemical modulation functions in biological neurons, chemical pools are utilized by D. A. Hartline [1][2] to simulate the chemical-electrical interactions in biological neurons. From the view of synthesis and degradation of the chemical materials, the intrinsic describing equation of a chemical pool can be written as

$$C\frac{dP}{dt} = I_{in} - I_{out} \tag{1}$$

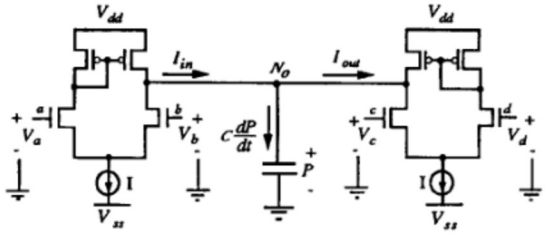
where C is the pool volume, P is the concentration of chemical materials in the pool and I_{in} and I_{out} represent the rates of chemical material flowing into and out of the pool, respectively. I_{in} and I_{out} can be modulated by the pool level (concentration) of other pools or by the same pool. The equilibrium state of the pool is determined when I_{in} equals I_{out}. By controlling their I_{in} and I_{out}, these pools can be made into an arithmetic unit for processing signals by adding, subtracting, or sign inverting voltage signals [4]. Here a voltage adder is used to make an equivalent circuit for an n-type adjustable threshold MOSFET. P-type adjustable threshold MOSFETs can also be made by the same techniques.

2 Basic Circuit

The basic circuit to realize (1) is depicted in Fig. 1(a) where the capacitor represents a pool and the voltage across the capacitor represents the pool level (material concentration) of the pool. The amount of the chemical material is represented by the charge in the capacitor. When the simplest modulation function, that is, linear modulation, is applied on the currents I_{in} and I_{out}, Fig. 1(a) is converted into Fig. 1(b). To linearly modulate I_{in} with the difference $V_a - V_b$, we use the circuit to the left of the capacitor, and, similarly, to linearly modulate I_{out}, with respect to $V_c - V_d$, the circuit to the right. In this circuit all transistors are assumed to work in their saturation region.



(a)



(b)

Figure 1:A pool circuit, the background circuit for a neural arithmetic unit. (a) The intrinsic circuit of a chemical pool. (b) The pool for inward and outward currents being linearly modulated by other signals. N_o is the output node with output voltage P.

Research supported by ONR Grant No. N00014-90-J-1114.

0-7803-0593-0/92 $3.00 1992 IEEE

3 Arithmetic Functions

Three arithmetic functions can be easily derived from the neural arithmetic unit (NAU) circuit of Fig. 1(b). To get addition we tie node b to N_o and c to ground. With this arrangement the inward and outward currents of this pool will be

$$I_{in} = K(V_a - P) \quad \text{and} \quad I_{out} = K'(0 - V_d) \tag{2}$$

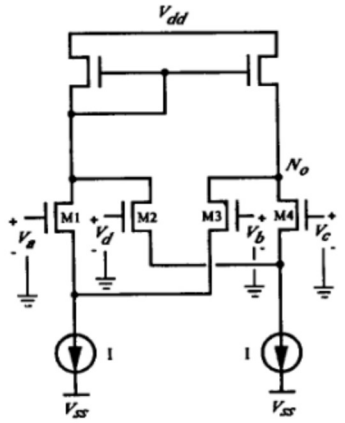
where K and K' are constants that depend on the geometry of the MOS transistors in the differential pairs used in Fig. 1(b). If these two differential pairs are identical, the constants K and K' will be equal. At the equilibrium state I_{in} is equal to I_{out}, that is, $(V_a - P) = (0 - V_d)$. In this case we get

$$P = V_a + V_d \tag{3}$$

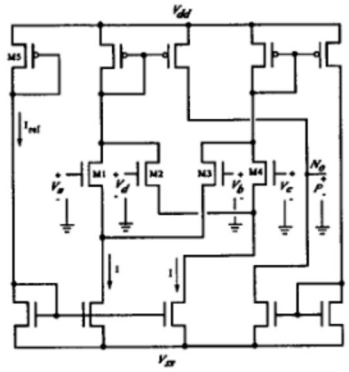
Equation (3) shows that Fig. 1(b) can be viewed as a voltage adder under the conditions used ($b = N_o$, $c = GND$). Two other functions, subtraction and sign inversion can also be realized by different arrangement of the input voltages of the two differential pairs and are given in [4].

4 Actual Circuit Layout

The circuit shown in Fig. 1(b) can be simplified into the circuit of Fig. 2(a) where the two differential amplifiers are combined. The capacitor in the NAU is also removed, and, thus, replaced by the parasitics of the circuit. This forces the circuit to its equilibrium point very rapidly. Figure 2(b) shows the circuit used in constructing an NAU. In order to increase the range of the input voltages and the accuracy of the results, we can also cascode the current mirrors in Fig. 2(b) or replace them by the MOS regulated cascode current mirrors as depicted in [5, p.352]. Figure 3 shows the PSPICE simulation for the voltage adder as described in (3).



(a)



(b)

Figure 2:(a) Simplified NAU. (b) Actual circuit for an NAU.

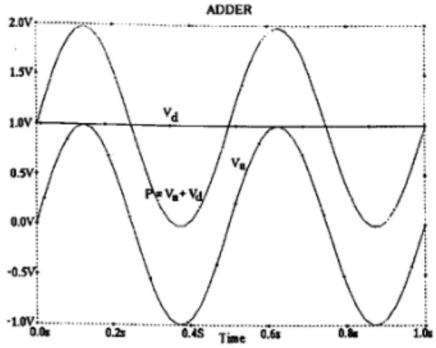


Figure 3:The PSPICE simulation results for a voltage adder from the NAU of Fig. 2(b) with $V_b = P$ and $V_c = 0$.

5 Adjustable threshold MOSFET

The realization of an adjustable threshold MOSFET is straightforward with an NAU adder in hand. Figure 4(a) shows an n-type MOSFET, M_1, whose threshold voltage is modulated by the control voltage V_c. The left-hand part of Fig. 4(a) is a voltage adder with the output, using (3),

$$V_g' = P = V_g + V_c. \tag{4}$$

We can use Fig. 4(a) to define a new 4-terminal device of terminals c, d, g, and s, symbolized by Fig. 4(b) and called an adjustable threshold MOSFET. If we assume the threshold voltage of transistor M_1 to be V_t' and the effective gate-to-source voltage to be the gate-to-source voltage minus its threshold voltage, the effective gate-to-source voltage of an adjustable threshold MOSFET will be

$$V_g' - V_s - V_t' = V_g + V_c - V_s - V_t' = V_g - V_s - V_t \tag{5}$$

Equation (5) defines V_t in terms of V_g', the voltage on the gate of M_1 as shown in Fig. 4(a). The threshold voltage for the four terminal element of Fig. 4(b) is, consequently,

$$V_t = V_t' - V_c \tag{6}$$

A PSPICE simulation of this adjustable threshold n-type MOSFET is shown in Fig. 5. The six curves represent the drain currents with the control voltage V_c swept from 0V to 1V in 0.2V steps. The effective threshold voltages are shown to be about 1V when V_c = 0V and about 0V when V_c = 1V and vary almost linearly between these ranges.

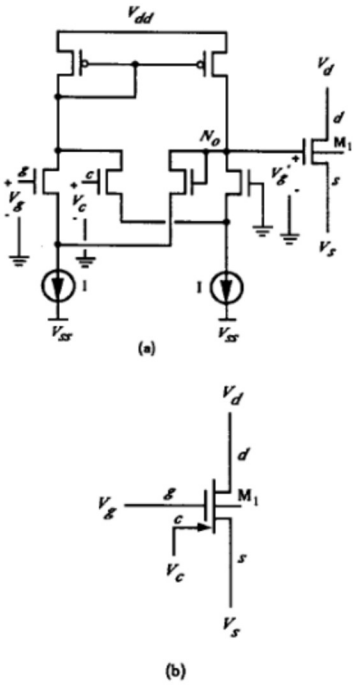


Figure 4:An adjustable threshold n-type MOSFET. (a) The gate voltage of M_1 is tied to the output of a voltage adder so that the threshold voltage can be modulated by the control voltage V_c. (b) The symbol for an adjustable threshold n-type MOSFET.

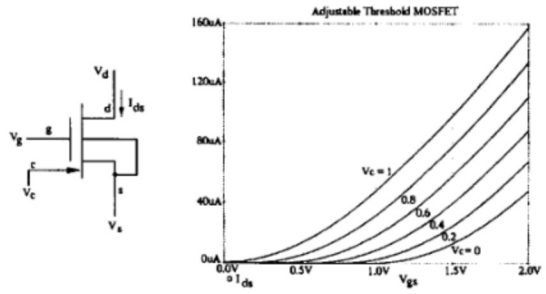


Figure 5:Simulation of an adjustable threshold n-type MOSFET using an adder from NAU.

6 Conclusions

This paper presents a way to make an adjustable threshold MOSFET by using the voltage adder which is derived from the circuit of a chemical pool in biological neural systems. The circuits used here are all composed of MOS transistors and no resistor is used to convert current to voltage. Thus, these circuits will only occupy a small die area and are very suitable for VLSI realizations.

References:

[1] D. K. Hartline, "*Simulation of Restricted Neural Networks with Reprogrammable Neurons*," IEEE Transactions on Circuits and Systems, Vol. 36, No. 5, May 1989, pp. 653-660.

[2] D. K. Hartline, "*Synetsim 3.3 Users' Manual*," Bekesy Lab., Honolulu, HI, 1990.

[3] S. W. Tsay, N. El-Leithy, and W. Newcomb, "*CMOS Realization of a Class of Hartline Neural Pools*," Proceedings of the IEEE International Symposium on Circuits and Systems, New Orleans, May, 1990, Vol. 3, pp. 2417-2420.

[4] S. W. Tsay and R. Newcomb, "*A Neural-Type Arithmetic Unit*," Proceedings of the IEEE International symposium on Circuits and Systems, Singapore, June, 1991, pp. 2519-2521.

[5] R. Geiger, P. Allen, and N. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, McGraw-Hill, New York, 1990.