Analysis and Operation of a Neural-Type Cell (NTC)

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Abstract

Analysis of the operation of a neural-type cell is presented. The modeling for the neural-type cell in different operation regions is presented and related analytical equations are derived. From these equations, output pulse rate of the neural-type cell can be determined in a closed form. The results obtained are important to the field of neural-type networks since the information can be used in the design of neural-type systems.

I. Introduction

Analog pulse modulation techniques in artificial neural networks draw considerable attention since these neural networks mimic the actual operation of biological neural networks. A basic processing element for this type of neural network is the neural-type cell (NTC) [1], which encodes input stimuli (voltage) into pulse rates of an output signal. The coding and generation of pulses in the NTC are known to rely on nonlinear hysteresis characteristics [2][3] and, thus, until now there was no way to predict or handle this coding in a NTC. It is, however, important to have a design theory for the coding of the pulses so that one can do information processing.

In this paper, the operation of an NTC is divided into several different regions depending on operation conditions of the transistors in the NTC, and analytical equations for important design variables are derived for each region. With these equations it is possible for us to predict and design a rise time, a fall time, and amplitude of the NTC pulses. This will help us to design and build neural networks, as intended, based on neural-type cells.

II. Cell Operation

The CMOS circuit for the neural-type cell (NTC) under consideration is shown in Fig. 1. For this circuit, with appropriate chosen values [4], oscillations, as shown in Fig. 2, result at the output (V4), and their frequency increases as the input voltage (V1) increases. For analytic treatment V1 and V4 versus time are redrawn in Fig. 3 to show important points. Here, we partition the signals into the five important regions along the time-axis. Table 1 lists the different operational conditions for transistors M1, M2, and M3 of Fig. 1. From these results, the following analytical equations are derived. These equations are derived by using standard equations [5] for transistors in the various states as determined in Table 1 with a given V1.

At the time that M2 turns on [see Fig. 1 and Fig. 3], $V1 = V_b$ where:

$$V_b = V_{tn} + \sqrt{\frac{(-2V_{tp})}{K_n(W1/L1)R4}} \qquad [1]$$

where V_{tn} and V_{tp} are the threshold voltages of an N-type and P-type transistors, respectively. K_n and K_p are the process gain factors for N-type and P-type transistors.

At the time that M3 turns on, V4 attains its highest value when in a pulsing mode. This high value depends in turn on the state of M1.

$$V4_{max} = Vdd - \left[\frac{K_n W1}{2\ L1}(V1-V_{tn})^2\right] * R4 - V_{tp} + \left(\frac{2V_{tn}}{K_p R5}\ \frac{L2}{W2}\right)^2 \qquad [2]$$

when transistor M1 is operating in saturation region, or,

$$V4_{max} = \frac{\frac{1}{R4} + K_n\frac{W1}{L1}(V1-V_{tn}) - \left\{\left[\frac{1}{R4} + K_n\frac{W1}{L1}(V1-V_{tn})\right]^2 - 2K_n\frac{W1Vdd}{L1\ R4}\right\}^{\frac{1}{2}}}{K_n\frac{W1}{L1}}$$

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$$-V_{tp}+\left(\frac{2V_{tn}}{K_p R5}\frac{L2}{W2}\right)^2 \qquad [3]$$

when transistor is in linear region.

When M3 turns off, V4 is at its minimum:

$$V4_{min} = (R_{eq} + R5) *$$
$$\left\{\left(\frac{V4_{max}}{R_{eq}+R5} - \frac{Vdd}{R_{eq}+R5+R6}\right) \exp\left(\frac{T_f}{RC}\right) + \frac{Vdd}{R_{eq}+R5+R6}\right\} \qquad [4]$$

In the above M2 is considered to be a linear resistor (R_{eq}) when in the ohmic region and a square law current source when in the saturation region. Using the value of equations [3] and [4] as end points, the times between peaks and valleys are determined as:

$$T_f=t_d-t_c = -RC*\ln\left\{\frac{V_{tn} - \frac{R5*Vdd}{R_{eq}+R5+R6}}{\frac{R5*V4_{max}}{R_{eq}+R5} - \frac{R5*Vdd}{R_{eq}+R5+R6}}\right\} \qquad [5]$$

where

$$R_{eq} = \left[K_p \frac{W2}{L2}(|V_{gs2,ave}|-|V_{tp}|)\right]^{-1}$$

and

$$R = (R_{eq} + R5)*R6/(R_{eq} + R5 + R6)$$

$$T_r = t_c - t_d = -C*R6*\ln\left(\frac{V4_{max}-Vdd+I2_{ave}*R6}{V4_{min}-Vdd+I2_{ave}*R6}\right) \qquad [6]$$

$$\text{Period} = T_f + T_r \qquad [7]$$

where V_{gs2ave} and $I2_{ave}$ are average values of V_{gs2} in region 4 and I2 in region 5, respectively.

III. Simulation Results

SPICE simulation is used in order to check the analytical equations above. For this we used the values:

Vdd = 5, K_n = 100E-6, K_p = 50E-6,
W1/L1 = 8/8(um), W2/L2 = 48/8,
W3/L3 = 20/8, R4 = 20K, R5 = 55K,
R6 = 90K, C = 30E-12, and input V1 = 4.

SPICE gives: V_b = 1.4, $V4_{max}$ = 3.49, $V4_{min}$ = 2.79, and Period = 2.9E-6 [Fig. 4]. By comparison analytical equations [1], [2], [3], [4] and [7] give V_b = 1.6, $V4_{max}$ = 3.03, $V4_{min}$ = 1.95, and Period = 2.55E-6.

V. Conclusions

In the above we have given the rising semi-period time, the falling semi-period time, and the maximum and minimum amplitude for the neural-type pulses in an NTC. Although they are only approximate, because they are derived from simplified circuits based on physical reasoning, they do give reasonable numbers for initial design purposes as is seen by comparing with the results of the SPICE simulations. Thus, with these equations, we are now able to control the pulse rates more precisely by adjustment of circuit parameters. The results of this paper will help in the engineering design of pulse coded neural-type networks.

References

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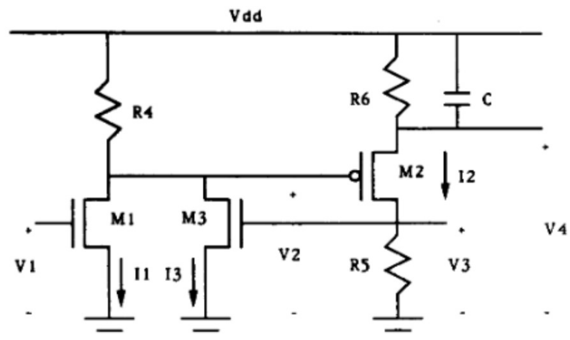


Fig. 1. Neural Type Cell.

Table 1. Different regions depending on the operating condition.

	Region numbers				
	1	2	3	4	5
M1	OFF	LIN SAT	LIN SAT	LIN	LIN
M2	OFF	OFF	SAT	LIN	SAT
M3	OFF	OFF	OFF	LIN	OFF

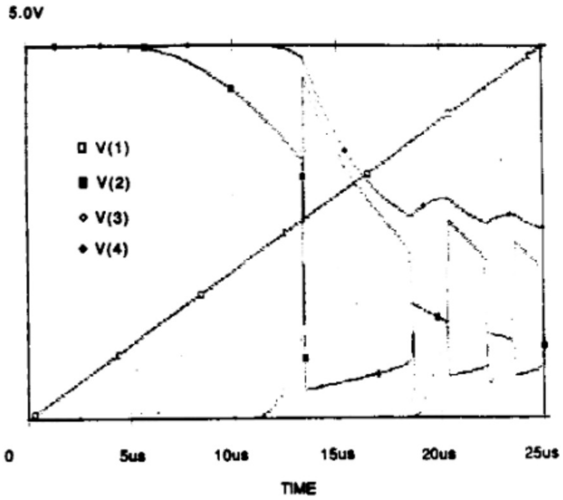
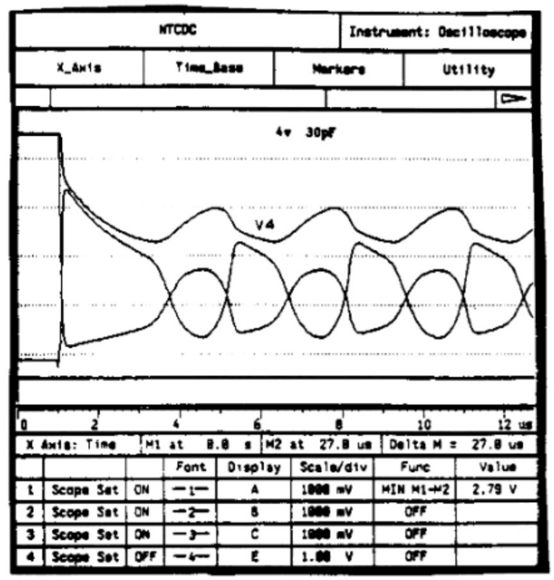


Fig. 2. SPICE output of NTC.



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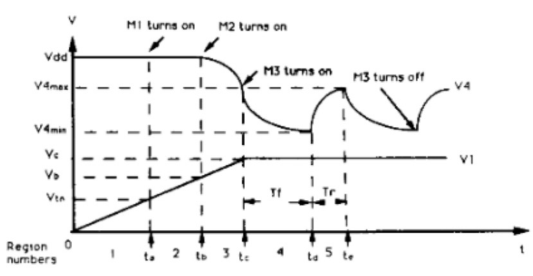

Fig. 3. Input (V1) - Output (V4) relation of NTC.

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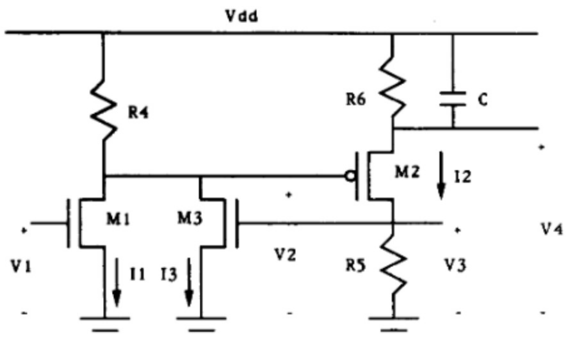

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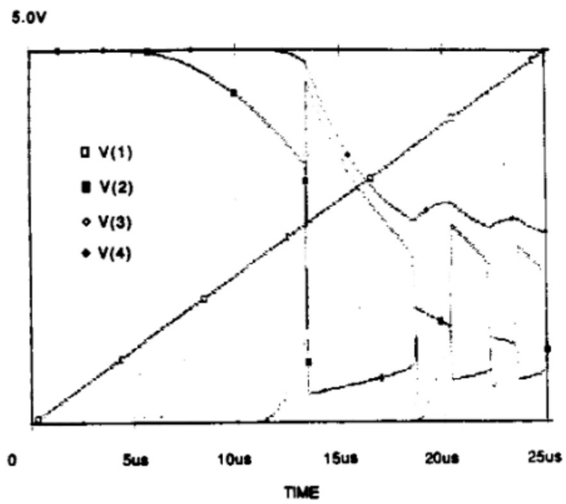

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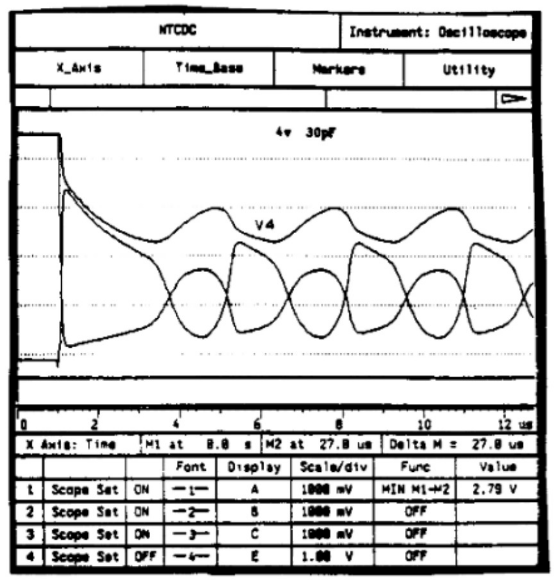

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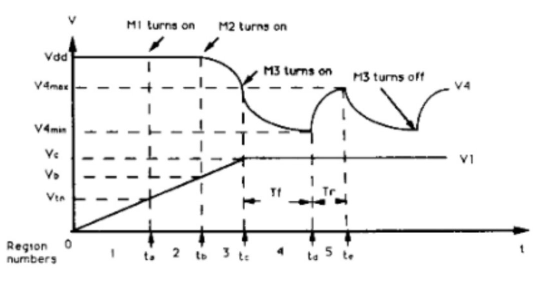

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