A Semistate Description for Hysteresis in MOS Neural-Type Cells*&

G. Wolodkin*, N. El-Leithy*&, M. de Savigny&,
S. W. Tsay& and R. Newcomb*&
Microsystems Laboratory
Electrical Engineering Department
University of Maryland
College Park, MD 20742 USA
phone: (301) 454-6869
email: newcomb@bagend.eng.umd.edu

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Abstract

This paper utilizes semistate theory to give a new means of viewing the hysteresis developed in an MOS neural-type cell. The current which feeds an RC load is represented in terms of single valued functions within the semistate equations with some node voltages considered as parameters. When these parameters are eliminated, via equations or SPICE simulations, hysteresis is found to be present for certain element value and input voltage choices.

I. Introduction

Hysteresis is recognized as an important element in biological neural systems [1]. That being the case, it is interesting to see that some neural network electronic circuit designs rely upon hysteresis to achieve their effects [2]-[5]. In particular, we have known for some time that hysteresis in the neural-type cell (NTC) forms the basis for its spike generating properties [6][7]. However, the hysteresis in the NTC is rather complicated with dependencies upon the cell input voltage and the circuit parameters that as yet have not been characterized analytically. In an effort to lend greater insight into these characterizations, we develop here a means of looking at the generation of this hysteresis which gives considerable physical insight into the parameters determining its formation and shape. In Section II we describe the NTC by setting up the semistate equations which characterize it and then reducing them to those describing the hysteresis. Based upon these semistate equations, in Section III we present SPICE runs showing both the final hysteresis obtained along with the intermediate steps leading to the hysteresis.

II. The NTC and Its Semistate Description

Figure 1 shows the NTC where the output is taken as v_3 and input as v_1. With the presence of the feedback transistor M_3 the circuit is found to oscillate with a proper choice of element values over a limited range of inputs. On investigating the source of this oscillation it has been found that the R_6-C combination sees an i-v characteristic which has hysteresis and that this hysteresis is rather nontraditional. To characterize it mathematically we desire the drain current, $-i_2$, of M_2 to be represented as a function of the voltage v_4. Consequently, after removing R_6-C, we desire to place a voltage source of voltage v_4 at the source of M_2 and then measure the current i_2. When hysteresis is present a multiple-valued function results. To reduce the problem to one of single-valued functions, we place another voltage source v_3 across R_5 and then get two characterizations for the current i_2, one through the source v_4 and one through R_5. Where these two characterizations have a common value is the solution for the circuit and where there are multiple solutions there is hysteresis. This process is to be interpreted as the resistor R_5 yielding a load line on the i-v curve of the circuit it sees.

Because we are looking for common solution of some subcircuits it is convenient to formulate the problem via the semistate equations [8] which can be used to incorporate the individual subcircuits. The semistate equations are obtained by breaking the circuit into three smaller circuits, as shown in Fig. 1. For the MOS transistors, we will assume that the gate current, i_g, is zero, while the drain current, i_d, is some non-linear function of the gate-to-source and drain-to-source voltages. This yields

$$i_g = 0, \quad i_d = f(v_{gs}, v_{ds}) \qquad (1a,b)$$

Notice that proper sign choices for the NMOS and PMOS variables can result in identical current equations for all transistors. With this in mind, we denote each transistor, its associated drain current, and the subcircuit containing it by the subscript i. The canonical semistate equations are of the basic form

$$EX = A(X) + BU \qquad (2a)$$
$$Y = CX \qquad (2b)$$

where E, B, and C are constant matrices and $A(\cdot)$ is a nonlinear vector valued function; U is the subcircuit input vector, Y the subcircuit output vector, and X the subcircuit semistate vector. With no dynamics in the circuit, as will be the case for the hysteresis determination, dX/dt will be zero and the semistate equation (2a) becomes

$$-A(X) = BU \qquad (2c)$$

For the input stage,

$$X_1^T = [v_1, v_2] = [X_{11}, X_{12}] \qquad (3a)$$
$$U_1^T = [v_1, i_3] = [U_{11}, U_{12}] \qquad (3b)$$
$$Y_1 = v_2 \qquad (3c)$$

and, thus, in canonical form,

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$$\begin{bmatrix} 1 & 0 \\ 0 & -G_4 \end{bmatrix} X_1 + \begin{bmatrix} 0 \\ G_4 V_{dd} - f_1(X_{11}, X_{12}) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} U_1 \qquad (3d)$$

$$Y_1 = [0, 1] X_1 \qquad (3e)$$

For the output stage, consisting of M_2,

$$X_2^T = [i_2, v_2, v_3, v_4] \qquad (4a)$$
$$U_2^T = [v_2, v_3, v_4] \qquad (4b)$$
$$Y_2 = [i_2] \qquad (4c)$$

giving the canonical form equations

$$\begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} X_2 + \begin{bmatrix} f_2(X_{24}-X_{22}, X_{24}-X_{23}) \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} U_2 \qquad (4d)$$

Finally the feedback stage, written as

$$X_3^T = [i_3, v_2, v_3] \qquad (5a)$$
$$U_3^T = [v_2, v_3] \qquad (5b)$$
$$Y_3 = i_3 \qquad (5c)$$

$$\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ -1 & 0 & 0 \end{bmatrix} X_3 + \begin{bmatrix} 0 \\ 0 \\ f_3(X_{33}, X_{32}) \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \end{bmatrix} U_3 \qquad (5d)$$

The above describe the circuit with R_6-C and R_5 removed. The constraints used to connect the subcircuits are

$$Y_1 = U_{21} = U_{31} = v_2 \qquad (6a)$$
$$Y_3 = U_{12} = i_3 \qquad (6b)$$
$$Y_2 = Y = i_2 \qquad (6c)$$

and we notice that many of the semistate variables are identical. Thus,

$$X_{12} = X_{22} = X_{32} = v_2 \qquad (7a)$$
$$X_{23} = X_{33} = v_3 \qquad (7b)$$

Combining the three subcircuits yields 9 equations, 3 of which are redundant. In removing them, we are left with the basic canonical semistate equations, of which there are 6, where

$$X_T = [v_1, v_2, v_3, v_4, i_2, i_3] \qquad (8a)$$
$$U_T = [v_1, v_3, v_4] \qquad (8b)$$

$$\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & G & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} X + \begin{bmatrix} 0 \\ f_1(X_1, X_2) + X_6 - G_4 V_{dd} \\ 0 \\ 0 \\ -f_2(X_4-X_2, X_4-X_3) \\ -f_3(X_3, X_2) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} U \qquad (8c)$$

$$Y = [0, 0, 0, 0, 1, 0] X \qquad (8d)$$

By eliminating i_3, taking i_2 & v_2 as the reduced semistate, choosing v_1 & v_4 as parameters, and v_4=u as the input with i_2=y as the output, a reduced semistate representation becomes

$$\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} X_r = \begin{bmatrix} V_{dd} - R_4[f_1(v_1, v_2) + f_3(v_3, v_2)] \\ f_2(v_4-v_2, v_4-v_3) \end{bmatrix} \qquad (9a)$$

$$y = [0,1] X_r \qquad (9b)$$

where the input is considered to be v_3 and

$$X_r^T = [v_2, i_2] \text{ and } R_4 = 1/G_4 \qquad (9c,d)$$

In (9a) we substitute v_2 of the first row to get, from the second row, i_2 as a function of v_1, v_4 as parameters and v_3 as independent variable. The result is a set of curves of i_2 versus v_3 parameterized by v_1 and v_4. These need to be intersected with the load line coming from

$$i_2 = G_5 v_3 \qquad (9e)$$

To solve these for i_2=y versus v_4=u we can eliminate v_2 after first representing the drain current using the standard form [9, p. 51]

$$f(x,y) = \begin{cases} 0 & x < V_T \\ \beta\,[2(x - V_T)y - y^2] & x - V_T > y \\ \beta\,(x - V_T)^2 & x - V_T < y \end{cases}$$

(off) (10a)
(ohmic) (10b)
(saturated) (10c)

III. Hysteresis Determination

PSPICE runs were used to gain solutions to the above equations. The ORSPICE circuits to do this are shown in Figs. 2 & 3 with the resulting graphs appearing in Figs. 4 and 5. In Fig. 4, the output current i_2 is plotted vs. v_3, with v_4 as a parameter (over the range 5 to 7.8V in 0.4V steps). Intersections of these curves with the load line of R_5, also shown in Fig. 4 as the linear curve, indicate possible operating points of the cell. For small v_4 there is only one solution for i_2, and similarly for large v_4. Notice, however, that for 7.85V < v_4 < 8.5V, i_2 becomes multiple-valued, and as v_4 is swept through this range, hysteresis will result. This is verified in Fig. 5. Circuit parameters for these runs were as follows: R_4 = 1KOhm, R_5 = 7.5KOhm, V_{dd}=10, v_1 = 4V. For the transistors MOSIS 2 micron CMOS parameters of Run M95C (of

the vender ORBIT) were used at level 2 with W/L ▫ 20 for M_1 and M_2, 6 for M_3.

IV. Discussion

In the above we have determined the semistate equations which characterize the operation of the NTC. These semistate equations are in terms of single-valued functions, but their nondynamical solutions are multi-valued, containing the desired hysteresis. This hysteresis results for only a small range of the input and circuit element values though as yet no precise design characterization exists. However, with the presence of an analytic tool, such as semistate theory, there is some hope that design formula can be obtained. It is in that spirit that we have set up the semistate equations in the form given above which when combined with PSPICE has allowed the design of operational NTCs through geometrical determination of the hysteresis described here. Much remains to be done and in particular to integrate these results with neural-type junctions [10].

References

[1]. G. W. Hoffmann, "A Neural Network Model Based on the Analogy with the Immune System," Journal of Theoretical Biology, Vol. 122, 1986, pp. 33 - 67.

[2]. N. El-Leithy and R. W. Newcomb, "Hysteresis in Neural-Type Circuits," Proceedings of the 1988 IEEE International Symposium on Circuits and Systems, Espoo, Finland, June 1988, pp. 993 - 996.

[3]. C. Cole, A. Wu and J. Meador, "A CMOS Impulse Neural Network," Proceedings of the 1989 Microelectronics Conference, preprint.

[4]. C. K. Kohli, R. C. Ajmera, G. Kiruthi, and R. W. Newcomb, "Hysteretic System for Neural-Type Circuits," Proceedings of the IEEE, Vol. 69, No. 2, February 1981, pp. 285 - 287.

[5]. B. Linares-Barranco, E. Sánchez-Sinencio, A. Rodriguez-Vázquez, and J. L. Huertas, "A Programmable Neural Oscillator Cell," IEEE Transactions on Circuits and Systems, Vol. 36, No. 5, May 1989, pp. 756 - 761.

[6]. C. K. Kohli and R. W. Newcomb, "Voltage Controlled Oscillations in the MOS Neural Line," Proceedings of the Twentieth Midwest Symposium on Circuits and Systems, Texas Tech University, August 1977, pp. 134 - 138.

[7]. R. W. Newcomb, "MOS Neuristor Lines," in Constructive Approaches to Mathematical Models, C. V. Coffman and G. J. Fix, editors, Academic Press, Reading, MA, 1979, pp. 87 - 111.

[8]. R. W. Newcomb and B. Dziurla, "Some Circuits and Systems Applications of Semistate Theory," Circuits Systems Signal Processing, Vol. 8, No. 3, 1989, pp. 235 - 260.

[9]. D. A. Hodges and H. G. Jackson, "Analysis and Design of Digital Integrated Circuits," McGraw-Hill Book Co., NY, 1983.

[10]. N. El-Leithy, R. W. Newcomb, and M. Zaghloul, "A Basic MOS Neural-Type Junction: A Perspective on Neural-Type Microsystems," Proceedings of the IEEE First International Conference on Neural Networks, San Diego, CA, June 1987, pp. III-469 - III-477.

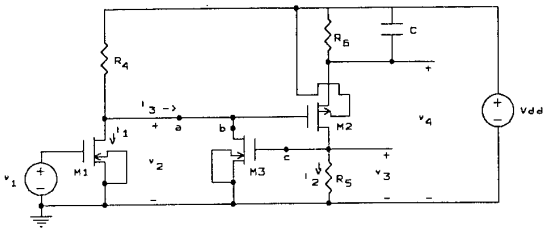

Figure 1. Neural-Type Cell (NTC)

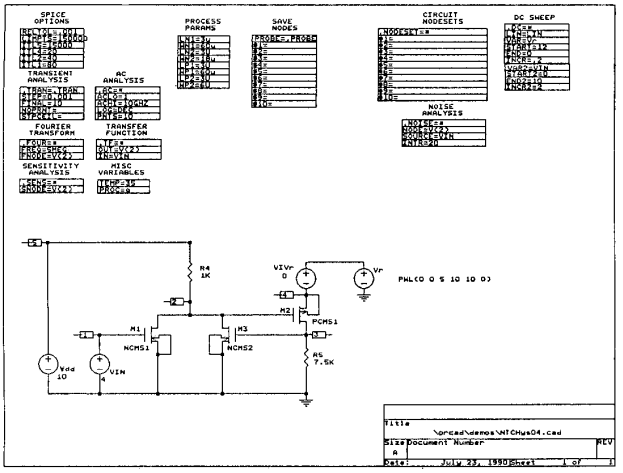

Figure 2. ORSPICE Circuit for Fig. 4

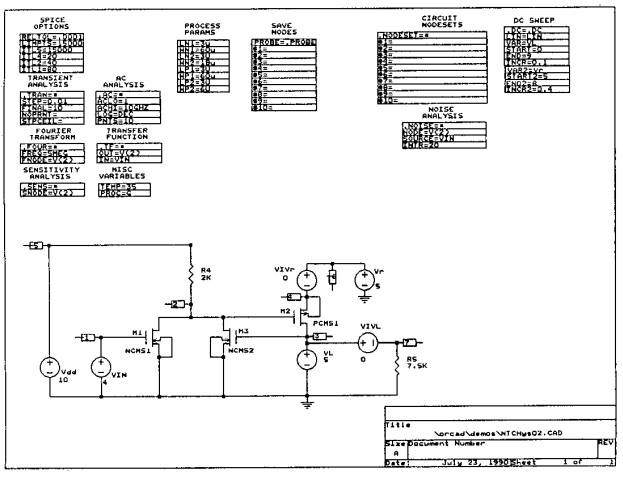

Figure 3. ORSPICE Circuit for Fig. 5

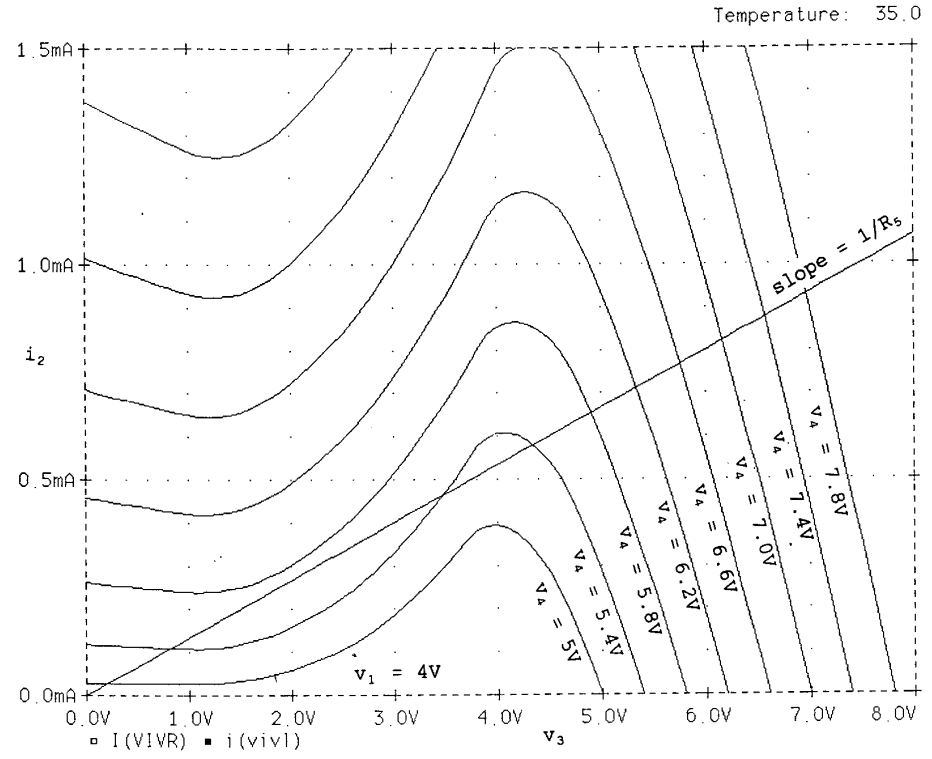

Figure 4. Parametrized DC Output of MOS NTC

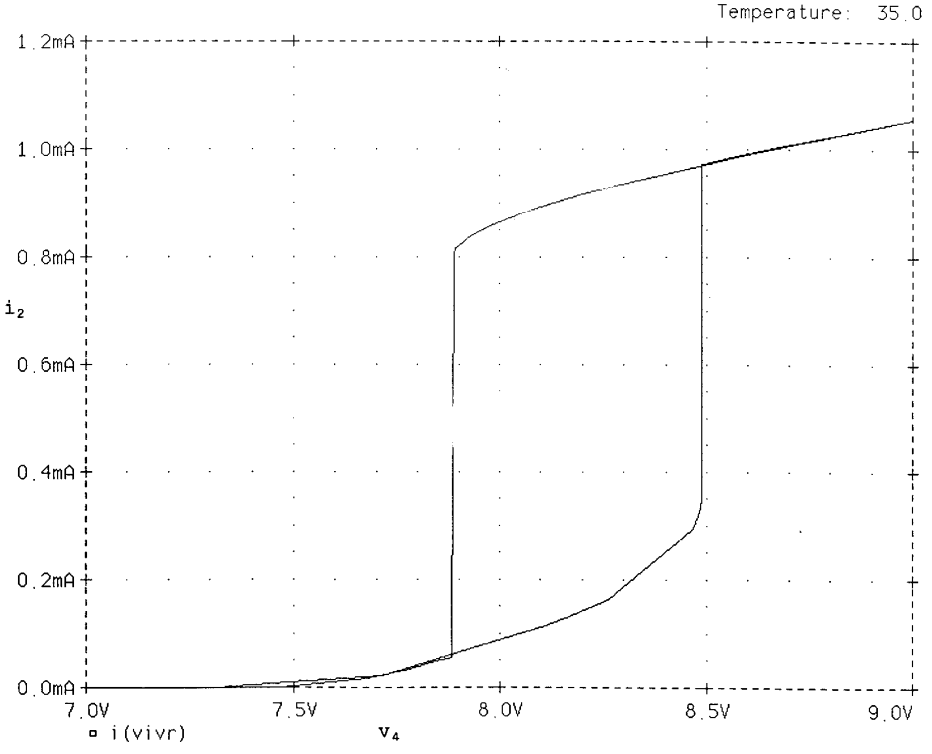

Figure 5. Resulting Hystersis of MOS NTC