Transaction Briefs

An Enhancement-Mode MOS Voltage-Controlled Linear Resistor with Large Dynamic Range

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Abstract—**It is shown that the depletion-mode linear resistor of Babanezhad and Temes can be implemented in enhancement-mode devices. This allows a large increase in the dynamic range of the resistors. By inserting a bias source the linearity can also be improved. A layout and experimental results on the resulting IC are included.**

I. Introduction

Recently, several authors have proposed voltage-controlled linear resistors in MOS technology [1]–[6]. In their results, several different techniques have been proposed for eliminating the effect of nonlinearities by manipulating the sum or difference of the current in two or more devices. By their simple structure and controllability, the depletion-mode unbalanced linear resistors proposed by Babanezhad and Temes [5] are attractive. In the modern popular CMOS technology, however, where usually depletion-mode transistors are not available, a linear resistor constructed from enhancement-mode transistors is inevitably in demand. Besides, the structures of [2], [3], [5] have, from the way of their manipulating of the current equations, a limited and fixed dynamic range, or linear range within the absolute value of the threshold voltage of the depletion-mode transistor.

Starting from the same simple structure of [5] but using enhancement-mode transistors, we propose, in this letter, a new linear MOS integrated circuit (IC) resistor based on the operation of two NMOS (or PMOS) transistors with resistance controlled via the gate voltage of one of the transistors. The proposed resistor is voltage controllable over a wide dynamic range and is suitable for implementing with small chip size as needed for neural type cells [7]. Measurements on the fabricated CMOS chip verify SPICE simulations.

II. Two MOS Transistors

Consider two enhancement-mode NMOS transistors connected, as shown in Fig. 1, with independent voltage source E_1. The voltage source E_1 is introduced to accommodate an appropriate dynamic region. Note that this bias source necessitates the substrate of $M1$ being connected to its source rather than to terminal 2 to maintain the reverse bias in its source junction.

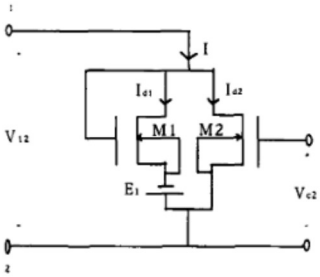

Fig. 1. Enhancement-mode NMOS linear resistor.

Assume the applied voltage across the common drain to node 2, V_{12}, satisfies the condition, $V_{12} \geq 0$. In this case $M1$ is operating in its saturation region due to its gate-to-drain connection, and the drain current will be approximately represented by [8]

$$I_{d1} = \begin{cases} (K_1/2)(V_{12} + E_1 - V_{t1})^2, & V_{t1} \leq V_{12} + E_1 \quad \text{(1-a)} \\ 0, & V_{t1} > V_{12} + E_1 \quad \text{(1-b)} \end{cases}$$

where V_{t1} is the threshold voltage of $M1$, and $K_1 = \mu C_{ox} W_1 / L_1$ is the transistor gain factor, which depends on the carrier mobility μ, unit area gate capacitance C_{ox}, transistor width W_1, and length L_1 [8]. For transistor $M2$, assume that it is operating in its ohmic region by assuming a suitably large voltage V_{c2} (larger than V_{t2}) is applied on its gate terminal; that is, let

$$V_{12} < V_{c2} - V_{t2} \tag{2}$$

where V_{t2} is the threshold voltage of $M2$. Thus for $M2$, the drain current is approximately represented by [8]

$$I_{d2} = K_2\left[(V_{c2} - V_{t2})V_{12} - V_{12}^2/2\right], \qquad 0 \leq V_{12} \leq V_{c2} - V_{t2} \tag{3}$$

where V_{t2} is the threshold voltage of $M2$, and $K_2 = \mu C_{ox} W_2 / L_2$ is the transistor gain factor for transistor $M2$.

Note that (1-a) and (3) are quadratic in V_{12}. Their I–V nonlinear characteristics are shown in Fig. 2, where V_{DD} is the largest voltage to be applied. As a result, if the degrees of convexity and concavity of the two drain current curves shown in the figure are adjusted to be the same, by simply using the same shape factor, W/L, for both transistors, that is $K_1 = K_2 = K$, then the square terms in (1-a) and (3) will cancel in the range of $V_{t1} - E_1 \leq V_{12} \leq V_{c2} - V_{t2}$ and the total current $I = I_{d1} + I_{d2}$ will be

$$I = \begin{cases} D\left[(V_{c2} - V_{t1})V_{12} - V_{12}^2/2\right], & 0 \leq V_{12} \leq V_{t1} - E_1 \quad \text{(4-a)} \\ K\left[(V_{c2} - V_{t1} - V_{t2} + E_1)V_{12} + (V_{t1} - E_1)^2/2\right], & V_{t1} - E_1 \leq V_{12} \leq V_{c2} - V_{t2}. \quad \text{(4-b)} \end{cases}$$

Here, $K = K_1 = K_2$ can be taken for granted assuming matching MOS devices with no process parameter variations between two closely placed transistors. This total current, I, is also shown together in Fig. 2, where the solid curve in region A corresponds to the current equation (4-a) and the straight line of region B corresponds to (4-b). Here, unlike the other proposed linear resistors [2]–[6], note that the dynamic range of this structure can be controlled by choosing suitable value of V_{c2}

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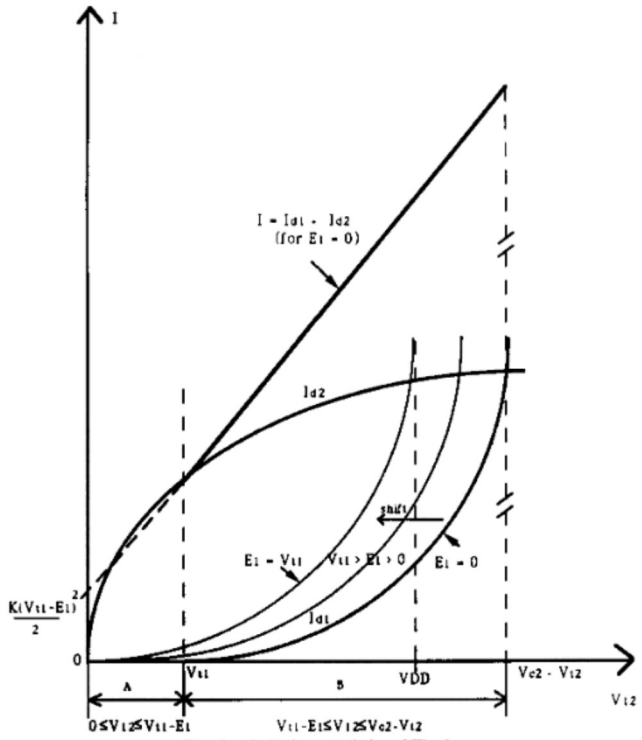

Fig. 2. $I-V$ characteristics of Fig. 1.

and E_1 depending on the range of the applied voltage V_{12} across the resistance in the circuit. In the region B, since the current I is linear with respect to V_{12}, the equivalent resistance can now be written as

$$R_{eq} = 1/[K(V_{c2} - V_{t1} - V_{t2} + E_1)] \tag{4-c}$$

which is controlled by the gate voltage V_{c2}, and voltage source E_1. The offset term $K(V_{t1} - E_1)^2/2$ in (4-b) depends on the transistor threshold voltage, voltage source E_1, and on K.

Techniques to minimize this offset term in (4-b) include using small shape factors of the transistors, controlling the threshold voltage V_{t1} through the use of substrate bias, or use of the voltage source E_1 shown in Fig. 1. The threshold voltage itself is a complex function of body effect, fixed surface charge and various process parameters and it is almost impossible to control by designers. However, it is possible to minimize the offset term through controlling either E_1 or transistor shape factors (as long as the resistor does not consume large silicon area). Since the shape factor is fixed at the design stage and can not be changed afterward, varying E_1 is preferable. Besides, if a shape factor is approximately given to match a certain value of resistance, fine tuning becomes possible by controlling E_1. As an example for the extreme case, if the voltage source $E_1 = V_{t1}$ is chosen, it will cause a shift of the nonlinear characteristic curve, I_{d1} (Fig. 2) to pass through the origin, and the resulting offset term will be zero. This has the added advantage that region A disappears and linearity is achieved throughout the applied voltage range, $0 \leq V_{12} \leq V_{DD}$.

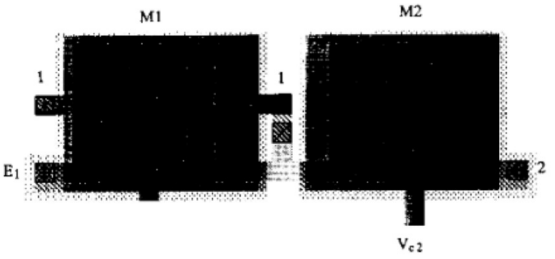

Fig. 3. Layout for Fig. 1.

Fig. 3 shows the actual layout for Fig. 1. Here, $M1$ and $M2$ each have separate substrates, p-wells in this case. Note that for such a layout, $V_{t1} = V_{t2} = V_t$ is automatically determined and no body effect is present. Equation (4-c) can consequently be simplified to

$$R_{eq} = 1/[K(V_{c2} - 2V_t + E_1)]. \tag{5}$$

In fact, an upper bound on the V_{c2} value is given by the gate oxide rupture voltage which expands approximately to 40 V at 400 Å oxide thickness [9]. This will make the upper limit of the region B in Fig. 2 close to 39 V ($= V_{c2} - V_{t2}$). An interesting point is that V_{c2} is controlling both R_{eq} and the upper bound of the dynamic range simultaneously. If, for example, high voltage of V_{c2} is chosen for large dynamic range it will decrease R_{eq} of (5) in return. Considering, in most cases, the dynamic range of the resistor has its maximum value same as the largest applied voltage (VDD), the corresponding suitable value of V_{c2} is firstly

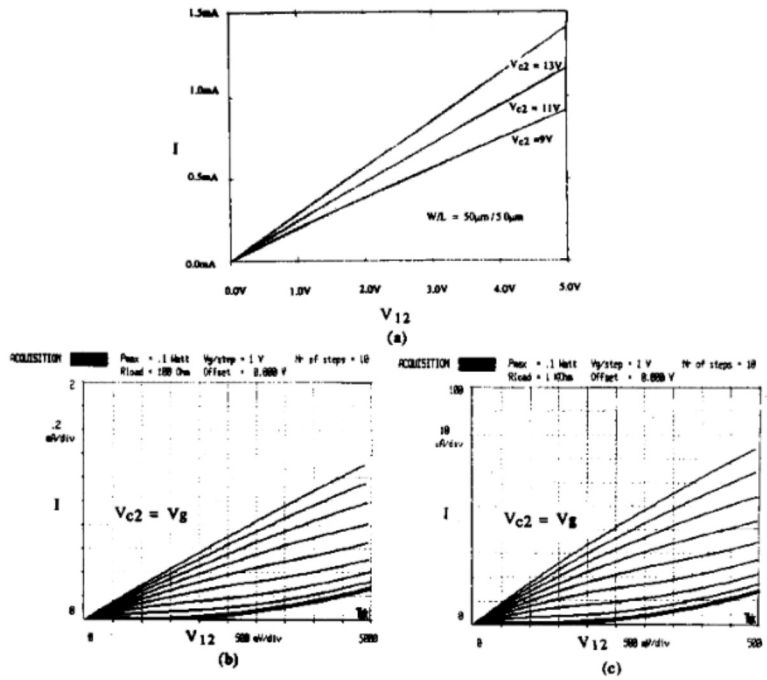

Fig. 4. (a) Simulation results of $I-V$ characteristics of Fig. 1. ($E_1 = 0$ V). (b) Measurements for $W/L = 50\ \mu m/50\ \mu m$. (c) Measurements for $W/L = 8\ \mu m/162\ \mu m$.

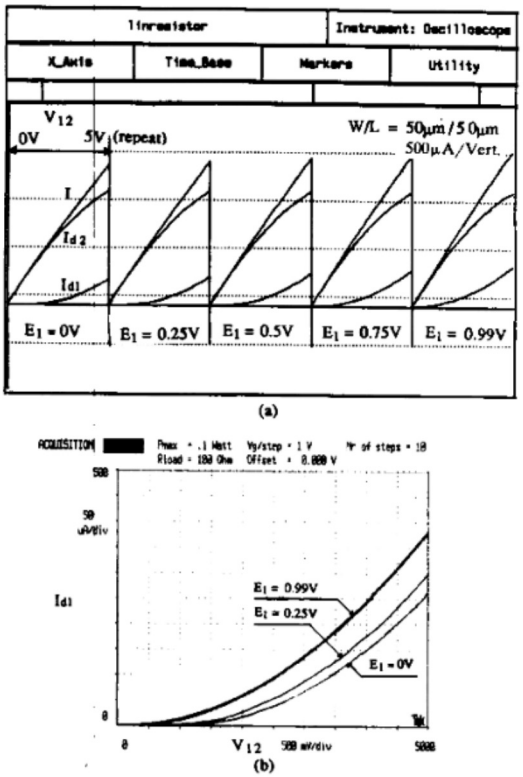

Fig. 5. (a) Simulation results of I_{d1} with varying E_1. (b) Measurements of I_{d1} with varying E_1.

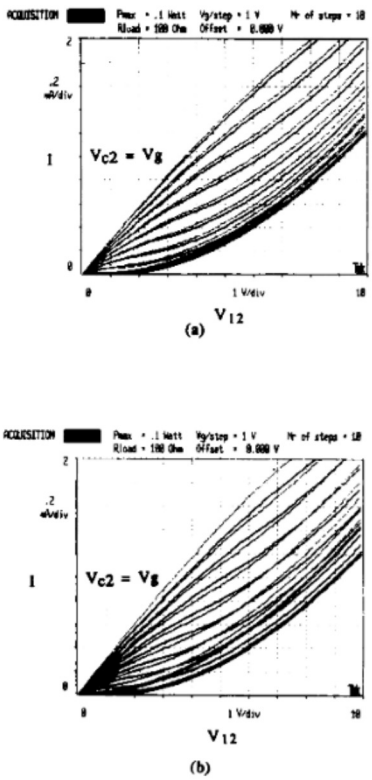

Fig. 6. Measurements of resistor curves with varying E_1 (dark lines are for $E_1 = 0$ V. (a) $E_1 = 0.25$ V. (b) $E_1 = 0.99$ V $= V_t$.

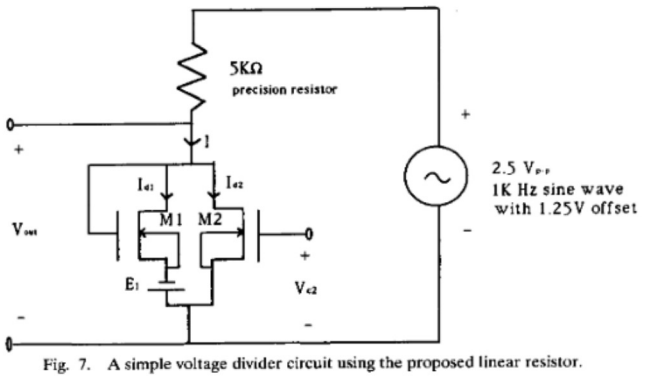

Fig. 7. A simple voltage divider circuit using the proposed linear resistor.

to be decided and R_{eq} can then be adjusted via transistor aspect ratio, accordingly. If the dynamic range is not a point of concern, then R_{eq} can be set as desired.

III. Simulation and Experimental Results

The circuit of the layout for Fig. 3 with external voltage source E_1 was designed and integrated via MOSIS silicon gate p-well CMOS technology with 2 μm minimum geometry for different sizes of transistors. The shape factors chosen were $W/L = 50/50$ μm $= 1$ and $W/L = 8/162$ μm $= 0.049$ along with the MOSIS process parameters [10] to implement linear resistors of values 3.3 and 67 kΩ, respectively, when $V_{c2} = 9$ V. For the layout of a long channel device, such as for $W/L = 8/162$ μm, two identical snake-shape transistors were used to guarantee device matching. A minimum channel width of 8 μm is chosen to avoid narrow channel effects and to minimize the effect of channel width deviation due to various process factors. The resistor will, therefore, have its resistance value mainly proportional to the inverse of the transistor shape factor when the gate control voltage is fixed. Fig. 4(a) shows the SPICE I–V characteristics with different gate control voltages for the circuit of Fig. 1 when $E_1 = 0$ V, and measurements shown in Fig. 4(b),(c) on the acutal chips using a digital curve tracer verify this simulation result. Fig. 5(a) shows the simulation results giving a shift of I_{d1} of transisitor $M1$ ($W/L = 50/50$ μm) due to varying E_1; Fig. 5(b) shows the actual measurements. The corresponding shifts of the resistance curves are shown in Fig. 6.

In addition, the main constraints at high frequencies will be imposed mainly by gate capacitances. In order to analyze the frequency characteristics, a voltage divider circuit was constructed as shown in Fig. 7. Measurements at the output, V_{out}, showed that, for a 1 V_{p-p}, 1 kHz signal across the proposed linear resistor, biased at 1.25 V, the total harmonic distortion (THD) was equal to 0.62% (−44 dB) when $E_1 = 0$ V and 0.46% (−47 dB) when $E_1 = 0.997$ V $= V_{t1}$ [see Fig. 8]. In Fig. 8(a) the first largest peak corresponds to the input 1 kHz spectral component and the next right peak corresponds to the 2 kHz component, and so on. In these experiments, V_{c2} is chosen as 9 V in order to force transistor $M2$ to be always operating in the ohmic region.

IV. Conclusions

In this paper, we have presented an enhancement-mode linear resistor with wide dynamic range. Instead of the depletion-mode transistors of [5], enhancement-mode transistors are employed to build this resistor. It is, therefore, expected to be

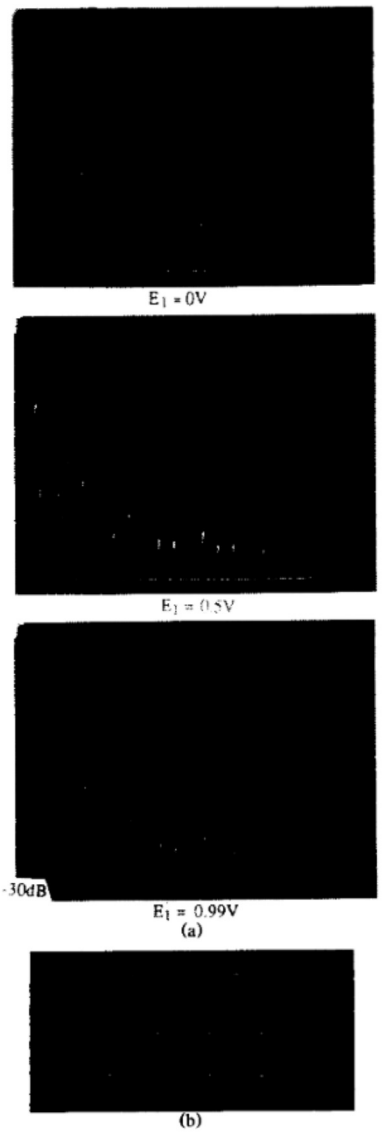

Fig. 8. (a) Spectral content at the output of a 1 V_{p-p} signal, $V_{c2} = 9$ V. (b) Upper trace: input signal; lower trace: output signal.

implemented well with modern popular CMOS technology. Also, while the other depletion-mode resistors of Babanezhad and Temes [5] or Han and Park [3] have fixed dynamic range within the absolute value of the depletion-mode transistor, this structure has controllable dynamic range which can be expanded over 30 V. Dynamic range is controlled by the value of V_{c2} which in turn is limited by the gate oxide thickness. The resistance value is adjusted through the transistor aspect ratio and V_{c2}. By using the external voltage source, E_1, the linearity of the resistor is improved.

The proposed linear resistor is suitable for applications where small chip area with a controllable dynamic range is required. One good use is for a neural-type cell [7]. Due to its simple structure and controllability, this resistor can be used in other CMOS applications as well. The characteristics of the NMOS voltage-controlled resistance discussed above apply equally well to PMOS constructions. This technique could be used to implement a wide dynamic range voltage-controlled linear resistor [4], [11].

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A Parametric Representation for k-Variable Schur Polynomials

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Abstract—**In this paper a parametric representation for k-variable polynomials with prescribed partial degrees is given, where the coefficients are functions of real parameter vectors. Simple conditions for these parameters are established, which are *sufficient* to guarantee that the corresponding polynomials are *widest sense Schur* (WSS). Furthermore, in the two-variable case simple *necessary* and *sufficient* conditions are introduced so that the corresponding polynomials are *scattering Schur* (SS). The synthesis of two-dimensional (2-D) lossless one-ports and a parametric representation of constant unitary matrices form the basis of our considerations.**

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I. Introduction

Widest sense Schur (WSS) and scattering Schur (SS) polynomials [1] have been introduced as the z-domain counterparts to widest sense Hurwitz and scattering Hurwitz polynomials [2] in the p-domain, respectively. They turned out to be the classes of polynomials being most relevant in the context of structurally passive digital filters, in especially multidimensional wave digital filters [3], [4]. A parametric representation for k-variable polynomials of the type

$$g(z_1,\cdots,z_k)=\sum_{i_1=0}^{n_1}\cdots\sum_{i_k=0}^{n_k}\alpha_{i_1,\cdots,i_k}z_1^{i_1}\cdots z_k^{i_k} \qquad (1)$$

where n_i is the partial degree in the complex variable z_i, $i=1,\cdots,k$, and the complex coefficients $\alpha_{i_1,\cdots,i_k}$ are the parameters, is the simplest we can imagine but less helpful in describing k-variable Schur polynomials, since the corresponding admissible parameter space is composed of very complex shaped domains in the whole coefficient space, i.e., the boundaries for a certain parameter $\alpha_{i_1,\cdots,i_k}$ depend on the other parameters and $n_1,\cdots,n_k$. Nevertheless, in the case of one-variable Hurwitz polynomials, Kharitonov investigated subsets of such domains having constant boundaries for each parameter [5]. However, not the whole class of one-variable Hurwitz polynomials can be comprised by using such representations and no explicit formulas are given for determining the appropriate boundaries. Recently, extensions of Kharitonov-type representations to k-variable scattering Hurwitz polynomials have been established [6], [7], which exhibit the same drawbacks as in the one-variable case. Hence, parametric representations of the type (1) are not suitable for describing Hurwitz and Schur polynomials, respectively. In the one-variable case, the representation of a polynomial in terms of its zeros or a continued fraction expansion of an associate rational function have turned out to be appropriate tools for describing Hurwitz polynomials in terms of parameters having well-defined constant boundaries. The latter parametric description is based on the fact that every rational para-odd positive function can be realized as the impedance of a canonic lossless ladder one-port. In the present paper a network synthesis based approach is used too, in order to find a parametric representation for k-variable Schur polynomials. Such a description is of interest in the context of computer-aided network design, where the parameters have to be optimized in such a way that a certain error function is minimized, taking into consideration the parameter boundaries. Hence, it is desirable to have constant admissible parameter intervals.

II. Definitions and Notations

We consider rational functions or matrices which are expressions in $k \geqslant 1$ complex variables z_i, $i=1,\cdots,k$. For convenience of notation we summarize them in a vector $z=(z_1,\cdots,z_k)$. A notation such as $|z|<1$ designating $|z_i|<1$ for all $i=1,\cdots,k$. If a polynomial $g(z)$ is written as a polynomial in the variable z_i as

$$g=\sum_{\nu=0}^{n_i}g_\nu z_i^\nu$$