The Semistate Description of a Four Transistor CMOS Schmitt Trigger*

A. Ahmad, R. Newcomb and F. Abedin

Microsystems Laboratory
Electrical Engineering Department
University of Maryland
College Park, MD 20742 USA
(301) 454-6869

Abstract

In this paper we give the means for setting up the relevant semistate equations of a four transistor CMOS Schmitt trigger under development for VLSI realization. By parametrically solving the nondynamic portions of the semistate equations one sees the physical basis through which the hysteresis results. The technique is illustrated with SPICE runs.

1. Introduction

The Schmitt trigger, first introduced by Otto Schmitt in the 1930's [1], occurs in many situations and has been basic to the operation of a number of systems, for example in reducing the effects of noise on triggering responses [2] and in describing the immune system for biological simulations [3]. It is an important enough electronic circuit element that it is now treated in most texts on electronics, even at the most elementary undergraduate level [4,p.567]. However, because the basic property of the Schmitt trigger is its hysteresis, mathematical descriptions need to be formulated with care. Several mathematically based descriptions are available [5][6][7][8][9] but in using these one loses physical insight as to just why the jump for increasing input is different than for decreasing input. The situation can be improved by reverting to semistate equations [10,p.246] which allow one to give mathematical characterizations of certain types of hysteresis, including the binary hysteresis of the Schmitt trigger, via single-valued descriptions; by choosing appropriate semistate variables physical meaning can be ascribed to account for the jumps at different inputs following the philosophy of [2,p. 340].

Because of its interest for neural networks, we have developed a Schmitt trigger using a small number of CMOS transistors so that it may be realized via VLSI techniques. Here we describe this circuit, which is a four transistor device, with the design philosophy coming from semistate theory. Other MOS Schmitt triggers exist [11]-[19] some of which are also four transistor MOS circuits [12][13][16][19] though the characteristics are not as sharp as those obtained with the circuit presented here.

As background we review semistate theory in Section 2. In Section 3 we describe the circuit using semistate theory, where only single-valued functions are involved, and discuss how the circuit yields hysteresis, a multi-valued function. Section 3 also contains SPICE results and Section 4 has some discussion.

2. Brief Overview of Semistate Theory

Semistate equations are generalizations of state variable equations which in canonical form are expressed as

$$E\cdot x' = A(x,t) + B\cdot u \qquad (1a)$$

$$y = C\cdot x \qquad (1b)$$

where x is the semistate vector, B, C, and E are constant matrices, $A(\cdot,\cdot)$ is a nonlinear vector-valued function; u and y are the input and output, respectively and the prime ' denotes time, t, differentiation. A key feature of these equations is the possible singularity of E, which implies that nondynamic characteristics are included along with the dynamics of a system. In using (1) to describe systems the nondynamic, and the dynamic, characteristics will normally be single-valued functions in which $A(\cdot,t)$ is a single-valued function. Equations (1) are known to be useful for describing hysteresis [10] even though hysteresis is described by multiple valued functionals. The presence of hysteresis is reflected in the semistate equations by double valued solutions of single-valued characteristics. In particular hysteresis results from the fact that there are multiple solutions of (1a) for the semistate x.

3. Circuit Description and Results

Figure 1a shows our four transistor CMOS Schmitt trigger, and a typical DC hysteresis curve which results from it is seen in Fig. 1b. The circuit of Fig. 1a is a modification of the standard one presented in [14, Fig. 3] and has M_1-M_2 forming a differential pair with M_3 acting to steer the current between M_1 & M_2. M_4 acts as a load for the current of M_1 across which the output voltage is taken (at node 3). Positive feedback to yield the hysteresis is achieved by attaching the gate of M_2, the second input of the differential pair, back to the drain of M_1, the first transistor in the differential pair to which the input voltage v_1=u is applied.

Figure 2 shows an equivalent circuit involving the key elements of interest for writing a semistate description of the circuit. Here we will choose the semistate to be the 5-vector, superscript T denoting the transpose,

$$x = [v_1,\ v_3,\ i_{c1},\ i_{cu}]^T \qquad (2)$$

Using Kirchhoff's laws the resultant canonical semistate equations are readily found to be

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$$\begin{bmatrix} . & C_u & . & . \\ . & C_1 & . & . \\ . & . & . & . \\ . & . & . & . \end{bmatrix} x' = \begin{bmatrix} . & . & . & 1 \\ . & . & 1 & . \\ . & . & 1 & 1 \\ -1 & . & . & . \end{bmatrix} x +$$

$$\begin{bmatrix} . \\ . \\ -i_u(x_2)+i_1(x_2,x_1) \\ . \end{bmatrix} + \begin{bmatrix} . \\ . \\ . \\ 1 \end{bmatrix} u \qquad (3a)$$

$$y = [.\ 1\ .\ .]x \qquad (3b)$$

Here the upper current i_u is that through the diode connected load transistor M_4 expressed as a function of the voltage $v_3=x_2$; that is $i_u(x_2)=-i_d(v_3-V_{DD})$ where i_d is the drain current taken as a function of the drain to source voltage. Similarly, the lower current i_1 is that in the drain of M_1 expressed as a function of v_3 with $x_1=u=v_1$ as a parameter. Analytic expressions for these two currents, i_u and i_1, are possible but rather complex due to the number of regions traversed by the transistors. This is especially true for i_1 since it incorporates the effects of M_1, M_2, and M_3. However, i_1 and i_u are relatively easily determined, once transistor parameters are known, via computer aided design packages, such as SPICE. Thus, using the curve tracing configuration of Fig. 3a run via ORSPICE (where the transistors receive a prefix X) with MOSIS CMOS parameters, a typical set of curves is graphed in Fig. 3b with an expanded view of these curves at large output voltages shown in Fig.3c. In this curve tracing i_u=I(VI4) is the current in M_4 and i_1=I(VI1) is the drain current of M_1, both being monitored in the zero voltage voltage sources similarly labelled; values including V_{DD}=5 are chosen to go with the hysteresis curve of Fig. 1b and u=v_1=V(1) runs between 1.2v (the lower I(VI1) curve) and 2.4v (the upper I(VI1) curve) in 0.1 v steps.

Proceeding toward the hysteresis, we see from the third row of the semistate equations, (3a), that $i_u=i_1$ at DC, i.e. when $x'=[0,0,0,0]^T$. That is, at DC the circuit has a solution when, by KCL, the upper current i_u equals the lower current i_1. The curves for these two currents are single-valued when plotted versus v_3, for a fixed input. However, they intersect at multiple points for certain values of the input, as again typicially seen in Fig. 3b, thus giving a multivalued input-output curve. This multivalued input-output curve is the hysteresis with the tracing remaining on a given branch (until switching is forced) due to the capacitors giving the dynamics in (3a). To see why switching occurs differently for increasing versus decreasing inputs, we can again consider Fig. 3 where we see that for small inputs there is no intersect point on the left (Fig. 3b) and only one on the right (lower curves of Fig. 3c). As the input is increased, the intersect point on the right remains but also a new one on the left comes about. For further increase in the input the one on the right actually disappears (after first branching into two), as seen in the expanded version of Fig. 3b shown in Fig. 3c; on disappearance, at about 2.24v, the only intersection is on the left and the system jumps to that intersection and remains there for further increases in the input. As the input is decreased the intersection on the left remains and is held as the solution well after the intersection on the right returns; a jump to the intersection on the right occurs when there is no more intersection on the left. The jump to the left intersection is seen to occur at a different value of the input than the jump to the right, giving rise to the hysteresis. As can be seen from Fig. 3c, there are some values of the input for which three intersections occur (but the intermediate intersection is not of practical interest for hysteresis, as it is undoubtedly unstable). From Fig. 3c it is also seen that the right most intersect point occurs for decreasing v_3, as the input is increased, over part of the input range, this giving the dip in the hysteresis curve just before the full jump in the output from the high to the low level.

4. Discussion

Using semistate theory we have presented the idea behind the operation of our four transistor CMOS Schmitt trigger. This same idea can be developed for other transistor Schmitt triggers that occur in the literature, as referenced above. Possibly such developments could lead to improved insight of their operation, especially since some of the circuits behave differently when so viewed than che descriptions given in the literature for their operation. The advantage of the actual circuit presented here is its suitability for VLSI implementation, since only four readily integrated CMOS transistors are used. In preparing this study we also discovered another, actually very similar, four transistor Schmitt trigger with a layout given in a recently appearing VLSI text [19,plate 8]. In analyzing the circuit of [19], which earlier appears in [12, Fig. 1], we can set up i_u and i_1 in a similar manner but one finds that both vary with the input if v_3 is used as the common independent variable. Consequently, it is advantageous to switch to a different independent variable so that only one of the curves will vary with the input, with such a variable being v_3-u.

It should be noted that we could have given a larger set of semistate equations by including the current in M_2 as well as by including the full descriptions of all of the tranistors. But for our purposes of describing the hysteresis all of these details are secondary and, hence, omitted in this short treatment.

From Fig. 3b it can be seen that if a larger hysteresis width is desired, then one wants to decrease the current through M_4 which is readily done by decreasing its W/L ratio. However, an expression for the hysteresis width, as well as its center, are best developed via analytic expressions. Although an analytic expression for the upper current, i_u, is readily given, one for the lower current, i_1, is more complicated and still remains to be perfected.

References

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[15] D. A. Hodges and H. G. Jackson, "Analysis and Design of Digital Integrated Circuits," Second Edition, McGraw-Hill Book Co., NY, 1988. (see Fig. 8.23, p. 321 for a 12 transistor CMOS circuit and Fig. 8.21, p. 318 for an emitter coupled BJT circuit)

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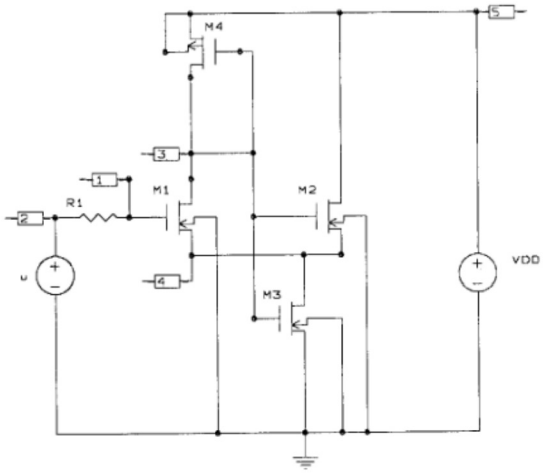

Figure 1a The Circuit

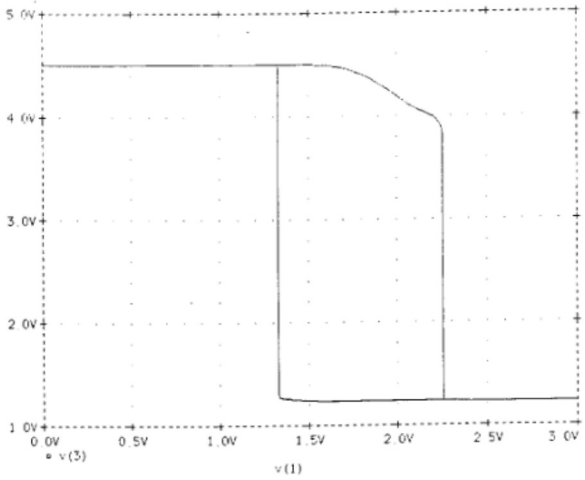

Figure 1b Resulting Hysteresis

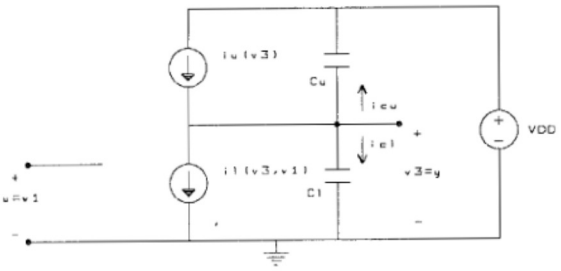

Figure 2 The Relevant Equivalent Circuit

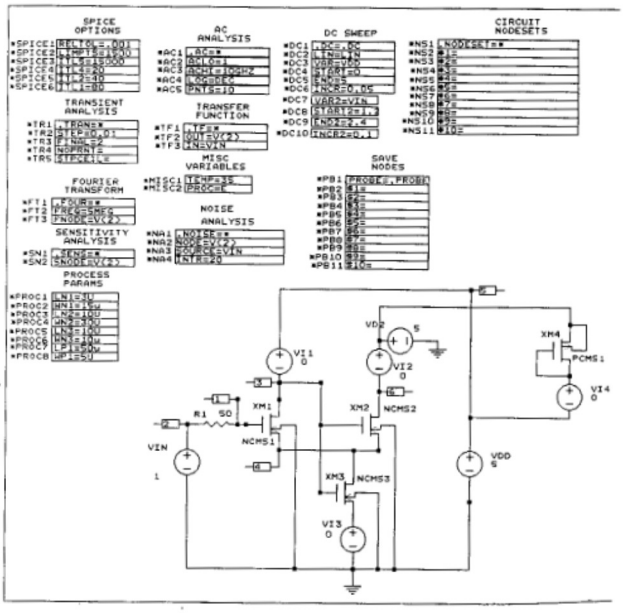

Figure 3a
The Curve Tracing Circuit
MOSIS CMOS parameters
(ORSPICE Setup)

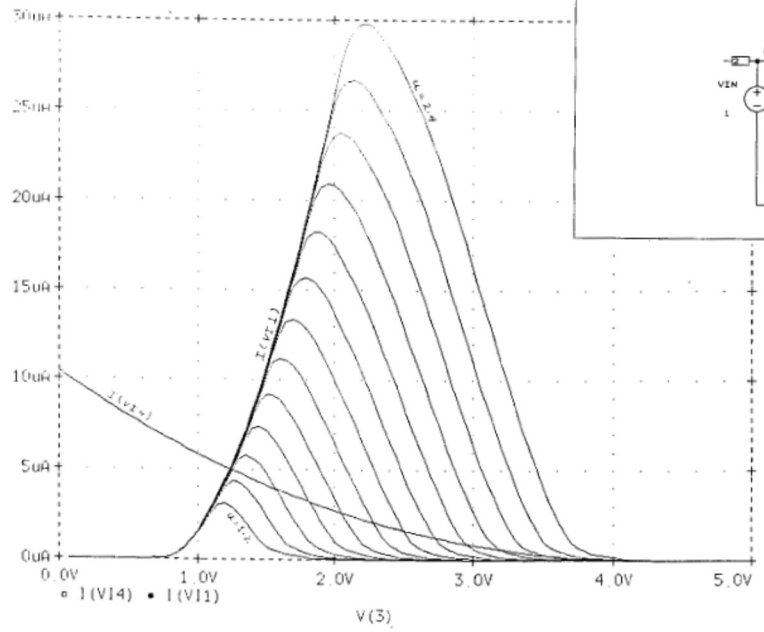

Figure 3b i_u and I_1 from Curve Tracing

Figure 3c Two Expansions
of i_u and i_1
Near Upper Hysteresis Level