CMOS Realization of a Class of Hartline Neural Pools *

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Abstract

In this paper we present CMOS realizations suitable for IC constructions of type three and four pools utilized by Hartline neurons. These pools are useful for neural networks with reprogrammable neurons which mimic physiological neural systems quite realistically as studied by Hartline. Important to the operation of these neurons are the "pools" which simulate biochemically derived properties.

1. Introduction

Hartline [1] has presented a network model SYNETSIM which is composed of two arrays of compartments, electrical and chemical, to simulate a set of neuron properties. The chemical components are constructed by a set of diffusionally connected compartments called "pools". There are four basic types of these pools with the first two of them being conditioned by transmitter binding, a third one having a filling rate proportional to ionic current with first order decay and the fourth one having a constant filling rate with first order decay. The latter two pools can be used to simulate the first-order biochemical reactions, including second messenger systems, activated through transmitter or hormone binding and through voltage-gated processes, such as Ca^{++} entry. The chemical material in the pools can diffuse into the neighboring pools by first-order diffusional constants. These chemical compounds can also modulate the properties of the electrical compartments and the filling constants of pools by certain modulation functions. Here we consider CMOS simulations of the last two types, that is the neuron pools in which the filling has first order decay. This is done in a way that the parameters are easily modulated by other pools.

2. Chemical pools and inter-pool diffusion

Each pool in the SYNETSIM network has a specific volume (v) which contains a certain amount of material (P) in it. The pool of type three has a filling proportional to the ionic current with first order decay with the describing equation for the type three pool being

$$\frac{dP}{dt} = CI - C'P + I_{DT} \qquad (1)$$

Here P is the total amount of material in the pool, I is the ionic current flowing in a specified electrical compartment and I_{DT} is the inter-pool diffusion term which will be explained later. C and C' are constants, C' being the decay rate. This pool can be used to simulate entry of ions through channels, (e.g., Ca).

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For the type four pool, the describing equation is

$$\frac{dP}{dt} = F - C''P + I_{DT} \qquad (2)$$

where F is the filling rate and C'' is the constant decay rate; all of the rates can be modulated by other pools.

Chemical materials can diffuse between pools via the I_{DT} with this diffusion described by first order diffusional rate constants and associated terms. For the k^{th} pool inter-diffusing with the j^{th} pool, the inter-pool diffusion term is

$$I_{DT} = \sum_{j \neq k} \left(K_{k,j} \frac{P_j}{v_j} \right) - \left(\sum_{j \neq k} K_{j,k} \right) \frac{P_k}{v_k} \qquad (3)$$

in which v_j is the volume of the j^{th} pool, P_j/v_j is the j^{th} pool concentration and the $K_{i,j}$ are the inter-pool volumetric decay rate constants. Here, according to [1], the K matrix is symmetric, that is, $K_{i,j} = K_{j,i}$.

3. Realization of type three and type four pools

For the circuit realizations, we consider the P's to be analogous to charge with a pool itself being considered as a capacitor since it stores the pool material. The volume v of the pool is analogous to the capacitance, in which case the concentration P/v will be analogous to the voltage across the capactor. Then, the F's are constant, bias, current sources and the C, C', and C'' can come from dependent current sources which can be easily modulated by other pools.

According to equations (1) and (2), we can view an isolated pool as a capacitor with some current flowing in (CI for type three and F for type four) and some self-concentration dependent current flowing out ($C'P$ for type three and $C''P$ for type four). Adding to these currents are the I_{DT} terms which flow in or out depending upon I_{DT} positive or negative, respectively. The terms $C'P$ and $C''P$ can be formed by (one quadrant) multipliers.The basic structures of the type three and four pools are shown in Figure 1 where $C'P$ and $C''P$ are the output currents of the multipliers .

When the filling current F is modulated by other pools, the F is simply an output current of an analog multiplier whose input is connected to the modulating pool. The structure of pool of type three is the same as for pool type four except the filling current CI is the output of another analog multiplier which is biased by the current I in a specified electrical compartment. According to this structure, the analog multiplier is the most importment sub-circuit when implementing the Hartline pools.

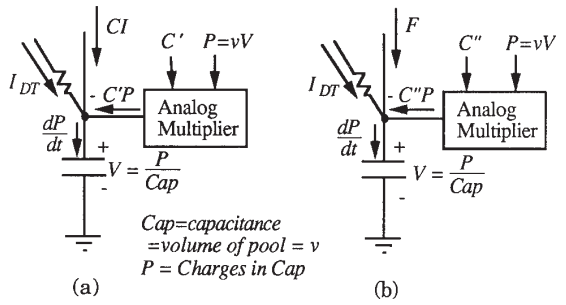

Figure 1: (a) Structure of type three pool
(b) Structure of type four pool

3.1. Analog multiplier

Analog multipliers play a very important role in the implementation of type three and type four pools. The basic source-coupled pair (Figure 2) can be used as a multiplier [2 p.705]. When both M1 and M2 are in the saturation mode, the difference between the drain currents of M1 and M2 will be

$$\Delta I_d = \mu_n \frac{C_{ox} W}{2L} (V_{in}) \sqrt{\left(\frac{2I_{ss}}{\mu_n (C_{ox} W/2L)}\right) - (V_{in})^2} \qquad (4)$$

When

$$V_{in} << \sqrt{\left(\frac{I_{ss}}{\mu_n (C_{ox} W/2L)}\right)} \qquad (5)$$

equation (4) can be simplied to

$$\Delta I_d = \sqrt{\mu_n \frac{C_{ox} W}{L}} (V_{in}) \sqrt{I_{ss}} = \beta (V_{in}) \sqrt{I_{ss}} \qquad (6)$$

However, there are two problems with the circuit of Figure 2:

(1): The loads due to M3 and M4 on the drains of the two NMOS transistors M1 and M2 are different.

(2): The output current of the current source M3 can vary considerably due to variations of the output voltage.

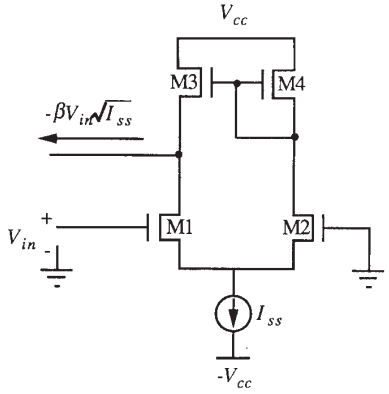

Figure 2: Source-coupled pair as multiplier

To remove the first problem, we can add an off-set voltage or change the W/L ratio but these are impractical solutions because the bias current I_{ss} may be desired to be modulated by other pools or it may be different for different pools. Once I_{ss} is changed, the loading problem occurs again. One method is to make the loads on the drains of M1 and M2 to be the same which will remove the first problem. This leads to the circuit shown in Figure 3.

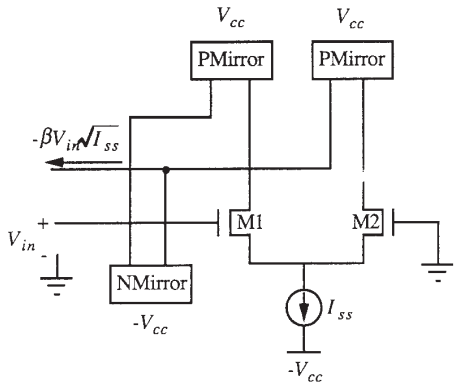

Figure 3: Improved multiplier

The second problem can be solved by cascoding the current sources to increase the output resistance. Because the constant β in the figure above is about the order of 10^{-3}, the output current is extremely sensitive to the output voltage. Therefore, we choose a triple cascode current source here so that the output current of a current source can be independent of the output voltage. The final circuit of the multiplier and its simulation are shown in Figure 4. In this and following simulations the MOSIS level 2 CMOS parameters were used. The W/L ratio for the MOS transistors in the source-coupled pair is 2 while the W/L ratio for the MOS transistors in the cascoded current sources is 10. The range of V_{in} in this multiplier can vary from 0 to 1 volt (the amount of material in a pool can not be negative) which is good for implementing a neural system.

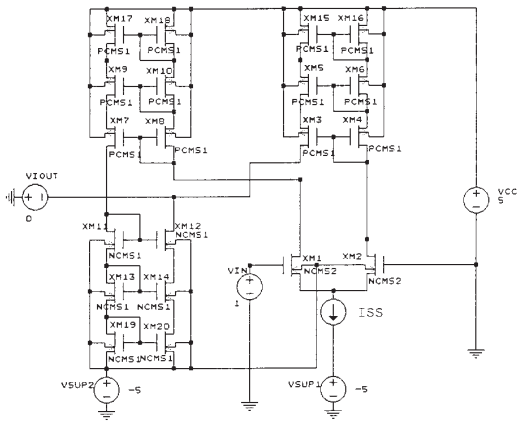

Figure 4(a): Circuit of multiplier

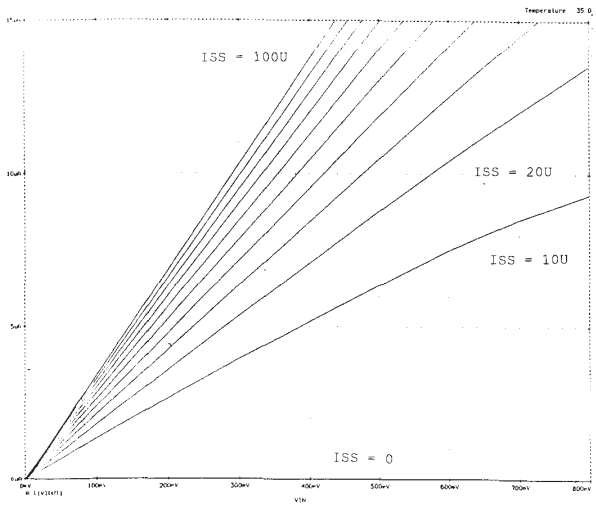

Figure 4(b): Simulation output of multiplier

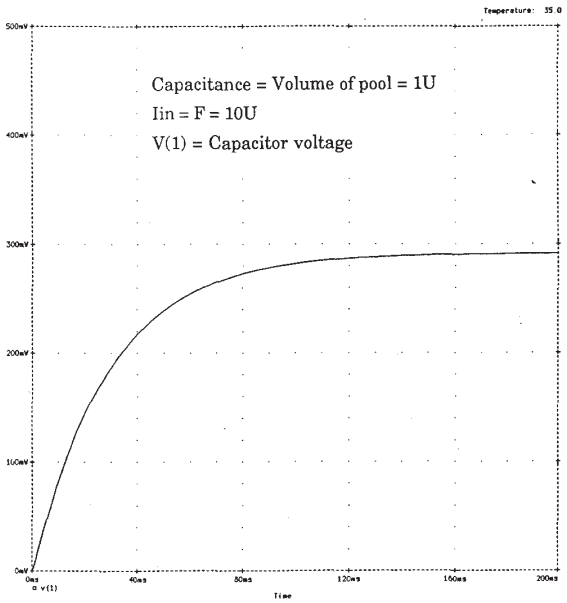

Figure 5 (b): Simulation of isolated type 4 pool with initial condition 0 volt

3.2. Type three and type four pool realizations

From equation (2) we can assume that a type four pool is actually a capacitor with current F flowing in and current $C'P$ flowing out, where the constants F and C' may be modulated by other pools. The type three pool is the same as the type four pool except the filling current CI is modulated by the ionic current I in a specified electrical compartment. Since the type three and four pools are almost identical, we show the results for type four alone in Figure 5. Here we only simulate a pool whose filling current is not affected by other cells. When this current is modulated by some other cell, we can replace the current source by some other circuit (e.g. analog multiplier for linear modulation).

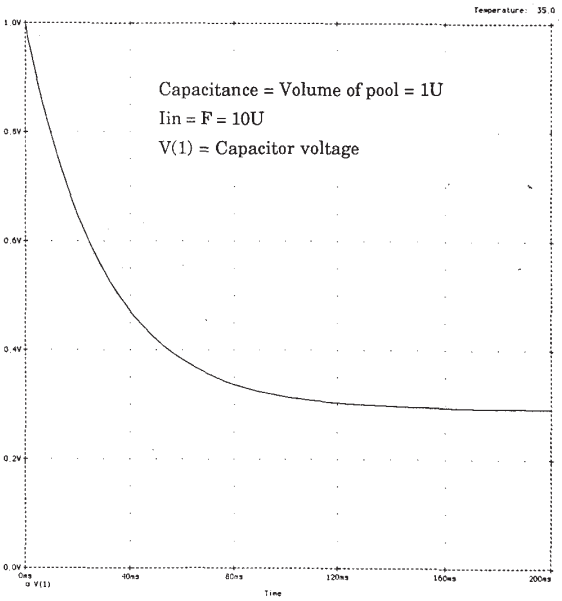

Figure 5(c): Simulation of isolated type 4 pool with initial condition 1 volt

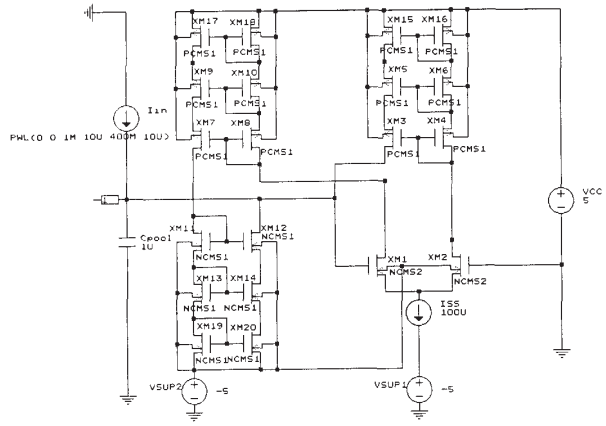

Figure 5 (a): Circuit of type 4 pool

3.3. Inter-pool diffusion

Chemical material in pools can diffuse between pools. This phenominum is simulated via the I_{DT} terms which can be realized by charges traveling between capacitors in a resistive path whose conductivity is interpreted as the diffusional rate constant. Because the diffusional rate constants between any two pools must be equal, that is, $K_{j,k} = K_{k,j}$, the structure of two pools with inter-pool diffusion between them is shown in Figure 6.

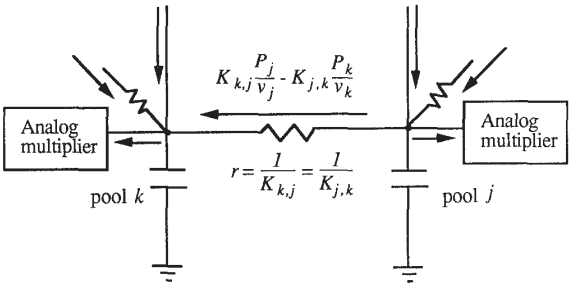

Figure 6: Inter-pool diffusion between two pools

4. Discussion

This paper presents the basic CMOS circuits for simulation of type three and four pools. In these basic circuits we did not incorporate modulation of the parameters by other pools, since the modulation interaction functions have not yet been implemented. As mentioned in Hartline's paper [1] (Table IV. C), there are at least seven types of interactions that can exist. Each interaction (pool-dependent modulation) function can be used to simulate a certain functional dependence in a neural system. The means to implement these interaction functions is still under investigation.

5. References

1. Daniel K. Hartline, "Simulation of Restricted Neural Networks with Reprogrammable Neurons", IEEE Transactions on Circuits and Systems, Vol. 36, No. 5, May 1989, pp. 653-660.

2. P. K. Gray and R. G. Meyer, "Analysis and Design of Analog Integrated Circuit", 2nd Edition, John Wiley & Sons, New York, 1984.