IC LAYOUT FOR AN MOS NEURAL TYPE CELL

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ABSTRACT

CMOS implementation of Neural Type Cell (NTC) is described. Two MOS transistors are used to realize the linear resistors in the Neural Type Cell. The integrated Neural Type Cell simulation results verify the expected behavior of the cell.

Several cells with different sizes have been designed and sent for fabrication.

1. INTRODUCTION

Current research on neural models builds on a long history of efforts to capture the principles of biological computational mathematical models. An approach to model biological systems is through the use of neural type microsystems. These are microelectronic structures which possess signal processing capabilities of physiological neural systems [1]. Models in this area are motivated by the desire to construct systems as close as possible to the physiological ones of the central nervous systems.

The field of neural-type microsystem appears to be one of promise, where VLSI technology will be an important development. The basic circuits are neural-type cells (NTC), neural-type junctions (NTJ), and neural-type lines (NTL). The NTC is the electronic analog of the neuron, or nerve cell, and can carry out the function of coding of sensed signals. The NTJ serves to combine signals and, as such, acts like the biological synapse. The NTL serves to transmit signals from place to place, and thus serves like nerve axons.

In this paper we will describe a CMOS implementation of a neural-type cell. Two MOS transistors are used as voltage controlled resistors to implement the NTC.

2. BASIC NEURAL TYPE CELL

The simplest cell of the type of interest is shown in Fig. 1a, which consists of two MOS transistors and RC components [2]. When a third feedback MOSFET is added, as shown in Fig. 1b, interesting properties result including output pulse repetition rate controlled by input amplitude. Fig. 2 shows PSPICE simulations. The operation of the circuit of Fig. 1b critically depends upon hysteresis generated through feedback [3]. Thus in the design of this circuit, it is desired to find the proper parameter R1, R2, R3, and C, and the transistor sizes to obtain hysteresis.

3. MOS VOLTAGE CONTROLLED RESISTANCE

The resistors of Fig. 1 can be made in IC form by the use of MOS transistors. For this two identical transistors, connected back-to-back such that one is operating in the saturation state while the other is in the nonsaturation state, will yield

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total current I which is essentially linear in V, where V > 0. Figure 3 shows the electronic circuit for the voltage controlled resistor. This resistor could be implemented by using n-type or p-type transistors. Other methods are given in the literature [4] - [5].

The PSPICE simulations of the resistors are shown in Fig. 4 for the I-V characteristics, with control voltage V as a parameter. The MOS voltage controlled resistor realized by the circuit of Fig. 3 possesses nonideal characteristics.

4. NEURAL TYPE CELL LAYOUT RESULTS

The MOS voltage controlled resistor of Fig. 3 is used in place of R1, R2 and R3 of NTC of Fig. 1b. The layout of the neural type cell is shown in Fig. 5 using MAGIC [6]. The PSPICE simulation of the circuit of Fig. 5 is shown in Fig. 6. In comparing the results of the lumped circuit, Fig. 2, we see that in realizing the integrated circuit NTC the effects of stray capacitors are directly related to the performance of the cell. Nevertheless, the integrated neural cell PSPICE simulation verified the expected behavior of the neural type cell. The final chip design is shown in Fig. 7. Several cells with different sizes have been designed and sent for fabrication though results on them are as yet unavailable.

ACKNOWLEDGEMENT

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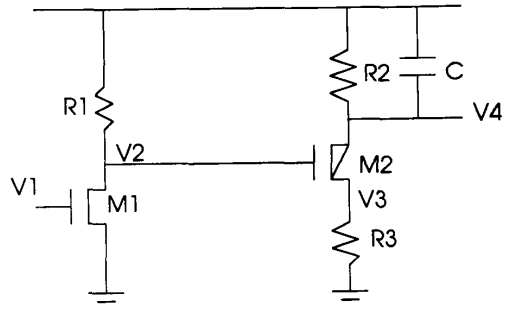

Fig. 1a

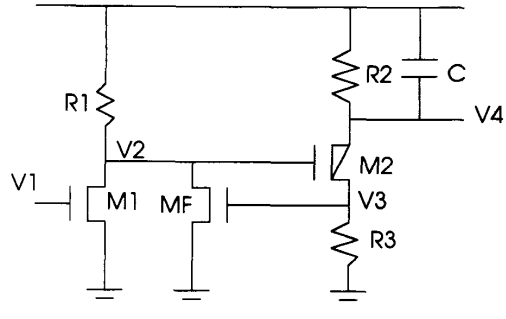

Fig. 1b

Fig. 1. Neural Type Cell (NTC)

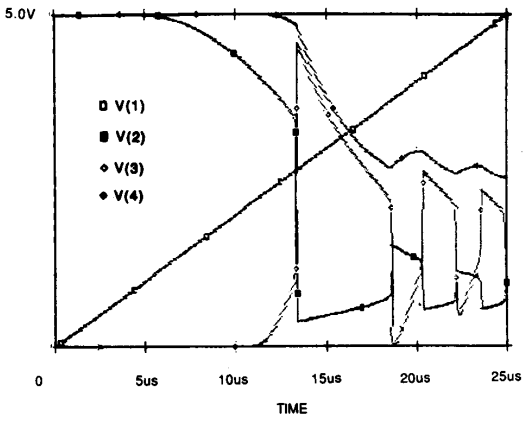

Fig. 2. SPICE Output of NTC

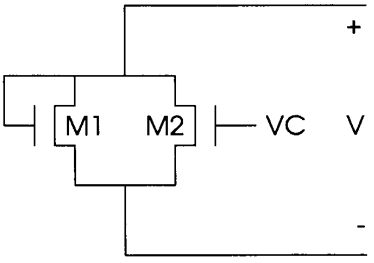

Fig. 3. MOS Voltage-Controlled Resistance

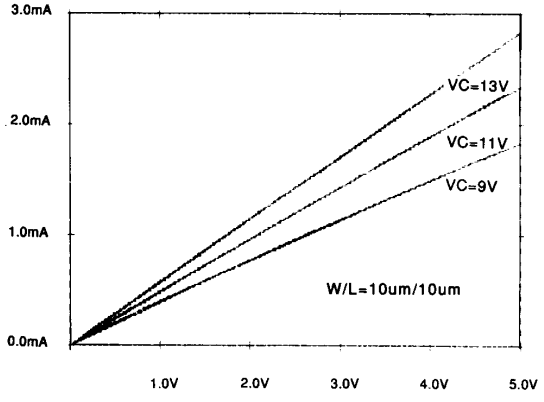

Fig. 4. Simulation Results of I-V Characteristics of MOS Voltage-Controlled Resistance of Fig. 3.

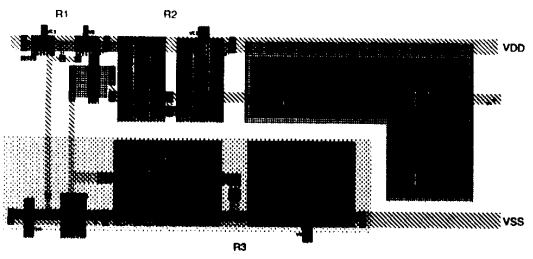

Fig. 5. Layout of NTC

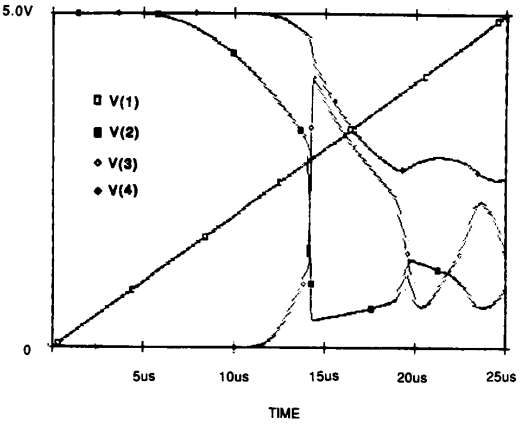

Fig. 6. SPICE Simulation Results of NTC Layout of Fig. 5.

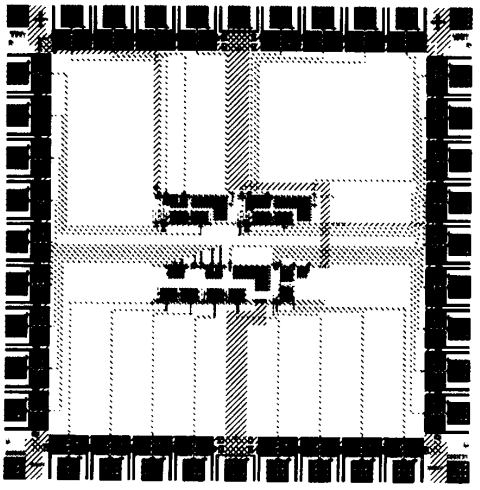

Fig. 7. Chip Layout