A CMOS VOLTAGE-CONTROLLED LINEAR RESISTOR WITH WIDE DYNAMIC RANGE

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ABSTRACT

A new type of voltage-controlled linear resistor utilizing a simple combination of complementary enhancement mode MOS transistors, is proposed. The design is suitable not only for discrete use but also for use as a unit cell in integrated circuits (IC's). The electronic structure and the IC layout of the circuit are given. The principle of operation is discussed and is verified by computer simulation (PSPICE). Parameters for the practical design have been established with satisfactory agreements with simulation results.

I. INTRODUCTION

In the past, several approaches towards the implementation of voltage-controlled resistors have been taken. Some acclaimed designs realize linearity in the I-V characteristics [1] [2] and others extend the dynamic range [3]. In this paper, we do both using enhancement mode CMOS technology. Although the authors of [1][2] proposed designs with a pronounced linearity, it is only over a small range and requires depletion mode devices. On the other hand, the authors of [3] use a feedback technique to extend the dynamic range of linearity. Although it works, their design is not suitable for integration since it requires quite a number of transistors to layout the Opamps in the feedback circuit.

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Here, because of our interest to obtain an integrable electronic circuit for a voltage-controlled linear resistor with a dynamic range that will allow for study of chaotic resistors in a stochastic network [4], we look at a nonlinearity cancellation technique. This technique accomplishes linearity by, basically, placing two transistors back-to-back. Moreover, we use two additional complementary transistors to compensate for the voltage range where nonlinearity is still present.

In order to implement the IC layout of the circuit, using the design rules and transistor specifications which are required by the manufacturer, MOSIS, we adjust the transistor parameters (i.e. channel width and length) and make the transistors operate in the enhancement mode.

In section II, the main portion of the paper, we discuss the technical description of the proposed circuit. Our discussion will proceed in the following format:

A. Principle philosophy
B. Circuitry
C. Computer simulation
D. IC layout

This is followed by section III which gives brief concluding remarks that open a number of future research paths.

II. LINEARIZATION OF ENHANCEMENT MODE TRANSISTORS

Electrically, a MOS transistor acts as a voltage-controlled switch that conducts initially when the gate-to-source voltage, V_{gs}, is equal to the threshold voltage, V_t [5]. When a voltage V_{ds} is

applied between source and drain, with $V_{gs}=V_t$, conduction occurs along the channel. When the effective gate voltage $(V_{gs}-V_t)$ is greater than V_{ds}, the channel becomes deeper as V_{gs} is increased. This is termed the unsaturated region where the channel current, I_{ds}, is given by:

$$I_{ds} = K*[(V_{gs} - V_t) - V_{ds}/2]*V_{ds} \quad (1)$$

$$K = C_{ox}*\mu*W/L$$

If V_{ds} is greater than $(V_{gs}-V_t)$, the channel becomes pinched-off, at which point the channel no longer reaches the drain. This is termed the saturation region in which the drain current is given by:

$$I_{ds} = K/2 * (V_{gs} - V_t)^2 \quad (2)$$

Therefore, below saturation, a MOS transistor performs the function of a variable resistor. However, as seen from equations (1) and (2), the I-V characteristics are asymmetrical and not linear.

A. Principle philosophy:

Our philosophy is to place two identical transistors back-to-back such that one is operating in the saturation state while the other is in the nonsaturation state with an offset bias battery inserted at the source end of the N-channel transistor (or to the drain end of the P-channel transistor). The total current I_D, which is the sum of the two currents through both transistors, is essentially a linear term. This linearity is good for the positive values of V_{ds}, since N-channel devices are used. To realize linearity in the negative range of V_{ds}, P-channel devices are placed, back-to-back, in parallel with the other two transistors. By symmetry, the same I-V characteristics are obtained (with negative current and voltage polarities).

B. Circuitry:

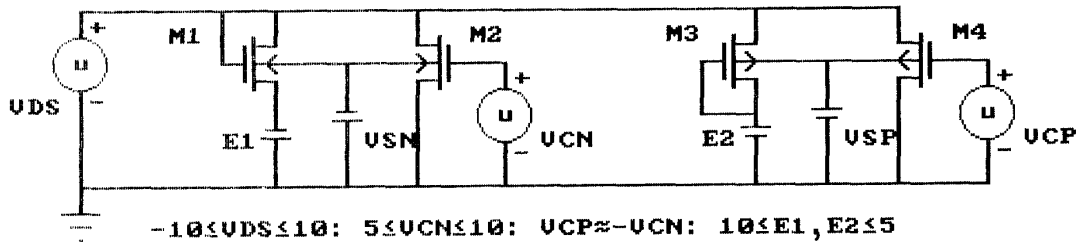
Figure 1 shows the electronic circuit for the proposed voltage-controlled resistor. Because N&P channel devices have different K's for equations (1) and (2), the ratio of W/L for the N-channel to the P-channel is approximately 1:2. The controlling voltage, V_c, at the P-channel is approximately the negative of the controlling voltage at the N-channel, but again this difference is due to using different threshold voltages for the N&P channel devices which are specified by MOSIS. The bias batteries, E1 and E2, are inserted to insure that the diode connected transistors are always turned on.

C. Computer simulation:

Figure 2 shows the typical I-V charac teristics from the PSPICE simulation (for 'V_C' = 5, 6, 7, 8, 9, 10 from bottom to top). From these, it is noted that the curves have a very linear nature in the voltage range from -6V to 6V. This is better than the results that were, previously, explored in the literature [1] [2] [3] in which linearity is assumed in the range from -3V to 3V. It is worth mentioning that increasing the magnitude of the bias batteries will further extend the region of linearity.

D. IC layout:

The layout of the voltage-controlled resistor, shown in figure 3, is implemented using MAGIC (a geometrical layout editor) [6]. The design rules specified by MOSIS (the Metal Oxide Semiconductor Implementation Service) are followed. Our layout has been sent to MOSIS to be fabricated by the latest technology offered, 2-λm P-well CMOS process that supports two layers of poly as well as two layers of metal. Since this design is considered



$-10 \le VDS \le 10$: $5 \le VCN \le 10$: $VCP \approx -VCN$: $10 \le E1, E2 \le 5$

$VSN = -10V$: $VSP = 10V$

FIGURE (1)

very small for fabrication, we have included several other cells, with different transistors' width and length, on the same chip. This will make our chip available for different applications depending on the designer's needs (i.e. various current ranging).

III. CONCLUDING REMARKS

By using a floating substrate and inserting batteries, E1 and E2, in the back-to-back connection of the matched pairs of N-channel and P-channel transistors, we have been able to realize linearity of the I-V characteristics over a wide range of input voltage, V_{ds}. In employing this technique, we choose the critical values for the parameters used, in accordance to mathematical formulas, such that an improvement in linearity is obtained. In addition, symmetry, in the shapes of the I-V curves, is manipulated by adjusting the controlling voltages, V_{cn} and V_{cp}.

As compared to other voltage-controlled resistors, our proposed circuit allows considerable linearization with fewer circuit components in CMOS technology. Moreover, we offer flexibility in extending the dynamic range by varying the substrate voltage. The transistors in the circuit are adjusted to operate in the enhancement mode as required by the present MOSIS design rules to realize the layout for the fabrication of the integrated circuit.

The voltage-controlled resistor, developed here, could be used in oscillators [7], controlled amplifiers, and attenuators. In particular, we take advantage of its extended range of linearity, and its electronic controllability to simulate chaotic behavior which could come from the heart during fibrillation or from the brain during epilepcy. The significance of such application could be a lead to a "Chaos Monitoring Device" that could be attached to the body [8]. The device could continuously, and in real time, track variations in the electrical impulses from the heart and give an immediate prognosis and an alarm warning a patient of the approach of a dangerous threshold.

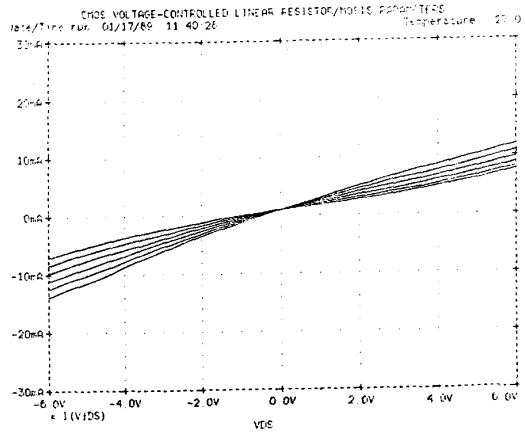


FIGURE (2)

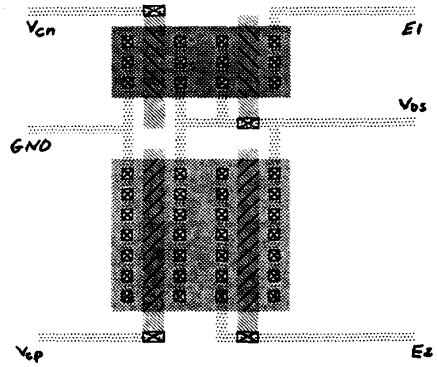


FIGURE (3)

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EFFICIENT GENERATION OF TESTS FOR COMBINATIONAL CMOS CIRCUITS

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ABSTRACT

This paper presents an efficient method for generating test patterns which yield high fault coverage for combinational Complementary Metal Oxide Semiconductor (CMOS) circuits. The method's efficiency is a consequence of: (1) its ability to simultaneously select test patterns for stuck-off and stuck-on transistor faults, and (2) its ability to generate test patterns which cover the common memory inducing faults, without the need for a conditionally sequential logic description. The proposed method consists of three steps. First, a simple procedure converts the transistor description of the CMOS circuit into a combinational logic description which represents the design-specified functionality of every transistor gate node of the CMOS circuit. Second, the standard D-algorithm is applied to the logic description using a reduced set of logical stuck-at-1 and stuck-at-0 faults. Third, a procedure generates an effective, yet short sequence of the D-algorithm test patterns which covers all of the stuck-on and stuck-off transistor faults.

INTRODUCTION

A number of conventional test generation algorithms have been developed for combinational circuits, including the D-algorithm [1], the literal proposition technique [2], and the fault table method [3]. Conventional test generation techniques identify and select primary input combinations that produce circuit outputs which are sensitive to the anticipated faults of the circuit.

The conventional algorithms typically use the stuck-at fault model and the logic description of the circuit to develop test patterns. The stuck-at fault model assumes that all physical faults can be modeled by gates responding as if circuit lines are permanently stuck at either a logic 1 or logic 0 value. The model also assumes that the logical functionality of gates within the circuit is unaffected by the fault. In other words, an AND gate continues to perform the AND function, even in the presence of a fault; only the lines connecting the AND gate with other elements are affected.

In combinational CMOS circuits, several common faults affect the circuit in such a way that the output is, under certain input patterns, a function of both the present input and a previous input. Such faults are sometimes called memory inducing faults because they cause the affected circuit to display memory. In brief, memory inducing faults transform combinational CMOS circuits into sequential circuits [4,5]. Examples of memory inducing faults include: (1) an open-circuited transistor drain connection, (2) an open-circuited transistor source connection, and (3) an open-circuited transistor gate connection.

As an example of a memory inducing fault consider the fault-free and faulty versions of a CMOS NOR gate shown in Figures 1 and 2, respectively. The fault illustrated in Figure 2 is a break in a line within the circuit. The faulty NOR circuit displays memory whenever the input pattern AB=10 is applied because the circuit's output terminal becomes electrically isolated from the two power supply nodes (V_{DD} and V_{SS}). Transistor capacitances between the

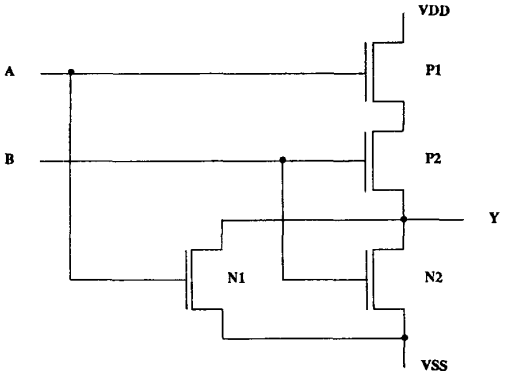

Figure 1: A fault-free CMOS NOR gate.

output node and the two power supply nodes will cause the output to retain the value that it had under the preceding input pattern. Consequently, the output is a function of the most recent input pattern that establishes a conducting path from either power supply node to the output terminal. For example, if the input sequence is AB=(11,10,10), the output sequence will be Y=(0,0,0). If the input sequence is AB=(00,10,10), the output sequence will be Y=(1,1,1). Clearly, both the second and third output values are a function of the first input pattern. Furthermore, the fault-free output for AB=10 is Y=0; therefore, the second sequence detects the fault, and the first does not.

In traditional test generation algorithms, no allowance is made for the possibility of sequential behavior by a faulty combinational circuit. As a result, the traditional algorithms blindly use a combinational description to generate tests for circuits that are sequential under certain faults. Furthermore, the traditional algorithms generate test patterns without specifying an ordering to the application of those patterns; the ordering is chosen arbitrarily. Therefore, a fault that causes sequential behavior can be detected, at best, only by chance.

Several researchers have addressed the problem of developing a satisfactory method of test generation for CMOS circuits [1,4-8,10,13]. The new methods have been designed in such a way that the generated tests reliably detect memory inducing faults, and those faults that appear as conventional stuck-at ones. In designing the new methods and algorithms, researchers have taken the approach of modeling the circuit as a logic circuit that is conditionally sequential. In other words, the logic circuit behaves sequentially when a