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IMPLEMENTATION OF PULSE-CODED NEURAL NETWORKS*

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ABSTRACT

The philosophy of pulse-coded neural-type networks is reviewed. Then some MOS circuits for their implementation are given. A means of obtaining the coding through hysteresis and a means of adjusting weights through MOS transistor threshold variation is discussed. Semistate theory is suggested as an ideal theoretical tool for neural network studies.

I. INTRODUCTION

It is well recognized that biological systems transmit information via action potentials [1, p.85]. For this, various forms of sensors convert information about the physical environment into trains of action potentials, which, as a consequence, contain a coding of information in the patterns of presence and absence of action potential pulses. In other words, biological neural systems contain their information in action potential pulse coding. This led electrical engineers in previous decades to formulate various theories of neural networks in terms of the processing of action potential-like pulses. A primary work of that era is the 1960 Ph.D. thesis of H. Crane which is summarized in his concept of the "neuristor" as presented in [2]. However, the field was handicapped by a lack of physical realizability, the ealy proposed devices using relays and tunnel diodes [2][3] both of which are rather impractical for large scale constructions. This led to the investigation of MOS devices for the realization of pulse coded neural-type networks [4], an area which continues with activity [5] due to the many advantages of MOS devices, including their low power consumption, their ease of fabrication, and their ability to be electronically adjusted.

Except for another exception that we know about [6], we note that this philosophy has been bypassed in the recent interest in neural networks. This recent interest deals almost exclusively with information coded into voltage levels which are considered to be interpretations of firing rates of biological neurons [7, p.2555]. Although this philosophy is having considerable success, at least on the relatively small scale circuits to which it is applied, the same results can be achieved with the biologically motivated philosophy of placing information via pulse code modulation. And some other advantages accrue, most notable of which is noise immunity.

II. THE BASIC CIRCUITS

Our circuits are made up of neural-type cells (NTC), neural-type junctions (NTJ), and neural-type lines (NTL). Interconnections of these devices form a neural-type network (NTN). The primary function of the NTC is to do pulse formation; thus the NTC contains dynamics and crucial nonlinearities. The NTC is the electronic analog of the neuron, or nerve cell, and can carry out the function of coding of sensed signals. The NTJ serves to combine signals and, as such, acts like the biological synapse. It can be simple or complex depending upon the nature of combinations desired - for example, it can incorporate both spatial and temporal summation as well as the setting of weights on its input signals. The NTL serves to transmit signals from place to place and, thus, serves like a nerve axon. Since the original neuristors were conceived as interconnections of NTLs, NTLs were originally conceived to incorporate the dynamics of NTCs. Still, an NTL can be as simple as a connecting wire or as complicated as a nonlinear transmission line of NTC sections, leading to partial differential equation or differential-difference equation descriptions.

In terms of MOS (Metal Oxide Silicon) transistors, Fig. 1 shows an NTC, Fig. 2 shows an NTJ and Fig. 3 shows an NTL with descriptions of these existing in the literature; see, for example, the references of [5].

Of special interest is the use of hysteresis in the NTC for effecting the coding of neural-type pulses with information [8]. Thus, through the use of hysteresis generated by the feedback transistor, Q_3 of Fig. 1, an external (sensed) voltage can be made to generate trains of neural-type pulses (analogous to action potentials). By changing the hysteresis width with the input amplitude, which naturally occurs due to the input transistor Q_1, an NTC can be made to change the frequency of pulse repetition in the output neural-type pulses. Thus, external sensory data can be encoded into pulse code modulated pulses that are to be processed within the network. On the other hand, if a neural-type pulse is received by an NTC the pulse is processed by the NTC in a manner somewhat analo-

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gous to the processing of action potentials in biological cells (meaning that there is refractory behavior, some delay, etc.).

In the NTJ circuit of Fig. 2 we see that the weight attached to each signal is set by the strength of the output current in each of the input structure circuits. The magnitudes of these currents are set by resistors, like R_1 & R_2, and transistors, like Q_1 & Q_2 in Fig. 2. Important here are the thresholds of Q_1 & Q_2 and the fact that these thresholds can be varied electronically, by various means, allowing for electronic adjustment and setting of the weights.

III. NEURAL-TYPE NETWORKS

By interconnecting the basic circuits of Section II we obtain neural-type networks (NTNs). Indeed any of the neural network architectures under use for the Hopfield, or similar, types of neurons can be used for the neural-type elements presented here to produce NTNs.

A general framwork for the analysis of such networks is semistate theory [9], which is a generalization of state variable theory which allows for nondynamic and dynamic portions to be included in the same equations. This latter is ideal for the characterization of neural networks because the weights (junctions) are usually nondynamic but the neurons (cells or processor elements) are usually dynamic.

IV. DISCUSSION

Here we have outlined the basic elements in the electronic construction of pulse coded circuits. More details on specific aspects can be found in the literature while considerable research is ongoing. For example, the semistate theory of neural networks is under development with especial emphasis to date upon the characterization of NTCs [10] and NTJs [11]. Likewise circuits which use nothing but MOS transistors have been designed, as well as electronically adjustable ones for voltage controlled adaptation of weights in NTNs.

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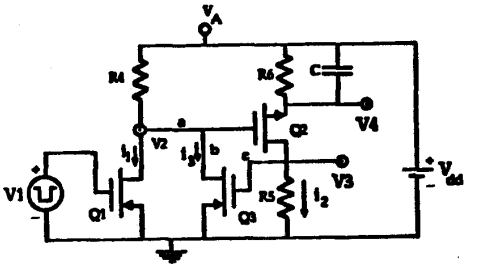

Figure 1. Neural-Type Cell = NTC

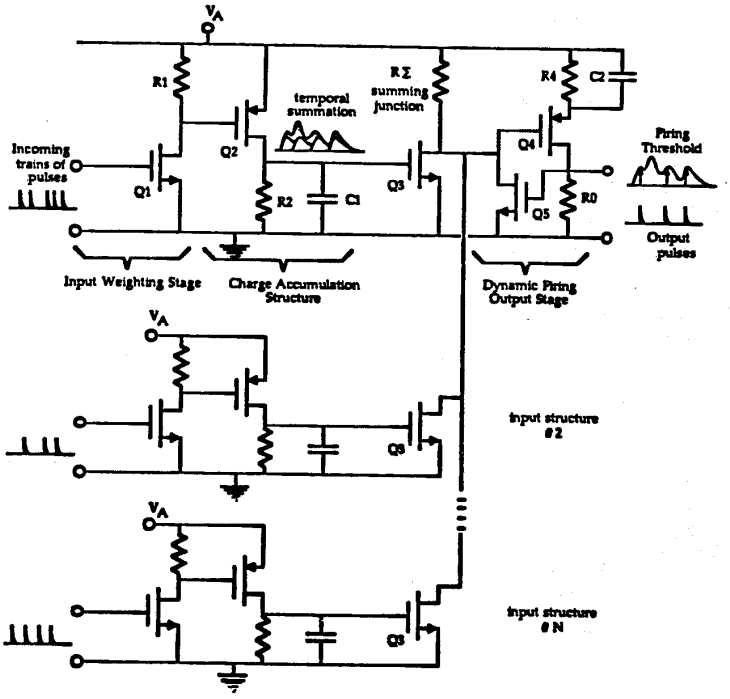

Figure 2. Neural-Type Junction ◘ NTJ

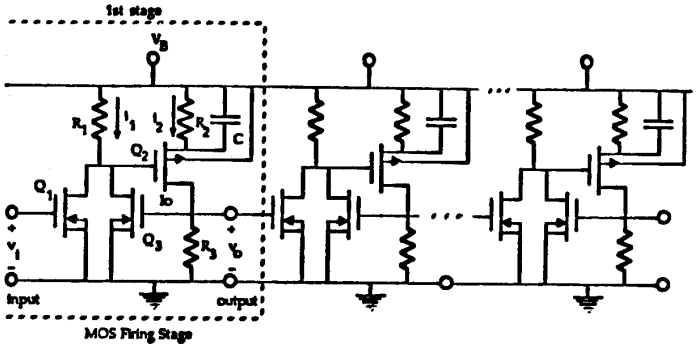

Figure 3. Neural-Type Line = NTL