# LOGIC GATE FORMED NEURON TYPE PROCESSING ELEMENT

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## ABSTRACT

A set of three neuron-type circuit elements based on logic gate circuits with multi-input multi-fan output capability is described. These three elements can be realized with standard logic circuits and are cascaded to form a neuron-type processing element from which neural-type systems can be constructed using off the shelf devices.

## 1. INTRODUCTION

The basic computational element or node employed in neural networks is nonlinear and relatively slow compared with modern digital computer components. The simplest of several analog model performs the sum of N continuous time, t, inputs $u(t)_i$ weighted by weights $W_i$ (positive and negative integer for excitation and inhibitory, respectively) and passes the results through a nonlinear operator, F, that perform a thresholding of threshold value $\theta$. The nonlinear operator is that of threshold logic with the input output relationship as follows [1][2][4]

$$y = F\left(\sum_{i=1}^{N} W_i \cdot u_i - \theta\right) \qquad (1\text{-}1)$$

It must be noted here that the summation results can be obtained in the physical neuron by two kinds of summation; Spatial and Temporal. The spatial summation is characterized by the fact that the input signals from different dendrites are available at the same instant of time, while for temporal summation the input signals from one dendrite are available such that the duration of their effective times overlap. This operation of summation is carried out in the axon base. However, prior to the axon base, the cell body performs the function of holding the excitation or the inhibitory pulse for a certain period of time in preparation for the two kinds of summation. In typical analog implementations of the summation of (1-1) it only spatial summation is obtained [3][4][5]. Thus, in order to completely specify the operation of the physical neuron a time factor must be introduced to accommodate the function of the soma for which purpose a time constraint variable $\tau$ is introduced in (1-1). Although this variable is difficult to incorporate in an analog type model, digital techniques can be utilized. In this paper a neuron-type processing element (NTPE) based on logic gate circuits with multi-input multi-fan output capability is described in terms of three subelements which mimic portions of the biological neuron. Using these, NTPEs neural-type systems, including computers can be conceived and constructed using presently available off the shelf components. Section two describes the new logic based design of the NTPEs. The input pulses to the neuron and the output pulses of this model will be shown (Fig. 5).

## 2. NTPE DESIGN

This section provides the proposed NTPE based upon its association to the biological neuron. The design structure of this NTPE is shown in Fig. 1 where three types of subelements are introduced, one called the dendritic and cell body, anorhter representing the axon base, and the final element representing the axon itself. The logic design implementation is based on NAND gates which perform the same functions as the physical neuron, namely temporal summation, spatial summation, and thresholding. The NTPE computes the sum of N inputs $u(t)_i$ in continuous time t weighted by the binary weights $W_i$ and passes the results through a non-linear binary operator F that performs a thresholding of threshold $\theta$ and an input combining in time $\tau$, as to be discussed, to give its binary output y(t) according to

$$y = F\left(\left(\sum_{i=1}^{N} W_i \cdot u_i - \theta\right), \tau\right) \qquad (2\text{-}1)$$

In this we require that the threshold $\theta$ be set so that the neuron will fire, i.e., y will be 1, if three or more pulses are available and when m input pulses are present (where m is greatest integer less or equal to $\theta - 1$) then a next pulse must arrive in an interval of time $[0,\tau]$ in order to obtain a pulse output. This time constraint is apparent when temporal summation is carried out by the physical neuron but not in spatial summation. This interval of time requires an action within the NTPE to maintain the input pulses for a short period of time to allow the triggering pulse to have a $\tau$ interval in which to interact (this being like a soma action). Thus, each input pulse has an effective time. This time interval is essential for the implementation of temporal summation. For example, if all excitatiroy and no inhibitory input pulses arrive to the neuron's different dendrites at the same instant, then spatial summation is performed in which case the threshold value is reached. However, if pulses arrive to the same dendrites at different times, then temporal summation is carried out only the during the overlapping effective time of the pulses.

The designed circuit has the same structure as asynchronous sequential circuits, but it differs in operation in the sense that this circuit contains one input dependent stable state to which it



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passes after going through appropriate unstable states. The stable state will continuously produce an output equal to logical 1 when the threshold and effective time criteria are satisfied. This is exactly the holding of the pulse for certain amount of time. The memory elements used are time delay elements that can be adjusted for the time required for the internal states to transit from one state to another. The input ports receive signals $u_i$ which are to be processed. These inputs are held for a period of time $\tau$ inside the cell body, thus satisfying the condition of (2-1). The output of the cell body is in turn processed in the axon base circuit. Finally, a NTPE output is produced after the processing function of (2-1) is computed, including summing and thresholding. The structure of each part will be discussed alone, then the three elements are cascaded to produce the desired design model for the NTPE from which the input-output functions can be illustrated.

## 2.1 Cell Body

The input signals received by the input ports of the neuron are held in the cell body circuits for a finite period of time, $\tau$. During this time, the cell body will send a continuous pulse to the axon base. At each input port of the cell body, a logic input port circuit (IPC) is designed to perform the required functions; receiving, holding, and sending pulses. The designed IPCs are structured to enable performing these operations without interaction with the other IPCs. Thus each IPC of any input port of the neuron is completely independent from other IPCs. This structured feature enables the addition of more IPCs as needed if the number of dendrites increases. In Fig. 1 three IPCs are chosen. This is in proportion to the selected threshold level for the spatial summation. Each IPC is composed of a number of block input port subcircuits (IPSC). Each of these IPSCs is responsible for one signal at a time. This feature gives the IPC the ability to maintain more than one signal, received through its corresponding input port. In our proposed model the number of IPSCs is based on the minimum number of pulses as required by the threshold of the axon base. This will enable the designed circuit to perform the temporal summation. Upon the arrival of the excitation pulse, which has duration at least $\tau$, to the input port of $IPC_1$, $IPSC_{11}$ (the first IPSC of the first IPC) is required to provide the axon base with a pulse that has a duration greater than that of the input pulse, this giving the holding effect of the excitation pulse. If a second excitation pulse arrives to the same IPC, $IPSC_{12}$ will hold the second pulse. If a third third pulse arrives to $IPC_1$, $IPSC_{13}$ will hold the third input pulse, etc..

The IPSC is designed similar to an asynchronous sequential circuit such that its output pulse represents the effective time of the input pulse resulting from the soma action. That is, the output will equal a logical 1 for a duration equal to the time required for the circuit to go though its cycle from the stable state to unstable states and return back to the stable state after being stimulated by an input pulse. Accordingly, this time can be controlled by inserting delay whenever needed, for example, by using two NAND gates connected in cascade. The designed circuit is shown in Fig. 2. In design of any asynchronous sequential circuit, the problem of race must be resolved. In this design the race condition is solved by requiring that the circuit follow a predetermined state transition path that prevents it from returning to its stable state until it passes though the other states. This is accomplished by designing a circuit containing three NAND gates (gates 3, 4, & 5 of Fig. 3).

The race problem and its solution introduces a restriction on the duration of the input pulse in that the input pulse must be maintained long enough until the output signal of a fourth gate is logical zero. This condition will enable the designed solution to prevent the race condition. Thus the minimum duration of the input pulse is equal to five NAND delays. The width of the output pulse is proportional to the delay inserted plus the time required for the circuit to progress from a stable state and back to the same stable state. Thus, the output pulse can be extended to last as long as desired. Typically, this duration is five times the duration of the input pulse as found in the physical neuron.

The IPC contains three IPSCs connected to the input port through the recieving unit, this being a NAND gate that steers the input pulses according to their sequence. For example, if a first pulse arrives $IPSC_1$ will be activated. If the second input pulse arrives $IPSC_2$ will handle this pulse. This is accomplished such that $IPSC_2$ is connected to the input port through a NAND gate that will insure that $IPSC_2$ will hold the input pulse if and only if $IPSC_1$ is busy (holding a previous input pulse). Similarly for $IPSC_3$ with the input of $IPSC_2$. The total circuit of the cell body is shown in Fig. 1. It contains three IPCs each handling one dendrite. Each IPC has three IPSCs connected to one input port of the dendrite. This enables the circuit to handle three pulses per input port and three input ports. This feature coincides with the characteristic of the cell body where pulses are presented to the axon base for temporal and spatial summation. Note that an extra IPC is included in the cell body to handle an inhibitory pulse input $u_4$ whenever it occurs and passes it to the axon base faster than the IPCs of the excitation pulses.

## 2.2 Axon Base

The axon base of the NTPE performs the summation and thresholding as described by (2-1). In this equation we require that the $W_i$ be binary numbers with a 1 for positive excitation. The value of the threshold is determined by requiring that the axon base takes three input pulses to fire. This makes the value of $\theta$ equal to three. In order to perform the two kinds of summation, temporal and spatial, using NAND gates, input output relationships are determined based on the availability of the cell body outputs. If there are three pulses available, the logic circuit shown in Fig. 3 will produce an output equal to logical 1 which in turn is used as an input to the axon. The the firing of the axon depends on temporal or spatial summation being performed. This restriction is purposely introduced to simplify the circuit without losing the functionality of the axon base. The axon base will order the axon to fire if the following logical functions are true ($Q_i$ is the output $IPSC_i$

belonging to IPC$_i$ ):

1 - TEMPORAL Summation:

$$\begin{aligned} &\text{i- } G_{i1} \text{ AND } G_{i2} \text{ AND } G_{i3} \text{ OR} \\ &\text{ii- } G_{21} \text{ AND } G_{22} \text{ AND } G_{23} \text{ OR} \\ &\text{iii- } G_{31} \text{ AND } G_{32} \text{ AND } G_{33} \end{aligned} \qquad (2\text{-}2)$$

2 - SPATIAL Summation:

$$\begin{aligned} &G_{11} \text{ OR } G_{12} \text{ OR } G_{13} \text{ AND} \\ &G_{21} \text{ OR } G_{22} \text{ OR } G_{23} \text{ AND} \\ &G_{31} \text{ OR } G_{32} \text{ OR } G_{33} \end{aligned} \qquad (2\text{-}3)$$

Since the inhibitory synapse is closer to the axon base than the excitation synapses, delay functions are inserted at the input ports of the axon base circuit (as in Fig. 3) to accommodate the timing of the arrival to the output gate. Thus, if an inhibitory signal is available at the axon base, this is immediately executed prior to the excitation signals. The inhibitory effect is accomplished by the fourth set of input ports in Fig. 3 which will try to prevent the firing of the neuron if:

$$G_{41} \text{ OR } G_{42} \text{ OR } G_{43} \qquad (2\text{-}4)$$

The function of the axon base is taken as:

$$\begin{aligned} Y = &[(G_{11}+G_{12}+G_{13})(G_{21}+G_{22}+G_{23})(G_{31}+G_{32}+G_{33})+ \\ &(G_{11}\cdot G_{12}\cdot G_{13})+(G_{21}\cdot G_{22}\cdot G_{23})+(G_{31}\cdot G_{32}\cdot G_{33})] \\ &\overline{(G_{41}+G_{42}+G_{43})} \end{aligned} \qquad (2\text{-}5)$$

## 2.3 Axon

The function of the axon is to produce a number of output pulses based on the duration of the axon base output pulse. Thus, the longer the duration of the pulse the larger number of pulses produced by the axon. A possible logic circuit is depicted in Fig. 4.

## 3. Simulation

The operation of a designed NTPE circuit for both spatial summation and temporal summation has been simulated. The input and the output pulses are shown in Fig. 5a and 5b, respectively. The duration of the input pulses were chosen as 6ns. The output, for the case of temporal summation, became logical 1 when three pulses were completely inside the cell body. The spatial summation output became logical 1 when three input ports were activated. The final simulation was the effect of the inhibitory input. When the input port of the inhibitory input was activated the output of the circuit, i.e., of the axon, was logical 0 for the duration of the effective time of this pulse. The action of the inhibitory input is illustrated in Fig. 5c 1 and 2.

## 4. CONCLUSIONS

This paper has shown the design of neuron-type circuit elements based on logic circuits, mainly NAND gates. Three types of subcircuits were introduced, one called the cell body with its dendritic inputs, another representing the axon base, and the final one mimicing the axon. The resulting design was an asynchronous sequential circuit. This NTPE computes the sum of binary weighted input pulses incorporating temporal as well as spatial summation and thresholding. This process has been accomplished by introducing the time constraint variable $\tau$ in the operation of the NTPE. With the availability of VLSI techniques to implement these NTPEs, full neural-type systems, including computers, can be conceived and constructed using presently available IC technology. Alternatively they can be assembled from off the shelf logic circuits.

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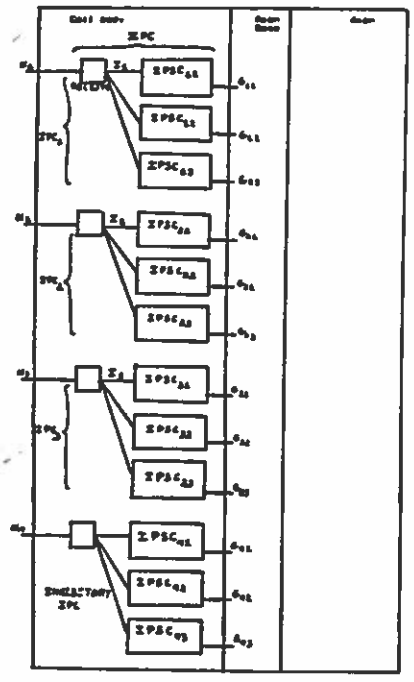

Figure 1 NTPE with IPCs & IPSCs

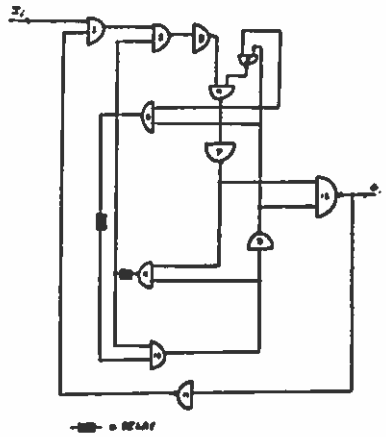

Figure 2 Logic Circuit of IPSC
Delay = 2 Nand Gates

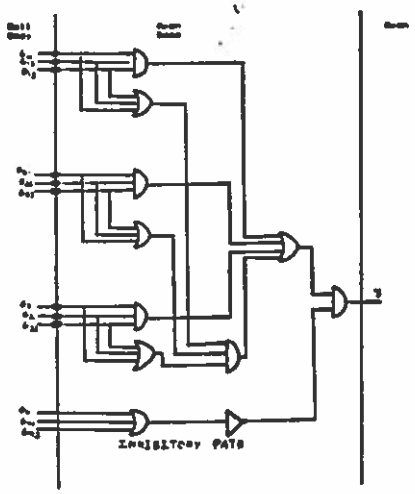

Figure 3 Axon Base Circuit

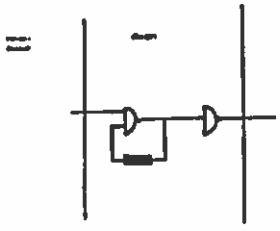

Figure 4 Axon Circuit

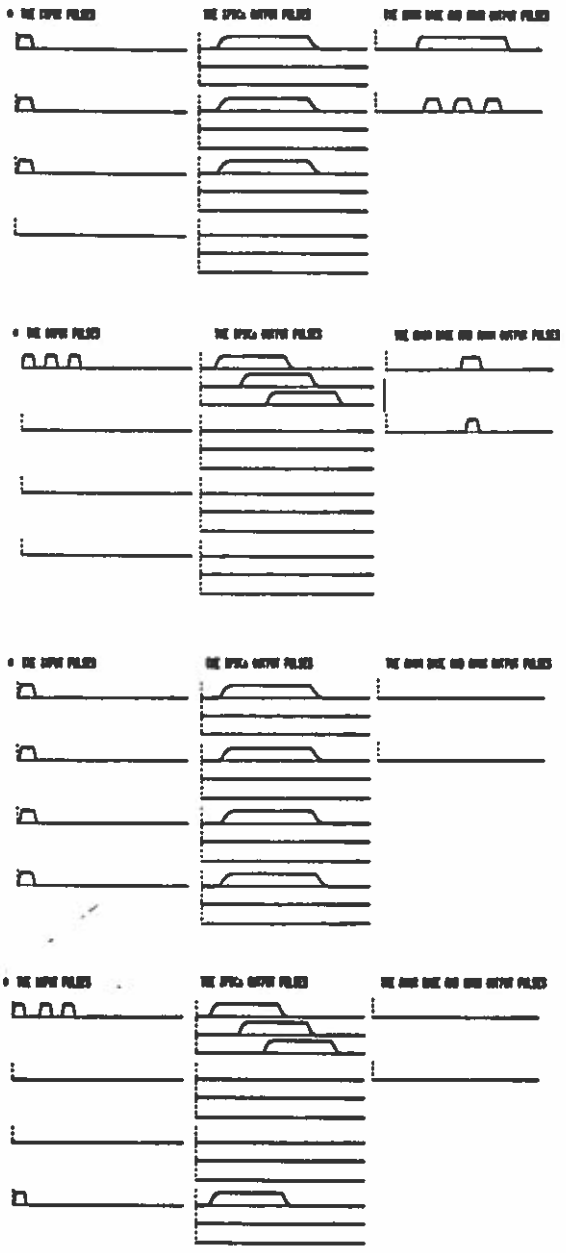

Figure 5 Input - output Pulses
(a) Spatial
(b) Temporal
(c) Inhibitory

Typical NAND Gate Delay = 0.55 ns

Input Pulse Duration Used = 6 ns (ports 1-3)

Inhibitory Pules duration = 6 ns (port 4)

Number Of Input Excitatiory Port Circuits = 3

Number Of Inhibitory Port Circuits = 1

Effective Duration of Effective Time = 36 ns

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