# Hysteresis in Neural-Type Circuits*

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ABSTRACT

The mechanism of generation of hysteresis in a neural-type cell is presented. This leads to a set of equations that can be used for the design of MOS transistor neural-type cells which give pulse code modulation for the coding of information in neural-type systems.

## I. INTRODUCTION

Since neural pulses comprise the "universal language of the nervous system" [1, p. 34] as interpreted in modern physiology, it is of interest to generate neural-type pulses which are pulse code modulated. An MOS circuit to do this has been available in the literature [2] with its use spelled out [3] and semistate equations set up [4]. As seen from [4] the circuit operation rests upon the presence of hysteresis which is controlled by the input signal. This hysteresis is seen by an RC load in the source of the controlling transistor of the dynamic firing output stage, and, consequently, shows up in the i-v characteristics seen looking into that transistor's source. To this point, though, only experimentally measured or simulation data was available to characterize that hysteresis. Here we give an analytical development which yields an expression for the hysteresis parameters and, therefore, allows us to initiate a design formalism.

## II. HYSTERESIS

Consider Fig. 1 which is the NTC cell [4] with the RC circuit removed which attaches to the source (upper lead) of the p-channel transistor $Q_2$. Since it merely acts as a current source for our purposes, here the input transistor of the NTC (called $Q_1$ in [4]) is so replaced by its drain-to-source current via the current source $I_i$. We desire to obtain the characterization of i versus v, with these variables as defined in Fig. 1.

Because hysteresis is present we use a parameter, this being the voltage $v_1$ across the input current source $I_i$. First we obtain $v_1$ as a function of i due to the operation of the feedback transistor $Q_3$. Then we obtain i versus $v_1$ with v as a parameter due to the operation of the dynamic firing transistor $Q_2$. The two resulting curves can be plotted as i versus $v_1$ with one slid along the other as v varies to get the multivalued i versus v curve.

To make the theory tractable we assume that the hysteresis determining MOS transistors $Q_2$ and $Q_3$ operate in their square-law region when turned on. Thus, their descriptions are taken to be

$$i = \beta_2(v-v_1-V_{T2})^2 1(v-v_1-V_{T2}) \quad (1a)$$

$$i_3 = \beta_3(R_L i-V_{T3})^2 1(R_L i-V_{T3}) \quad (1b)$$

Here 1(.) is the unit step function and the transistor parameters $\beta_2$, $\beta_3$, $V_{T2}$, & $V_{T3}$ are all taken positive (we also assume that $v \geq v_2$). When $v_1>0$ we have

$$v_1 = V_{DD} - R_1 I_i - R_1 i_3 \quad (2)$$

from which we find that $Q_3$ turns on at

$$i_{t_0} = V_{T3}/R_L \quad (3a)$$

when also $v_2$ drops from the value

$$V_1 = V_{DD} - R_1 I_i \quad (3b)$$

From (2) and (1b) we find that $v_1$ drops to 0 at

$$i_0 = i_{t_0} + R_L^{-1}[V_1/R_1\beta_3]^{\frac{1}{2}} \quad (3c)$$

The curve for i versus $v_1$ as determined by $Q_3$ via (1b)-(3c), called $i_1(v_1)$, is plotted as in Fig. 2a). To go with it is the curve for i versus $v_1$ with v as a parameter determined by $Q_2$ via (1a), called $i_2(v_1,v)$. This is as plotted on top of the curve of Fig. 2a) in Figs. 2b)-f) for five important values of v (v=0, v=a, v=c, v=a, v=d, respectively, with a, b, c, d, defined in (4) below).

For each value of v the two curves of Fig. 2 intersect, sometimes with multiple intersect points, to give the values of i that go with v. As v is increased the $i_2$ curve moves to the right and as v decreases it moves left. Jumps between the two vertical branches of the $i_1$ curve occur at different values of v, giving the hysteresis. Figure 3 shows the result, giving the hysteresis, where the labeled voltage axis points are given by

$$a = V_{T2} \quad (4a)$$

$$b = V_{T2} + V_1 \quad (4b)$$

$$c = V_{T2} + (i_0/\beta_2)^{\frac{1}{2}} \quad (4c)$$

$$d = V_{T2} + V_1 + (i_{t_0}/\beta_2)^{\frac{1}{2}} \quad (4d)$$

The upper curve of Fig. 3 is described by

$$i = i_u = \beta_2(v-a)^2 1(v-c) \quad (5a)$$

and the lower curve is given by

$$i = i_l = \beta_2(v-a)^2 1(v-b)1(d-v) \quad (5b)$$

We see that the condition for hysteresis is that c<d which can be evaluated in terms of circuit parameters as

$$[R_L\beta_2(R_1\beta_3)^{\frac{1}{2}}]V_1^2 - V_1^{\frac{1}{2}} + 2(R_L\beta_2 R_1\beta_3 V_{T3})^{\frac{1}{2}} > 0 \quad \text{(hysteresis condition)} \quad (6a)$$

When (6) holds the hysteresis width, $v_{hw}$, is given by d - c which is

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$$v_{hw} = V_1 + V_{T3}/(R_L\beta_2))^{\frac{1}{2}}\{1-[1+((V_1/(R_1\beta_3))^{\frac{1}{2}}/V_{T3}]^{\frac{1}{2}}\} \quad (6b)$$

As an example, for which the curves of Figs. 2 & 3 were drawn using MATHCAD, consider the circuit of [4] which has $V_{DD}$=10v, $I_1$=3.94ma, $\beta_2=\beta_3$=0.00063, $V_{T2}=V_{T3}$=2v, $R_1=R_L$=2KOhm, the transistor values being those for the MC 4007 package and $I_i$ resulting from choosing a 4.5v input to a similar transistor. Then $i_o$=1ma, $i_{to}$=1.65ma, a=2, b=4.125, c=3.61802, d=5.38488 and we see that the hysteresis condition d>c is satisfied and $v_{hw}$ = d-c = 1.77v. To obtain neural-type pulses we wish to choose a load line that passes through the two vertical portions of the hysteresis of Fig. 3, with a lower limit for the load line passing through v=d on $i_1$ and an upper limit passing through v=c on $i_o$ giving

$$R_{load\ max} = (V_{DD}-d)/i_{to} \quad (7a)$$
$$R_{load\ min} = (V_{DD}-c)/i_o \quad (7b)$$

In this case we find $R_{load\ min}$ = 6.62KOhm and $R_{load\ min}$ = 3.87KOhm. Thus, connecting a resistor of range 3.87KOhm - 6.62KOhm between the upper two contacts of Fig. 1 should yield neural-type pulses in this example. In using the MICRO-CAP model we found in [4] that a smaller value had to be used, i.e, 3KOhm resistor in parallel with a 50pfd capacitor yields the neural-type pulses of Fig. 4 where $I_i$ is stepped up from zero to the 3.94ma value at 100Ns. The discrepency in load line resistance value seems to come from the fact that actual transistors have parasitics and operate some of the time in the ohmic region, yielding a slight modification to the hysteresis which accounts for the practical use of a slightly smaller load than Fig. 3 indicates. Also it should be noted that c<b means that there is another hysteresis present, which has not been treated here since practically i will remain at 0 until v=b as v increases from below c.

## III. DISCUSSION

Under the assumption that the active operation is in the square-law region for the two hysteresis determining transistors we have shown that the conditions for hysteresis can be given for the NTC. This depends upon the input, represented by $I_i$, in a critical and quite nonlinear way, as seen by (6a) where $V_1$ is linear in $I_i$ by (3b). Equation (6b) gives the hysteresis width and, consequently, can be used as a guide in designing NTC's for the purpose of pulse code modulating information sensed via $I_i$. As seen above the square-law model is always not exact enough, so an analytic model including the ohmic region needs development. Still the results give an engineering feeling for the important parameters determining the hysteresis.

## REFERENCES


[1]. W. F. Ganong, "Review of Medical Physiology," Twelfth Edition, Lange Medical Pub., Los Altos, CA, 1985.

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[3]. N. El-Leithy, R. W. Newcomb, and M. Zaghloul, "A Basic MOS Neural-Type Junction; A Perspective on Neural-Type Microsystems," Proceedings of the IEEE ICNN, San Diego, June 1987, pp. III-469 - III-477.

[4]. R. W. Newcomb and N. El-Leithy, "Semistate Description of an MOS Neural-Type Cell," Proceedings of the MTNS, Phoenix, June 1987, to appear.

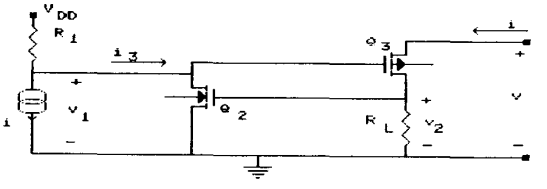
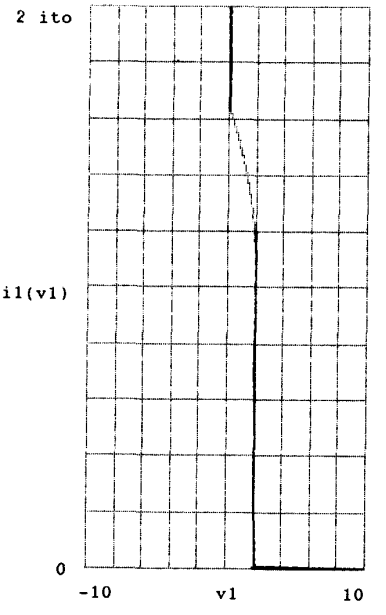
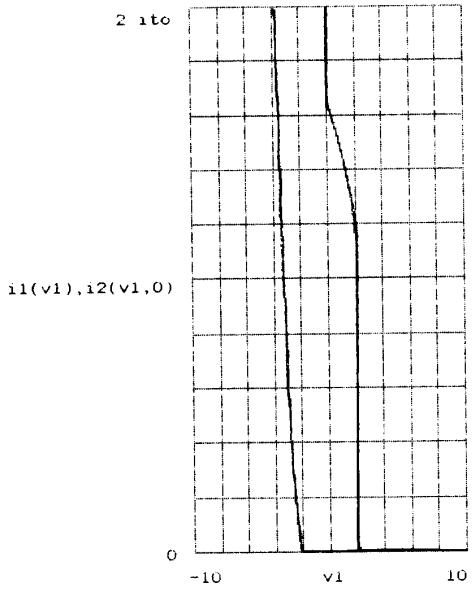



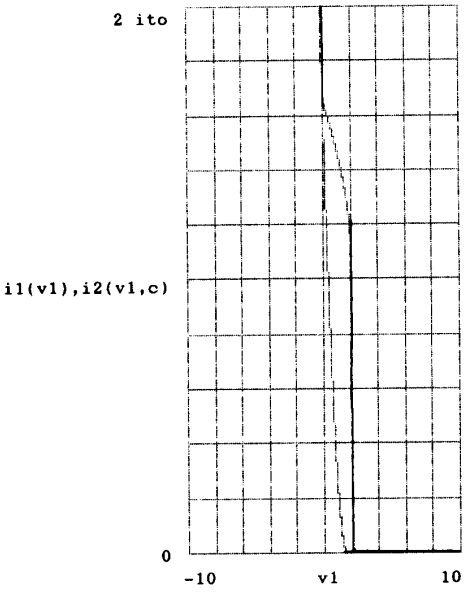

Figure 1
Circuit for i versus v Hysteresis



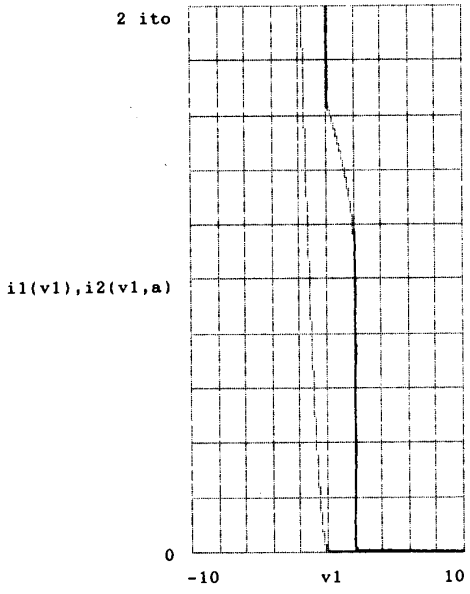

2a) $i_1$ versus $v_1$



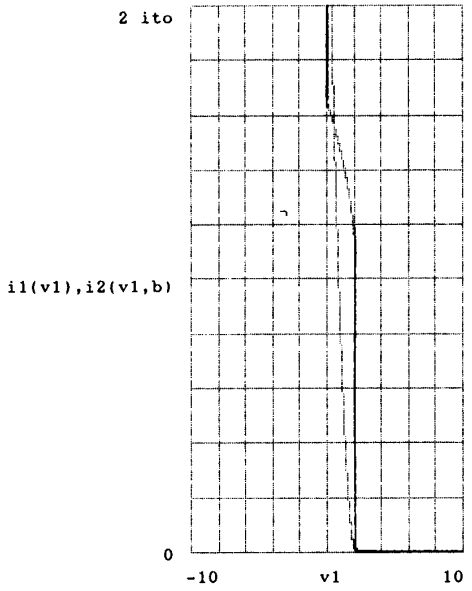

2b) $i_2$ versus $v_1$ for v=0



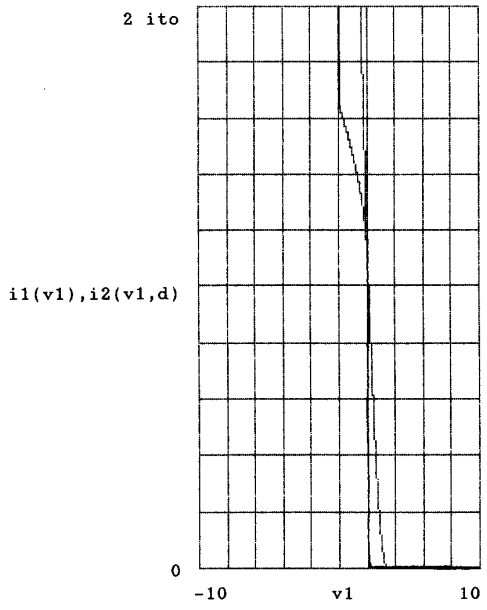

2d) $i_2$ versus $v_1$ for v=c




2c) $i_2$ versus $v_1$ for v=a




2e) $i_2$ versus $v_1$ for v=b




2f) $i_2$ versus $v_1$ for v=d

Figure 2
$i_2$ Superimposed on $i_1$ for Various v

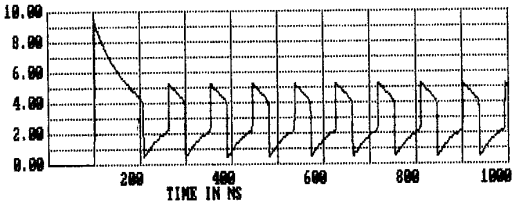
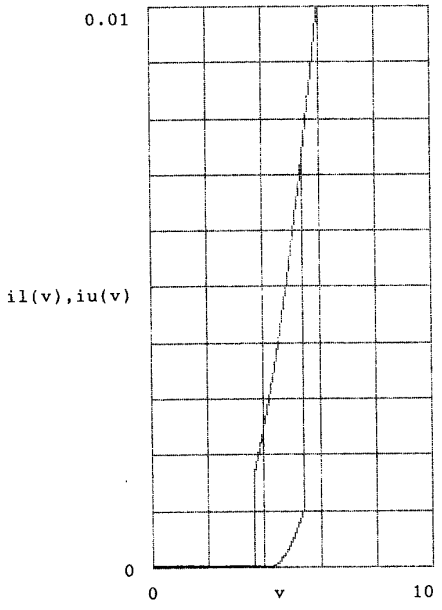



Figure 4
Typical Neural-Type Pulses Generated




iu(d) = 0.00722

iu(c) = 0.00165 =io

$i_l(d) = 1 \cdot 10^{-3}$ =ito

a = 2 b = 4.125
c = 3.61802
d = 5.38488

Figure 3
i versus v Hysteresis