Multi-Valued Processors Using Solitons*

S. Minkara@, N. El-Leithy@, H. Youssef@,
V. Rodellar#, P. Gómez#, & R. Newcomb#,

@Microsystems Laboratory
Electrical Enginnering Department
University of Maryland
College Park, Maryland 20742 USA

#Grupo de Sistemas (PARCOR)
Facultad de Informática
Universidad Politécnica de Madrid
Ctra. de Valencia, Km. 7,00
28031 Madrid, Spain

Abstract

The concept of multi-valued processors based on solitons at N different amplitudes is introduced. In such a system, solitons act to propagate signals and to form proper levels. It is shown that such a system can be realized by N binary computers in one soliton processor or by one N-Algebra soliton processor. Means of constructing logic systems based on the neuristor concept of Crane, modified to fit the solitons, are discussed.

I. INTRODUCTION

In this paper a new multi-valued systems philosophy is presented. Rather than work with point processors we turn to the use of travelling pulses and their manipulation. We note that systems to handle travelling pulses are available for VLSI realization via the Surface Electrode Transistor (SET) [1]. The SET is a device that can be used to realize multilevel characteristics conveniently [2] and leads to circuits with behavior that is soliton-like. We here propose a method of using our previously discussed soliton circuits [3][4] in multi-valued processors.

In part II we review pertinent topics on solitons and in part III we discuss two ways by which these solitons can be used to implement processing via multi-valued logic.

II. SOLITONS AND NEURISTORS

The solitons which we propose to use for multi-valued processors are special types of solitary pulses which propagate on a soliton line, or in a soliton lattice, without changing form and enjoying the following properties [5][6][7][8][9]:

1) Solitons propagate at fixed velocities and retain their shape.

2) Solitons of higher amplitude travel at a rate faster than those of lower amplitude.

3) When solitons collide they do not interfere with each other. That is, after a collision the pulses retain the same properties that they had before a collision.

Otherwise said, solitons are specially formed pulses that travel in a system where they retain their shape even after colliding with other solitons. Indeed, it is this ability to persist even after collision that primarily distinguishes solitons from other solitary waves. Water waves are special cases of solitons, as are some pulses that propagate in plasmas and optical fibers [5][10]. Since they are special cases of solitary waves, techniques available for design of processing systems using solitary waves may be adaptable to the design of soliton systems. In particular, this is true of systems based on neural pulses, such as the neuristors of Crane [11], which have been shown to be suitable for the construction of computers. But a soliton system has a big advantage over the neuristor. This advantage is that in a soliton system N different levels of solitons may simultaneously exist on a soliton line or lattice and solitons at these different levels need not interact.

From these properties we make the critical observation that in a soliton system we may process pulses at one set of amplitudes independently of another set while using the same equipment to support all of the solitons.

III. MULTILEVEL PROCESSING

Here we discuss two basic ways to use solitons in multivalued processing. In both of these the solitons act to propagate information and combine together to form new solitons into proper levels. To introduce these alternatives we note that the key property of the soliton we wish to use is that signals at different levels propagate independently of each other, at differing speeds, and, when they come together on a soliton line, they pass through each other without distortion. In other words information on one level is not confused with information on another

* This research was supported in part by NSF Grant MIP 85-06294 and in part by the US-Spain Joint Committee for Scientific and Technological Coorporation under Grant No. CCB 86-04017.

level on a soliton line. To use these properties we can proceed by working with each level conceived as a separate binary system or we can work with all levels simultaneously via an associated algebra which combines information among the levels. Besides propagating signals on soliton lines, it is necessary for signal processing applications to combine signals, for which new concepts and circuit devices must be introduced into a soliton processing system. We use the key notions previously developed by Crane [11] for neuristors; however, since solitons do not destroy each other, as neuristor pulses do, the techniques of Crane also need modification.

In specifying the levels at which the processor will work, we set allowed levels separated by non allowed levels. In making this separation, enough room should be left between pulse levels to allow for interference due to noise so that pulses at one allowed level do not switch into another allowed level. In addition to this consideration, one needs to take into account that during a two soliton collision, the combined pulse is at an amplitude that is not one of the two amplitudes of the pulses. Thus, one needs to place all possible amplitudes resulting from colliding pulses outside of the allowed levels. Once this is done, then when one finds a pulse at the amplitude of colliding pulses, one does not process it immediately but takes steps to separate it into its constituent pulses. If pulses that are outside of the allowed levels arrive, then they must be corrupted pulses. Consequently, error correction steps would need to be taken to remove the noise or other interference corrupting them.

A. N-Binary computers in one soliton processor

In this case we use the fact that a soliton at level m out of the possible N levels can be considered to interact only with other solitons at the same level m. Then at each level m we can work with the soliton pulses as if they are pulses in a binary computer. Consequently, we set up interaction of pulses at a fixed level to be in accordance with the rules of a binary computer. That is, we use Boolean algebra logic in manipulating the mth level soliton pulses for any m. In this case we need logic circuits that are capable of performing the customary operations [12] of AND, OR, and NOT, etc., on pulses of the separate levels. In designing devices where pulse interactions take place, we use circuits that independently process the different levels. To accomplish this we can use the neuristor techniques of Crane. In particular, we can form Crane's T and R junctions which he shows can be combined to yield the above mentioned logic circuits. Here the T junctions are simply fan outs of soliton lines. However the R junctions require refractory periods which are in turn used for the annhilation of pulses. To obtain the refractory periods we can create refractory cells via use of the SET [2], or any other desired solid-state device such as MOS transistors, that will allow discharging of a solitary line when appropriate pulses are passed through. References [2], [3], and [4] give means to construct solitary lines using solid-state devices. In doing this we note that it is possible that two or more pulses of different levels could arrive at the point where the logic function is to be performed. Since we wish to perform the logic functions on only pulses at a given level, it is necessary to separate the pulses at different levels for this processing. Such a separation can occur by gating the simultaneous different level pulses into a short section of soliton line where a separation will naturally take place due to the different speeds of propagation of different level soliton pulses. Of course such a gating only is to take place if two different amplitude pulses arrive simultaneously, where by simultaneously, we mean any time overlap that leads to the movement of pulses into non-allowed levels.

B. N-algebra soliton processor

In this case we wish to be able to manipulate any of the N level soliton pulses in the processor with any other pulse in the processor with the result being an allowed pulse of the system. In reality we wish to implement an algebraic structure appropriate to multi-valued logic, with the various values being defined as the allowed levels of solitons within the processor. As any such logic can be described by a ring [13][14], and a ring is characterized by two distinguished operations, here denoted by + and $\cdot$, we wish to manipulate the soliton pulses via circuitry that realizes these two operations. In other words, if pulses at levels x & y represent the numbers x and y in a multi-valued logic then $u=x+y$ and $v=x\cdot y$ are both defined numbers in the multi-valued logic being implemented by the soliton processor. Consequently, we design circuits that give a soliton pulse at level u for x+y and level v for $x\cdot y$. One approach to design such circuits is carried out in Gutierrez [15] where again the neuristors of Crane are suitably modified to perform the two operations. In the theory of Gutierrez pulses are interleaved in special ways to form AND and OR. Here we would interleave in the same manner, except that if two pulses of different amplitude are simultaneous we run them through a separator to be sure that the

pulses are not simultaneous so that true interleaving can occur. Practically this means that every AND and OR gate needs to contain a separator.

IV. DISCUSSION

By using solitons which inherently support arbitrary levels of pulses, we have shown the possibility of a new class of multi-valued processors. These support soliton pulses at prescribed levels and allow manipulations between pulses of different types. In one type only pulses at the same level combine. In another type pulses at all levels combine. To make the system noise immune one desires that there be a separation of levels. Thus, one carries out designs for only certain prescribed levels with these levels avoiding those of simultaneous soliton pulses.

Using small energy VLSI devices, such as the SET, the soliton processors proposed here should be practically realizable and should offer advantages of operation in inherently noisy environments at small energy cost. However, much remains to be developed before such advantages can be actually realized in practice. Especially investigation of separators is needed. As pointed out by one of the reviewers, a sensitivity study is needed to explore the complete integrability property of solitons when used in the computer context.

REFERENCES

[1]. T. Tamama, K. Murase, and Y. Mizushima, "Voltage-Controlled Negative Resistance in a Submicron Vertical JFET," Solid-State Electronics, Vol. 27, No. 10, October 1984, pp. 855 - 866.

[2]. S. Minkara, N. El-Leithy, and R.W. Newcomb," Applications of a VLSI SET in Analog Signal Processing," Proceedings of the 30th Midwest Symposium on Circuits and Systems, Syracuse, August 1987, to appear.

[3]. R. W. Newcomb, V. Rodellar, and P. Gómez, "A Nonlinear Lattice for Multivalued Neural-Type Logic," Proceedings of the 1985 IEEE Workshop on Languages for Automatic, Palma de Mallorca, Spain, June 1985, pp. 44 - 46.

[4]. N. El-Leithy, R. W. Newcomb, T. Aldave, V. Rodellar, and P. Gómez, "Multilevel Neural-Type Lattices," Proceedings of the 1986 IEEE Workshop on Languages for Automation, Singapore, August 1986, pp. 237 - 242.

[5]. M. Toda, "Theory of Nonlinear Lattices," Springer-Verlag, Berlin, 1981.

[6]. R. Hirota and K. Suzuki, "Theoretical and Experimental Studies of Lattice Solitons in Nonlinear Lumped Networks," Proceeding of the IEEE, Vol.61, No.10, October 1973, pp. 1483 - 1491.

[7]. M.J. Ablowitz and H. Segur, Solitons and the Inverse Scattering Transform, SIAM, Philadelphia, 1981.

[8]. G. Eilenberger, "Solitons," Springer-Verlag, Berlin 1981.

[9]. P. G. Drazin, "Solitons," London Mathematical Society Lecture Note, Series 85, Cambridge University Press, Cambridge, 1983.

[10]. R. Hirota, "Exact N-Soliton Solution of a Nonlinear Lumped Network Equation," Journal of the Physical Society of Japan, Vol. 35, No. 1, July 1973, pp. 286-294.

[11]. H. Crane, "Neuristor- A Novel Device and System Concept," Proceedings of the IRE, Vol. 50, No. 10, October 1962, pp. 2048-2060.

[12]. F. J. Hill and G. R. Peterson, "Introduction to Switching Theory and Logical Design," 3rd edition, John Wiley & Sons, New York, 1981.

[13]. J.C. Muzio and T.C. Wesselkamper, "Multiple-valued switching theory," Adam Hilger Ltd., Bristol, 1986.

[14]. G. Birkhoff and T.C. Bartee,"Modern Applied Algebra," McGraw-Hill, New York, 1970.

[15]. J. Gutierrez, J. Mulet and W. Warzanskyj,"Boolean Multiple-Valued Logic Based on Neuristor Properties," Proceedings of the 26th Midwest Symposuim on Circuits and Systems, Mexico, August 1983, pp. 66 - 69.