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VLSI IMPLEMENTATION OF A DIGITAL FILTER FOR HEARING AIDS

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ABSTRACT

Through the present paper a Digital Filter for Hearing Aids is described. A Signal Processing Method based on a one-dimensional model of the Inner Ear is presented, and a proposed Architecture based on a "bit-serial" 16 bits two's complement fixed point arithmetic is introduced. An evaluation of Real Time Execution, Area and Power Dissipation for a 2 µm. nMOS realization is given. Results of simulations and other practical considerations are discussed.

INTRODUCTION

During the recent years a great effort has been devoted to the design of new Hearing Aids [1, 2]. These may be classified as "External" to the Auditory System, or as "Internal" (embedded in part into the Auditory System by means of surgery). Both kinds of Hearing Aids may be represented by Fig. 1.

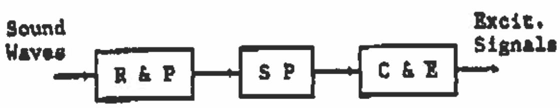


Fig. 1. General Diagram of a Hearing Aid.

The block labeled R&P translates sound waves into electrical signals. SP is the Signal Processing Unit, which reproduces the Frequency Selectivity of the Auditory System. C&E is the Coding and Exciting Unit, and translates the ouputs of MS into sound waves (External Aids) or to trains of pulses (Internal Aids) simulating the Transduction Process in a real Auditory System [3]. When conventional banks of filters [4] are used in SP according with the Theory of Hearing [5] the adjustment of their time response may be critical for the perception of certain nonstationary sounds [6, 7]. A Signal Processing Strategy is herein presented [8], which may ensure more natural transient responses. Its implementation as a VLSI Digital Filter is described, some evaluations and results being discussed.

SIGNAL PROCESSING MODEL

The Auditory System may be viewed as the block diagram of Fig. 2. Sound Waves are pre-Processed in the Outer and Middle Ears (O&M). The main frequency selective mechanism is the Membrane System (MS) within the Cochlea. Its outputs are Transduced and Coded (T&C) into signals stimulating the Auditory Nerve.

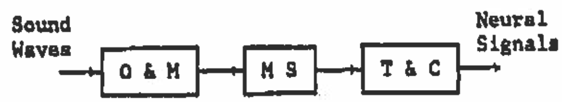


Fig. 2. General Diagram of the Auditory System.

We will concentrate on the behavior of MS, which may be reproduced by the transmission line model [5, 9] in Fig. 3.

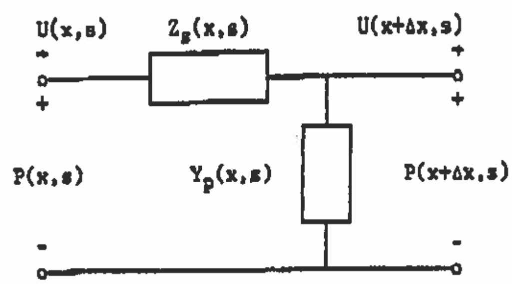


Fig. 3. Incremental Section of MS.

We will assume that MS is being excited from the Middle Ear by a flux U(x,s) a pressure P(x,s) appearing between both sides of the membranes in MS. The relation between P and U at a given point in the Laplace Domain may be given by the following differential equations:

$$\frac{\delta P}{\delta x} = - Z_s\, U \qquad (1)$$

$$\frac{\delta U}{\delta x} = - Y_p\, P \qquad (2)$$

$Z_s(x,s)$ and $Y_p(x,s)$ being:

$$Z_s = l\, s \qquad (3)$$

$$Y_p = [\mu\, s + \sigma + \varepsilon\, s^{-1}]^{-1} \qquad (4)$$

l, μ, σ and ε are the cochlear parameters as functions of x. We will express this model in the time domain introducing the definitions:

$$P = Z_c\,[F + G] \qquad (5)$$

$$U = F - G \qquad (6)$$

F and G are the incident and reflected waves in the model, both functions of x and s, with:

$$Z_c = [Z_s/Y_p]^{\frac{1}{2}} \qquad (7)$$

Equations (5-6) may be solved for one section, assuming constant line parameters. The behavior of such a section would then be given by:

$$F'_{k-1} = F_{k-1}\, e^{-\gamma_k \Delta x_k} \qquad (8)$$

$$G_{k-1} = G'_{k-1}\, e^{-\gamma_k \Delta x_k} \qquad (9)$$

$$\begin{vmatrix} F_k \\ G'_{k-1} \end{vmatrix} = \begin{vmatrix} 1-\rho_k & -\rho_k \\ \rho_k & 1+\rho_k \end{vmatrix} \begin{vmatrix} F'_{k-1} \\ G_k \end{vmatrix} \qquad (10)$$

ρ_k and γ_k being the reflection and propagation coefficients:

$$\rho_k = \frac{Z_{ck} - Z_{ck-1}}{Z_{ck} + Z_{ck-1}} \qquad (11)$$

$$\gamma_k = [Z_{sk}/Y_{pk}]^{\frac{1}{2}}\, \Delta x_k \qquad (12)$$

Z_{ck}, Z_{sk} and Y_{pk} are the respective functions evaluated at the right interface of the section. Equations (8-10) are the basis of the proposed model, and we will rewrite them in the domain of z by means of the Bilinear Transformation [10] as:

$$e^{-\gamma_k \Delta x_k} \approx \frac{2 - \gamma_k\, \Delta x_k}{2 + \gamma_k\, \Delta x_k} \qquad (13)$$

$$\rho_k(z) = c_{k0}\, \frac{1 + 2\, z^{-1} + z^{-2}}{a_{k0} + a_{k1}\, z^{-1} + a_{k2}\, z^{-2}} \qquad (14)$$

where γ_k is:

$$\gamma^2_k = \frac{4\, l_k\, f^2_m\, (1 - z^{-1})^2}{a_{k0} + a_{k1}\, z^{-1} + a_{k2}\, z^{-2}} \qquad (15)$$

The realization of (8-10) is shown in Fig. 4., in which FPRF and FPRG are the filters realizing (8) and (9) while FRF implements (11). a_{k0}, a_{k1}, a_{k2} and c_{k0} are functions of the line parameters, and f_m is the sampling frequency.

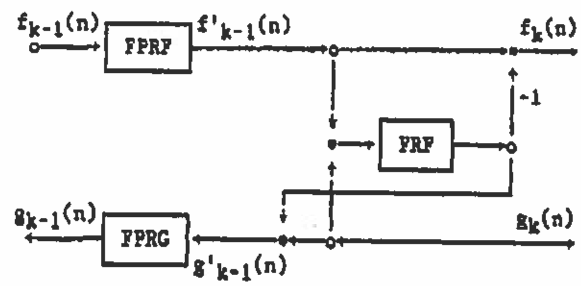
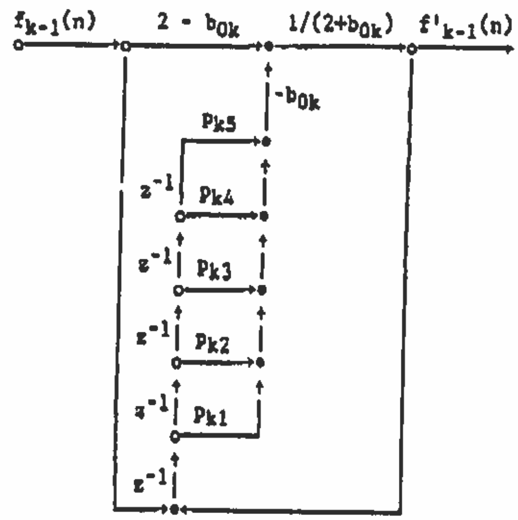


Fig. 4. Global flowgraph for one section.

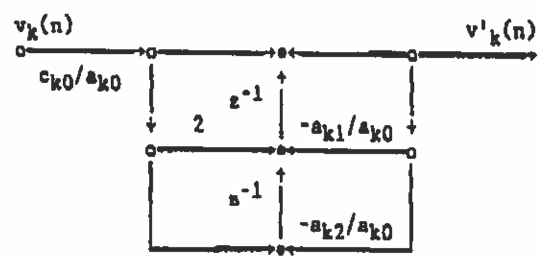
As implied by (15) the propagation function is irrational, and the inversion of (13) to the time domain will be done by a series expansion:

$$\frac{F'_{k-1}(z)}{F_{k-1}(z)} \approx \frac{2 - b_{0k}\,[1 + P_k(z)]}{2 + b_{0k}\,[1 + P_k(z)]} \qquad (16)$$

where b_{0k} is function of the line parameters, and $P_k(z)$ is a polynomial in powers of z^{-1}. As it seems reasonable $P_k(z)$ will have infinite terms, but in our case five coefficients will suffice. Expressions (14) and (16) may be expanded into the flow graphs shown in Fig. 5.



a) Flowgraph for FPRF and FPRG.



b) Flowgraph for FRF.

Fig. 5. Propagation and Reflection functions.

The proposed Signal Processing Model should be viewed as the realization of the flowgraphs in Fig. 5 into the global flowgraph of Fig. 4. The output of the model will be the membrane dynamics [11] given by:

$$v_k(n) = \frac{1}{\Delta x_k\ D}\,[f_k(n)-g_k(n)-f_{k-1}(n)+g_{k-1}(n)] \quad (17)$$

When implementing the overall MS structure by connecting several such sections, as given in Fig. 6, a new problem arise.

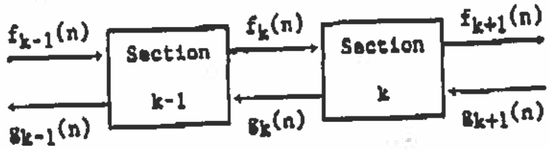


Fig. 6. Constraints in connecting two sections.

The problem is that to evaluate $f_k(n)$ and $g_{k-1}(n)$ we will need to know $f_{k-1}(n)$ and $g_k(n)$. The first value would have been evaluated at step k-1, with k increasing, but $g_k(n)$ will not be available yet, because it must be evaluated at step k. Reversing the recursion with k decreasing does not help much, because in that case the problem appears on $f_k(n)$ in evaluating $g_k(n)$ and $f_{k+1}(n)$. To solve this problem we have to reconsider the behavior of the filters FPRF and FPRG. These represent the affects of propagating a wave through one section, and as such, when properly adjusted, they should introduce a unit delay, as may be inferred from Fig. 5.a. In fact, forcing:

$$b_{0k} = 2 \quad (18)$$

we will break the delay-free path between the input and output, and the results will depend only on data stored in the Internal File of the filters, allowing two or more global sections to be directly connected as in Fig. 6. The flowgraph in Fig. 5.a. becomes that in Fig. 7.

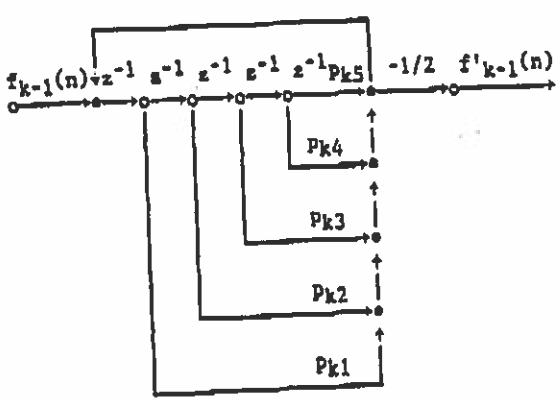


Fig. 7. Time separated flowgraph for $e^{-\gamma_k \Delta x_k}$.

As it can be shown [11], b_{0k} depends on the wave group velocity at the given point, and (18) means choosing the section length Δx_k according with the parameters at that point:

$$\Delta x_k = \left[\frac{4\mu_k\ f^2_m + 2\sigma_k\ f_m + c_k}{l_k} \right]^{\frac{1}{2}} 1/(f_m) \quad (19)$$

In what follows we will assume that condition (18) holds for any section being synthesized.

PROPOSAL FOR A PRACTICAL ARCHITECTURE.

We have followed the ideas in [12] for sequential number processing when synthesizing the flowgraphs in Fig. 5.b. and 7. The proposed architecture is a Sequential Data Hardwired Machine with bit-serial buses. Data word length is 16 bits fixed point two's complement. The general structure may be seen in Fig. 8.

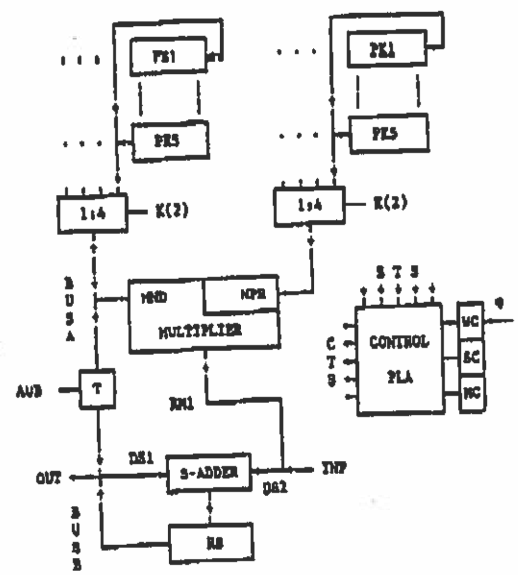


Fig. 8. Signal Processor Architecture.

Other characteristics of this structure are serial multiplication and addition, and multiplexed access to Data and Coefficient Files (PE and PK). This same machine may implement FRF. In a first approach we will deal mainly with speech signals, for which a bandwidth of 5 kHz. has been assumed, the sampling rate having been established in 10 kHz. When using these data to evaluate Δx_k from (18) with the parameter values taken from [13] we find that four sections will suffice to represent the whole cochlea. Then we have to multiplex four different files of data on the arithmetic units as implied in Fig. 8. Increasing the sampling rate will yield a higher number of sections, but this will in general improve the representation for frequencies above 5 kHz. The Time Data Transfer Diagram of the Machine is exposed in Fig. 9.

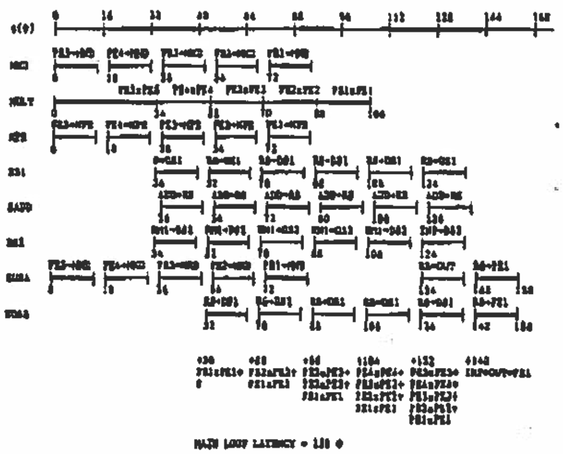


Fig. 9. Register Transfer Time Diagram for FPR.

The guard bits between transfers will guarantee a reliable data transmission between piles and arithmetic resources. The number of machine cicles (Φ) to complete the execution of a FPR graph is 158. A similar evaluation for FRF in the same hardware will cast a number of 122 machine cicles. Having in mind from Fig. 4 that the execution of one section requires two FPR and one FRF, this means at least 2x158+122=438 cicles. We will add up 62 cicles more to cover minor operations as those in (17) to complete a total of 500 cicles per section. To execute four sections in one sampling interval of 100 µsec. we need a clock period of 50 nsec., or a frequency of 20 MHz.

VLSI IMPLEMENTATION

We have chosen a 2 µm. realization for the architecture described in the last section based on a well known nMOS cell library [14]. The serial arithmetic units (multiplier and adder) have been built using functions from this library, and the register piles have been configured with serial shift register cells. The pile selector and multiplexer have been designed with parts taken from the PLA section. The Control Unit has been designed also around a PLA structure, its inputs being the status (STS) of the arithmetic units and the timing signals from the word (WC=16 Φ), section (SC=500 Φ) and sampling (MC=2000 Φ) clocks. The Control Unit provide the signals firing the transactions through the structure (CTS). Fig. 10 shows a simplified floorplan for the different units on a square chip of 2500 λ sides, this implying an area of 25 mm². An evaluation of Power Dissipation under worst case conditions gives an estimate of 2140.2 mW.

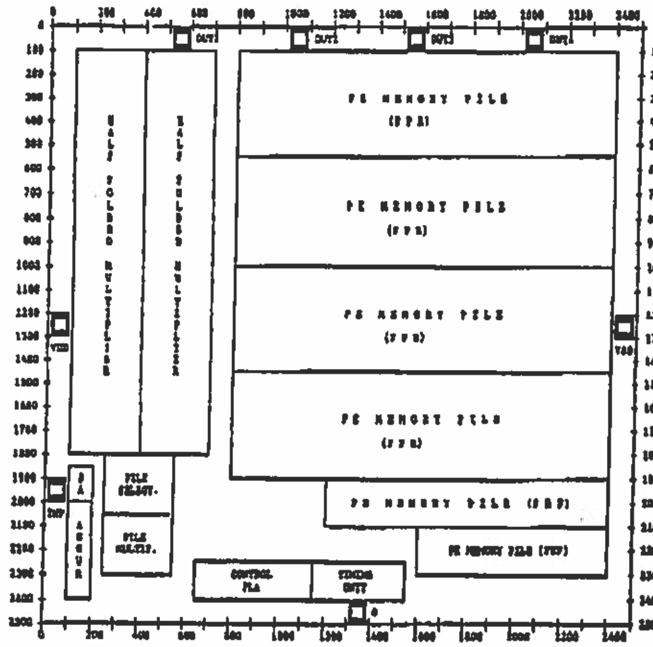


Fig. 10. Signal Processor Floorplan.

Power dissipation will force us to choose a less consuming technology like CMOS [15] to implement critical sections, as the data piles. The use of different technologies will split the whole architecture in two different chips, for Arithmetics/Control and Memory.

RESULTS AND DISCUSSION

The implementation of a Signal Processing Unit of the kind described is under progress. The results presented here have been produced by a computer simulation of the filters FPR and FRF. In Fig. 11 we may appreciate the impulse response of FPR for a section at x=1.68 cm. from the basal end.

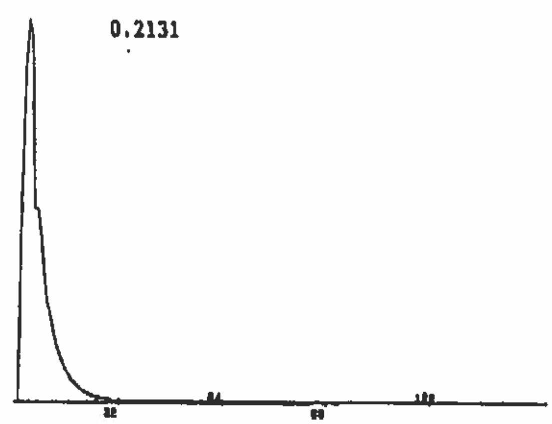


Fig. 11. Impulse response for FPR.

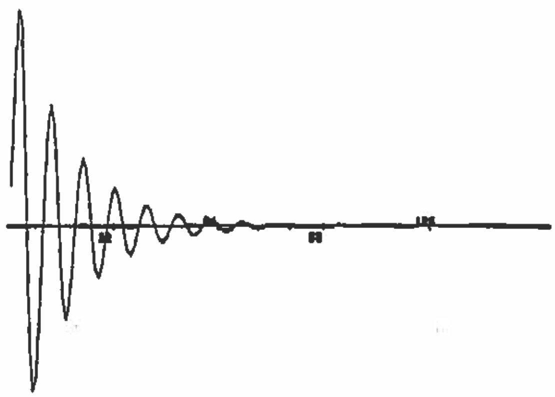


Fig. 12. Impulse response for FRF.

It can be seen that the response of FPR is one sample delayed respect to the unit impulse. Atenuation and dispersion may also be appreciated. The response to FRF lasts about 100 samples (10 msec.) this fact implying a long latency in the system, which could produce slow decaying responses of the kind known as "Kemp Echoes" [16]. The VLSI implementation of this Hearing Aid is being done using the primitive declaration system proposed in [12] for FIRST. The method of implementing the FPR sections may be further optimized. More compact realizations could be used, such Least Square all-pole structures [17]. This fact would imply reductions in the computational complexity of a section from order 13 (current) to order 7-9. The limitation in the number of sections may be by-passed using interpolation. An important aspect of the simulation is the numerical representation accuracy and rounding error effects in arithmetic operators. This study is being done using 16 bit microprocessor standard arithmetics, and the results seem to perform reasonably well. The performance of the system with speech signals is being studied in depth.

ACKNOWLEDGEMENTS

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