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APPLICATIONS OF A VLSI SET IN ANALOG SIGNAL PROCESSING*

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ABSTRACT

The SET is reviewed and shown to be a very useful device for VLSI implementation of some analog signal processing systems. A means for incorporating capacitors in the VLSI layout is given along with a preliminary mathematical characterization of the SET. Using these a solitary wave circuit is proposed with its potential for use in neural type circuits discussed.

INTRODUCTION

The surface electrode transistor, SET, has been introduced as a voltage controlled device that is ideal for VLSI [1]. This because it is a self-aligned vertical transistor which operates at high speed, has a considerable transconductance, and is very reproducible. Consequently, the SET has been proposed as an ideal device for VLSI logic gate fabrication [1]. In addition it also has a very interesting N-type negative output admittance with the characteristics variable via the gate voltage which should make it ideal for analog signal processing. Here we discuss the possibilities of use of the SET for VLSI analog circuit design. For this we review some of the key concepts of the important, creative, and to our knowledge only, paper presently available covering the SET [1]. Along with the resistors that can be designed directly with the SET we introduce a means of incorporating capacitors into the structure. Taken in total these should allow for the construction of a neural-type line, NTL, as is also discussed.

THE SET

Part a) of Fig. 1 shows a cross section of the upward mode SET with a circuit symbol introduced in part b). The important point is that the diffusion depths of both the drain and gate layers are negligibly small (less than 200 Angstroms), thus, allowing for a very simple fabrication. It has been constructed from amorphous Si-Ge-B material which supports amorphous Si resistors to be simultaneously fabricated with the SET, the details being covered in [1].

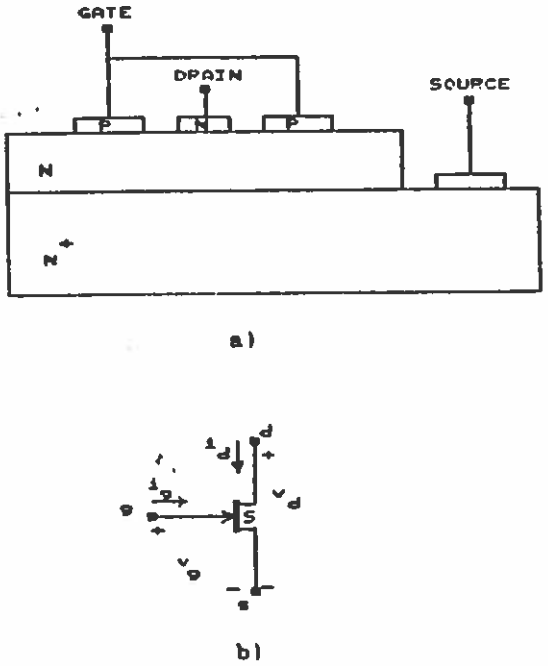

Figure 1
a) SET Cross Section, b) SET Circuit Symbol

Figure 2 shows typical SET curves (for v_g=1, 1.4, 1.8 from left to right). From these it is noted that, for nonzero gate voltage, the drain current is negative for small drain voltages and that the output characteristic has an N-type negative conductance form of a very nonlinear nature. There is also a very strong dependence of the output characteristics upon the gate voltage. The input characteristic is somewhat of diode form but is also gate voltage dependent while behaving like an open circuit for drain voltage somewhat above the gate voltage.

Although [1, Sec. 4.1] gives an almost circuit like characterization of the SET based upon unijunction type of operation [2], we are unable to duplicate the SET curves from that, either through mathematically solving the equations or via simulation in SPICE and MICROCAP. Consequently, we have developed the following characterization by way of curve fitting

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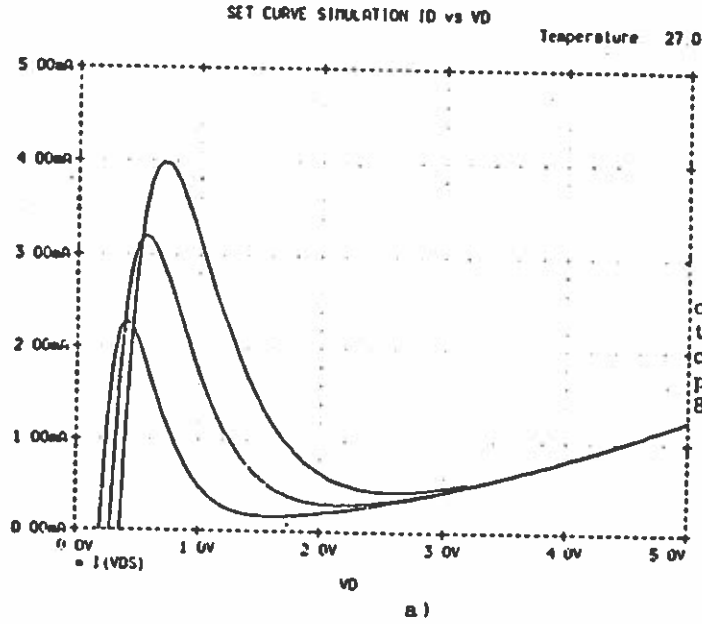

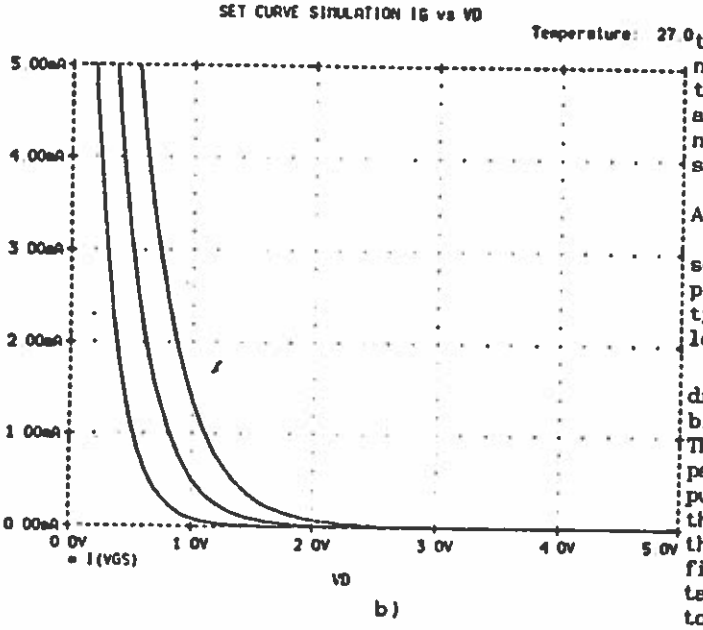

Figure 2
Typical SET Characteristics
a) Drain, b) Gate

$$i_d(v_g, v_d) = A(v_d - Bv_g)\exp(-C(v_d - Bv_g)/v_g) + Dv_d^2 \quad (1a)$$

$$i_g(v_g, v_d) = ABv_g\exp(-C(v_d - Bv_g)/v_g) \quad (1b)$$

In equations (1) A, B, C, and D are curve fitting constants for which we use for the device presented in [1]

$$A = 5 \text{ ma}, \; C = 1/B = 5, \; D = 0.001 \text{ ma} \quad (2)$$

On noting the details of fabrication we observe that it is also possible to include capacitors in the fabrication steps, since these can be constructed via an oxide layer placed between two polysilicon resistors of small resistance [3, pp. 88, 131], as shown in Fig. 3.

Figure 3
Polysilicon Capacitor for Integration with a SET

With the possibility of constructing capacitors jointly with resistors and voltage-variable nonlinear negative resistance SET's we have all of the ingredients available for making very general analog circuits. Because of the present interest in neural networks, we propose the circuit of the next section as a possible NTL [4].

A SOLITARY WAVE TYPE CIRCUIT

Figure 4 shows a cascade of identical R-C-SET sections which is intended to serve as a line to propagate solitary wave pulses, for example, neural-type pulses. The philosophy of operation is as follows.

When there is no input all of the gate and drain voltages are at zero, the capacitors have the bias voltage, V_{DD}, across them and no current flows. This shows that for no excitation the circuit dissipates no power. When a positively going voltage pulse, v_1, arrives at the input the gate voltage of the first SET rises causing current to flow up into the first capacitor and, consequently, raising the first drain voltage with time. When the drain voltage rises sufficiently it causes the current in C to reverse in which case the voltage on the drain decreases, it falling all the way back to zero as the pulse passes. With appropriate matching of the system parameters (R, C, and SET characteristics) with the pulse characteristics the pulse will propagate to the right with a constant velocity and without attenuation. Because of the shape of the nonlinearity, it should be possible to match to a neural type of pulse.

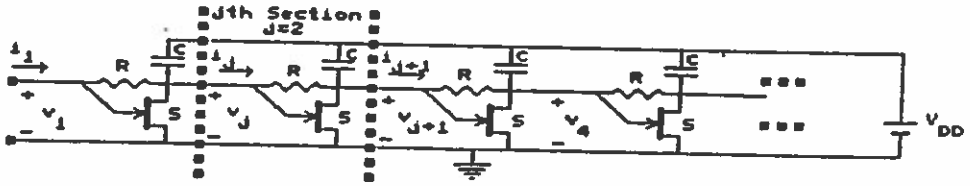

Figure 4
R-C-SET Cascade

In Fig. 4 we have isolated one section of the cascade. Considering it and equations (1) we can describe the jth section by the following admittance type of description (where · means differentiation).

$$i_j = i_g(v_j, v_{j+1}) + G(v_j - v_{j+1}) \qquad (3a)$$

$$-i_{j+1} = i_g(v_j, v_{j+1}) + G(v_{j+1} - v_j) + C\dot{v}_{j+1} \qquad (3b)$$

In order to solve these equations one would like to find v_{j+1} from (3a) to substitute into (3b) and then solve the differential equation in v_j. However, generally there is a multivalued solution for v_{j+1} of (3a) leading to hysteresis (as one expects to find in a NTL [5]). Consequently, practical solutions depend upon parasitics and require somewhat sophisticated techniques for which the semistate formulation [6] is most appropriate.

introduced into the circuits, resistors having previously been so incorporated. Because the characteristics of the SET show a voltage variable negative output resistance, the SET can be used to insert energy in lines propagating signals, as NTL's. Other types of such lines of interest are the Toda lattices [7] and others propagating solitons [8] and, thus, the SET should prove valuable for the design of VLSI soliton circuits. But because negative resistance characteristics are useful for the design of oscillators, and especially Van der Pol oscillators [9], investigation of their use in the design of VLSI oscillators is well warranted.

Besides the upward mode SET which we have discussed here there is also a downward mode SET, this latter having the drain and source reversed from the upward mode one. Experimentally it is found [1] that the curves for the downward SET are not as sharp as those for the upward mode one in which case the downward SET should also find its niche in VLSI analog signal processing.

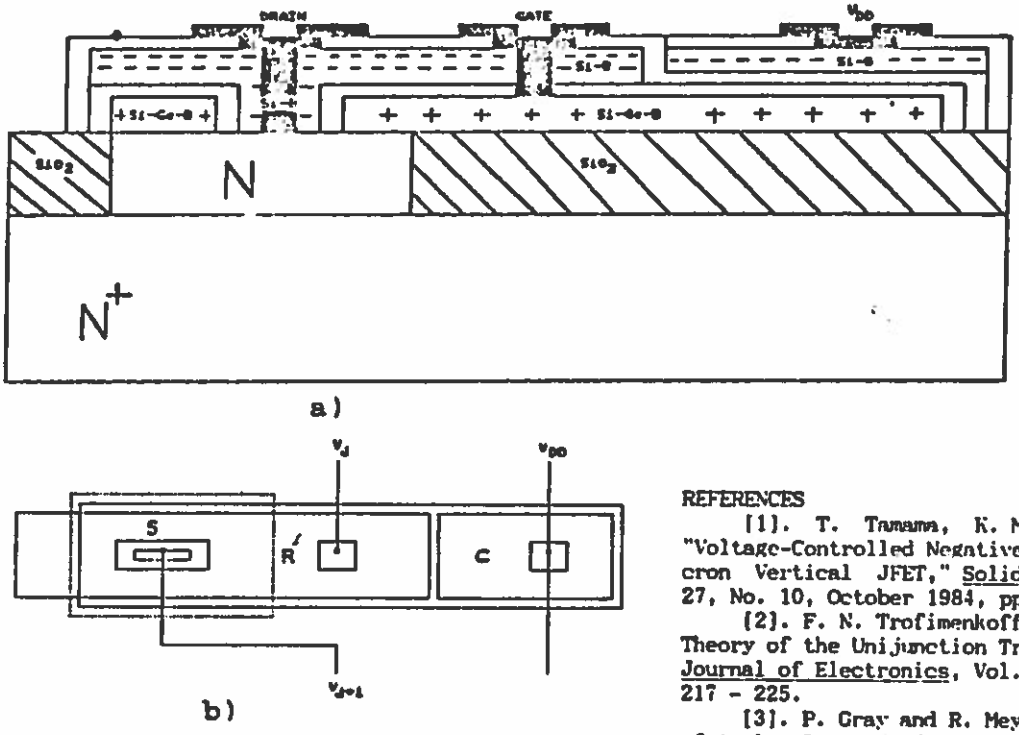

Figure 5
IC Layout for the R-C-SET Cascade
a) Side View b) Top View

In Fig. 5 we show a possible layout for one section of the circuit of Fig. 4. In Fig. 5 the capacitor is located on the right and the resistor is the upper Si-B material between the drain and the gate. We see that this circuit can conveniently be fabricated in VLSI form.

DISCUSSION

Here we have introduced the SET as a potentially very valuable device for VLSI analog signal processing. To go along with this a polysilicon capacitor is proposed such that dynamics can be

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