MTNS, Phoenix June 1987

313

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# Semistate Description of an MOS Neural-Type Cell*

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Abstract:

This paper sets up the canonical semistate description for a neural-type cell (NTC) MOS circuit. The circuit is very nonlinear and is considered as the interconnection of three subcircuits including the incorporation of a feedback transistor which greatly enhances the cell's performance. Canonical semistate equations are obtained and show that the system with the feedback transistor present exhibits hysteresis, thus, giving the necessity of using semistate equations. A practical numerical example verifies the theory.

## I. Introduction

Since the time of the introduction of the neuristor by Crane [1] there has been considerable interest in neural-type electronics [2] because of the possibility of yielding new types of computers based upon the principles of biological neural systems. If suitable electronic circuits could be found for integrated circuit realization then considerable promise would exist for the field since, for example, neuroscientists are presently obtaining good maps of neural connections pertinent to specific functions, such as the control of swimming in the leech [3]. Although at the time of publication of Crane's paper the main circuits available for these constructions were based upon tunnel diodes, and, hence, impractical for large scale implementations, much better circuits have been developed over the years [4]. Here we look at one of these circuits [2, Fig. 2], a neural-type cell (NTC) which holds considerable promise.

As we will see, the operation of this circuit critically depends upon hysteresis generated through feedback. Consequently, conventional state-space analysis does not work to describe the circuit and it is necessary to turn to other theories. In particular semistate theory, which is known to handle some types of hysteresis, is ideally suited for covering this NTC.

Before proceeding to the circuit analysis we comment that neural-type systems (NTS's) are constructed as interconnections of neural-type cells (NTC's), neural-type junctions (NTJ's) and neural-type lines (NTL's). In a companion paper [5] we set up the semistate equations for a particular NTJ so that the NTC's and NTJ's may be analyzed in a consistent semistate framework. It is also to be noted that the NTS theory under discussion here is somewhat different than that of neural optimization networks [6] which recently has gained some press coverage [7]. The latter is based upon Morshita types of interconnections [8] using essentially classical circuitry.

## II. The NTC

Figure 1 shows the MOS NTC under discussion. In Fig. 1 there are two n-channel MOS transistors, $Q_1$ & $Q_3$, and a p-channel one, $Q_2$. The input $u=v_1$ is applied to $Q_1$ which gives the threshold and develops a signal across $Q_2$, via the voltage on $R_4$, which controls in a very nonlinear way the charging of the pulse shaping $R_4$-C combination. The output is $v_3$ which is devloped by the drain current of $Q_2$ in $R_5$; this output is internally fed back via $Q_3$ as a current in $R_4$ to control the action of $Q_2$. This feedback gives some of the most useful information processing properties of the NTC since it allows for pulse repetition rate modulation of the neural-type pulses developed by the $Q_1$-$Q_2$ pair.

For obtaining the semistate equations the circuit of Fig. 1 is conveniently broken into a connection at points a, b, c, of three subcircuits, with the subcircuits given in Fig. 2. Thus, we will obtain the semistate equations of the three subcircuits and then apply the interconnection laws to obtain the semistate equations of Fig. 1. In doing this we need the description of an MOS transistor for which we assume that the gate current, $i_g$, is zero, and take the drain current, $i_d$, to be a nonlinear function $f(.,.)$ of the gate-to-source voltage, $v_{gs}$, and the drain-to-source voltage, $v_{ds}$; thus

$$i_g = 0 \tag{1a}$$
$$i_d = f(v_{gs}, v_{ds}) \tag{1b}$$

Later we will call upon specific $f(.,.)$ but here point out that by proper sign choices in the variables we can assume the same functional form for the law of the n- and p-channel devices. Thus, we use $f_i$ to designate the $f$ for the $i$th transistor. Similarly we will index according to the $i$th subcircuit the quantities in the canonical semistate equations

$$\mathcal{D}\dot{X} + \mathcal{R}(X) = \mathcal{B}U \tag{2a}$$
$$Y = \mathcal{L}X \tag{2b}$$

Here $\mathcal{D}$, $\mathcal{B}$, and $\mathcal{L}$ are constant matrices and $\mathcal{R}(.)$ is a nonlinear vector valued function; $U$ is the subcircuit input vector, $Y$ the subcircuit output vector, and $X$ the subcircuit semistate vector.

For the input stage, Fig. 2a), we can write by inspection

$$v_1 = u = U_{11} \tag{3a}$$
$$G_4(V_{dd}-v_2) - f_1(v_1, v_2) = i_3 = U_{12} \tag{3b}$$

Here resistor $R_4$ is assumed to be linear of (constant) conductance $G_4$. Since the input stage has no dynamics the canonical semistate equations become

$$\mathcal{R}_1(X_1) = \mathcal{B}_1 U_1 \tag{3c}$$
$$Y_1 = \mathcal{L}_1 X_1 \tag{3d}$$

where, using a superscript T to designate the transpose,

$$X_1^T = [v_1, v_2] = [X_{11}, X_{12}] \tag{3e}$$
$$U_1^T = [v_1, i_3] = [U_{11}, U_{12}] \tag{3f}$$
$$Y_1 = v_2 \tag{3g}$$

Thus, when (3a,b) are written in the canonical form (3c,d) they are

$$\begin{bmatrix}1 & 0\\ 0 & -G_4\end{bmatrix}\dot{X}_3 + \begin{bmatrix}0\\ G_4V_{dd}-f_1(X_{11},X_{12})\end{bmatrix} = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}u\\ U_{12}\end{bmatrix} \quad (3h)$$

$$Y_1 = [0,\ 1]X_3 \quad (3i)$$

For the output stage, Fig. 2b), we can similarly proceed to get

$$\mathcal{C}_2\dot{X}_2 + \mathcal{G}_2(X_2) = \mathcal{B}_2U_2 \quad (4a)$$

$$y = \mathcal{L}_2X_2 \quad (4b)$$

with

$$X_2^T = [i_2,\ v_2,\ v_3,\ v_4] = [X_{21},\ X_{22},\ X_{23},\ X_{24}] \quad (4c)$$

$$U_2 = v_2 \quad (4d)$$

Written in full these are

$$\begin{bmatrix}0 & 0 & 0 & C\\ 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\\ 0 & 0 & 0 & 0\end{bmatrix}\dot{X}_2 + \begin{bmatrix}1 & 0 & 0 & G_6\\ -1 & 0 & 0 & 0\\ -1 & 0 & G_5 & 0\\ 0 & 1 & 0 & 0\end{bmatrix}X_2 + \begin{bmatrix}-G_6V_{dd}\\ f_2(X_{24}-X_{22},X_{24}-X_{23})\\ 0\\ 0\end{bmatrix} = \begin{bmatrix}0\\ 0\\ 0\\ 1\end{bmatrix}U_2 \quad (4e)$$

$$y = [0,\ 0,\ 1,\ 0]X_2 \quad (4f)$$

And for the feedback stage, Fig. 2c),

$$\mathcal{G}_3(X_3) = \mathcal{B}_3U_3 \quad (5a)$$

$$Y_3 = \mathcal{L}_3X_3 \quad (5b)$$

with

$$X_3^T = [i_3,\ v_2,\ v_3] = [X_{31},\ X_{32},\ X_{33}] \quad (5c)$$

$$U_3^T = [v_3,\ v_2] = [U_{31},\ U_{32}] \quad (5d)$$

$$Y_3 = i_3 \quad (5e)$$

which when written out in full are

$$\begin{bmatrix}0 & 1 & 0\\ 0 & 0 & 1\\ 1 & 0 & 0\end{bmatrix}\dot{X}_3 + \begin{bmatrix}0\\ 0\\ -f_3(X_{33},X_{32})\end{bmatrix} = \begin{bmatrix}0 & 1\\ 1 & 0\\ 0 & 0\end{bmatrix}U_3 \quad (5f)$$

$$Y_3 = [1,\ 0,\ 0]X_3 \quad (5g)$$

The full system semistate equations are found by using the connection constraints, these being

$$U_2 = Y_1 \ (=v_2) \quad (6a)$$

$$U_{12} = Y_3 \ (=i_3) \quad (6b)$$

$$U_{31} = y \ (=v_3) \quad (6c)$$

$$U_{32} = Y_1 \ (=v_2) \quad (6d)$$

Defining the (preliminary) full semistate as

$$X_p^T = [X_1^T,\ X_2^T,\ X_3^T] \tag{7a}$$

we obtain, using (6),

$$\begin{bmatrix} 0 & 0 & 0 \\ 0 & \beta_2 & 0 \\ 0 & 0 & 0 \end{bmatrix} \dot{X}_p + \begin{bmatrix} f_1(X_1) - \beta_{12} x_3 X_3 \\ f_2(X_2) - \beta_{21} x_1 X_1 \\ f_3(X_3) - \beta_{32} x_1 X_1 - \beta_{31} x_2 X_2 \end{bmatrix} = \begin{bmatrix} \beta_{11} \\ 0 \\ 0 \end{bmatrix} u \tag{7b}$$

$$y = [0,\ x_2,\ 0]X_p \tag{7c}$$

In obtaining (7) we note that the feedback is internal, that is, $Y_3$ is only a part of $U_1$. Likewise we note that a number of the semistate variables are actually the same quantities. Thus,

$$X_{12} = X_{22} = X_{32} = v_2 \tag{8a}$$

$$X_{23} = X_{33} = v_3 \tag{8b}$$

in which case there are three identical equations among the algebraic portion of (7b). Now (7b) is a set of 9 equations which we reduce to 6 by eliminating these three equations, the 6th through 8th equations. Doing this we finally come to the basic canonical semistate equations

$$X^T = [v_1,\ v_2,\ i_2,\ v_3,\ v_4,\ i_3] = [X_1, X_2, X_3, X_4, X_5, X_6] \tag{9a}$$

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \dot{X} + \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & G_4 & 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & G_6 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & G_5 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} X + \begin{bmatrix} 0 \\ f_1(X_1, X_2) - G_4 V_{dd} \\ -G_4 V_{dd} \\ f_2(X_3 - X_2, X_5 - X_4) \\ 0 \\ -f_3(X_4, X_5) \end{bmatrix} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} u \tag{9b}$$

$$y = [0,\ 0,\ 0,\ 1,\ 0,\ 0]X \tag{9c}$$

It should be observed that these equations can be written almost by inspection of the NTC. However, the method used above of connecting the various subsystems is universally applicable and represents more the philosophy of design. By eliminating $v_3$, $i_3$, a four dimensional set of canonical semistate equations can be obtained and by further eliminating $v_1$ and using $R_4 = 1/G_4$ & $R_5 = i/G_5$ with

$$X_r = [v_4,\ v_2,\ i_2] \tag{10a}$$

these canonical equations can be written in the reduced (but noncanonical) form

$$\begin{bmatrix} C & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \dot{X}_r + \begin{bmatrix} G_4 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} X_r = \begin{bmatrix} G_4 V_{dd} \\ V_{dd} - R_4 \{ f_1(u, v_2) + f_3(R_5 i_2, v_2) \} \\ f_2(v_4 - v_2, v_4 - R_5 i_2) \end{bmatrix} \tag{10b}$$

$$y = [0,\ 0,\ R_5]X_r \tag{10c}$$

If it were possible to obtain state-variable equations these would be found by eliminating $v_2$ & $i_2$ from the second and third rows of (10b) and substituting the $i_2=F(v_4,u)$ so found into the first row. Then we would obtain

$$\dot{C}v_4 + G_4v_4 = G_4V_{dd} - F(v_4,u) \qquad (11)$$

However, as we discuss in the next section, elimination to a single valued function $F(.,u)$ is not generally possible when $f_3(.,.)\neq 0$, since hysteresis can be obtained.

Nevertheless, if the feedback transistor is absent then $f_3=0$ and $X_4=i_3=0$ can be set allowing the second row of (10b) normally to be solved for $v_2$ which in turn allows $i_2$ of the third row to be determined as a single-valued $F(v_4,u)$.

III. Hysteresis in the NTC

In order to investigate the nature of responses of the NTC we need a description of the transistors, that is the $f(.,.)$ of (1b). For this we use the standard description [9, p. 51] which is

$$f(x,y) = \begin{cases} 0 & 0\geq x-V_T \quad \text{(off)} \\ \beta[2(x-V_T)y - y^2] & 0\leq x-V_T\geq y \quad \text{(ohmic)} \\ \beta(x-V_T)^2 & 0\leq x-V_T\leq y \quad \text{(saturation)} \end{cases} \qquad (12)$$

where the threshold voltage, $V_T$, and the gain parameter, $\beta$, are process dependent (these two parameters having subscripts 1, 2, 3 corresponding to which transistor they belong).

Now we investigate the $F(.,u)$ which can be done by removing the C-$R_4$ combination from the circuit and monitoring $i_2=X_3$, the $Q_2$ drain current, as a function of voltage $v_4=X_5$ and input u. To get a feeling for the result we discuss the transistor behaviors as $v_4$ is increased from 0 to $V_{dd}$. For small $v_4$ $Q_2$ and $Q_3$ will be off, and, hence, $i_2=0$. Assuming that the input is large enough to turn on $Q_1$, then increasing $v_4$ will eventually turn on $Q_2$ which will first be in the saturation region since $v_3$ starts at 0. As $i_2$ increases with $v_4$ it will eventually turn on $Q_3$ which also starts in the saturation region. The turning on of $Q_3$ can lead to hysteresis since, now monitoring $v_4$ as a function of $i_2$, we find that $v_4$ can, by a proper choice of circuit elements, increase and then decrease with increasing $i_2$. Eventually $i_2$ will be large enough to bring both $Q_2$ & $Q_3$ into the ohmic region with the voltage on the drain to source of $Q_2$ falling to 0, this latter leads to $i_2$ versus $v_4$ determined solely by $R_3$ as a straight line with slope $G_3$. Thus, the interesting region to consider is that covering $Q_3$ from where it turns on until it becomes saturated.

To consider some mathematical details, we assume the practical case of equal (complementary p and n) transistors; then while $Q_3$ is saturated, $Q_2$ is also saturated, since $v_3-V_{T3}\leq v_2$ for $Q_3$ implies $v_4-v_2-V_{T2}\leq v_4-v_3$ for $Q_2$ . Thus,

$$i_2 = \beta_2(v_4-v_2-V_{T2})^2 \qquad (13a)$$

in which $v_2=v_2(i_2,u)$ is a decreasing function of both u and $i_2$

(decreasing since $i_1$ and $i_3$ increase with increasing $u=v_1$ and $v_3=R_3 i_2$, respectively). When solved for $v_4$ (13a) is

$$v_4 = V_{T2} + v_2(i_2,u) + (i_2/\beta_2)^{1/2} \qquad (13b)$$

(here the + sign on the root must be used since $Q_2$ is not off). For certain choices of parameters we can make the square root first dominate and then eventually have $v_2$ decrease much faster with $i_2$ than the square root increases, thus giving the hysteresis. To see this more specifically we next look at the dependence of $v_2$ on $i_2$. Since this depends on the state of $Q_1$ there are two cases to consider:

$Q_1$ saturated: $v_2 = V_{dd}-R_4\{\beta_1(u-V_{T1})^2+\beta_3(R_3 i_2-V_{T3})^2\}$ (13c)
$Q_1$ ohmic: $v_2 = V_{dd}-R_4\{\beta_1[2(u-V_{T1})v_2-v_2^2]+\beta_3(R_3 i_2-V_{T3})^2\}$ (13d)

To find the peak of the $v_4$ versus $i_2$ curve we differentiate (13b) and use (13c or d). Thus,

$$dv_4/di_2 = -2R_4R_3\beta_3(R_3 i_2-V_{T3}) + 1/(\beta_2 i_2)^{1/2} \qquad (Q_1 \text{ sat}) \qquad (14a)$$

$$= \frac{-2R_4R_3\beta_3(R_3 i_2-V_{T3})}{1 + 2R_4\beta_1[(u-V_{T1})-v_2]} + 1/(\beta_2 i_2)^{1/2} \qquad (Q_1 \text{ ohm}) \qquad (14b)$$

Clearly these derivative can be zero since they are positive for small $i_2$, where the square root term dominates, and negative for large $i_2$, where the first term dominates (this is for $\beta_3\neq 0$, that is, if feedback is present; otherwise we do note that if $\beta_3=0$ then no hysteresis will be present as $v_4$ will always increase with $i_2$ in (13b)). To obtain hysteresis we desire the derivative of (14) to be zero in the region where $Q_3$ is saturated. Thus, we next determine the values of $i_2$ for which $Q_3$ is saturated.

We have that $Q_3$ turns on when

$$i_2 = I_{2a} = G_3 V_{T3} \qquad (15a)$$

and it turns ohmic at

$$i_2 = G_3(V_{T3}+v_2(i_2,u)) \qquad (15b)$$

Since this is dependent upon $v_2$ there are the two cases of (13c,d) to again be considered. In the $Q_1$ saturated case (13c) is substituted directly into (15b) which is in turn solved for $i_2$ while in the $Q_1$ ohmic case (13d) is first solved for $v_2$ in terms of $i_2$ and then substituted into (15b), which again is solved for $i_2$. The resulting $i_2$ we call $I_{2b}$, which is the value of $i_2$ when $Q_3$ leaves the saturated state as $i_2$ increases.

For $Q_1$ saturated we find

$$I_{2b\,sat} = I_{2a} + G_3\{\frac{1}{R_4\beta_3}(V_{dd}-R_4\beta_1(u-V_{T1})^2-(u-V_{T1}))\}^{1/2} \qquad (15c)$$

while for $Q_1$ ohmic we find, in the practical case of $Q_1=Q_3$

$$I_{2\text{ohm}} = I_{2a} + G_5\left(\frac{V_{dd}}{2R_4\beta_1(u-V_{T1}+(1/[2(R_4\beta_1)]))}\right) \qquad (15d)$$

The situation is best seen through an example.

IV. An Example

We consider the NTC of Fig. 1 with the following choice of parameters

$$R_4=R_5=2k\Omega,\ R_6=3k\Omega,\ C=50pf,\ V_{dd}=10v,\ u=4.5v \qquad (16a,b,c,d,e,f)$$
$$\beta_1=\beta_2=\beta_3=0.00063 \quad V_{T1}=V_{T2}=V_{T3}=2v \qquad (16g,h,i,j,k,l)$$

in which the transistor parameters are chosen to go with the MC4007 package. After some extensive calculations, much aided by MATHCAD, Fig. 3 is obtained which shows the curve of $i_2$ (multiplied by $R_5$) versus $v_4$ when the $R_6$-C combination is removed. For this case $Q_1$ remains in the ohmic region, in which case (15d) is used. As is seen, a multivalued curve results; this gives hysteresis in the physical circuit since parasitic capacitors force jumps between the upper and lower branches at their endpoints (for which the voltages $v_4$ are 5.0053 and 5.5147 with currents $i_2$ of 1.685ma and 1.106ma, respectively). The full circuit of Fig. 1 operates with a load line determined by

$$i_2 = G_6(V_{dd}-v_4) \qquad (17)$$

which is also plotted versus $v_4$ in Fig. 3 (likwise multiplied by $R_5$). The load line shown has been chosen to intersect the vertical jump lines of the hysteresis so that oscillatory neural-type pulses will result. To further verify this result, the circuit was run on MICROCAP using the above values with the MICROCAP run shown in Fig. 4. In Fig. 4 signals of all the nodes of Fig. 1 are monitored and it is seen that the lowest curve which is the voltage of node 3, the output node, is a repetition of neural-type pulses.

It should be noted that the hysteresis varies with the input u. For too large or too small u only a single output pulse results, whereas, when oscillatory pulses result the repetition rate is controlled by u. For the numerical values of this example we found these lower and upper limits for u were about 4 and 5 volts, respectively. And, as seen by Fig. 3, there is only a small range over which $R_6$ may vary and still intersect only the vertical sides of the hysteresis. Thus, the future use of the circuit entails the availability of good design tools to be able to design with this hysteresis.

V. Discussion

The circuit presented, a neural-type cell (NTC), shows the need for good semistate design techniques as well as for good solution techniques. As is seen by equations (10) the circuit is described by a three dimensional semistate system which is designed to be quite nonlinear with feedback inserted to obtain coding of input pulse amplitude into output neural-type pulse repetition rate. Through the semistate equations we hope to learn enough about the design parameters for the hysteresis presented such that we can design for prescribed neural-type pulse repetition rates, thus allowing for the coding of neural-type pulses in a manner similar to that in biological neural systems.

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* Research supported in part by NSF Grant ECS-85-06924.

Figure Titles

1. MOS Neural-Type Cell
2. NTC Subsystems
   a) Input stage
   b) Output Stage
   c) Feedback Stage
3. $i_2$ versus $v_4$ Showing Hysteresis
4. NTC Time-Domain Signals

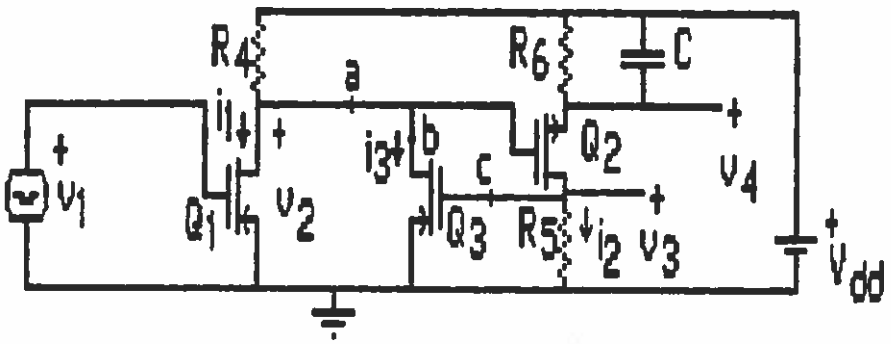
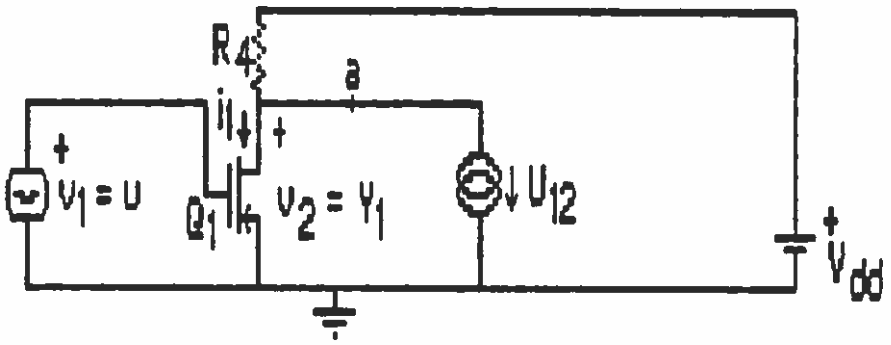
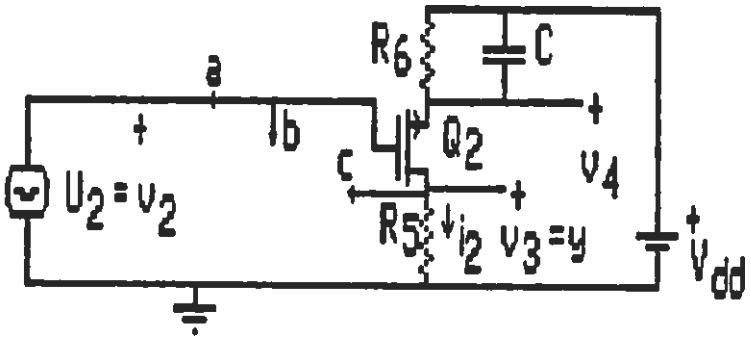



Figure 1
MOS Neural Type Cell




2a)

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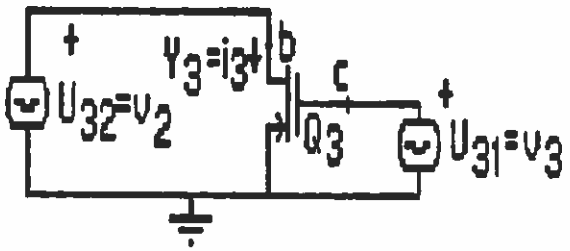


2c)

Figure 2
NTC Subsystems

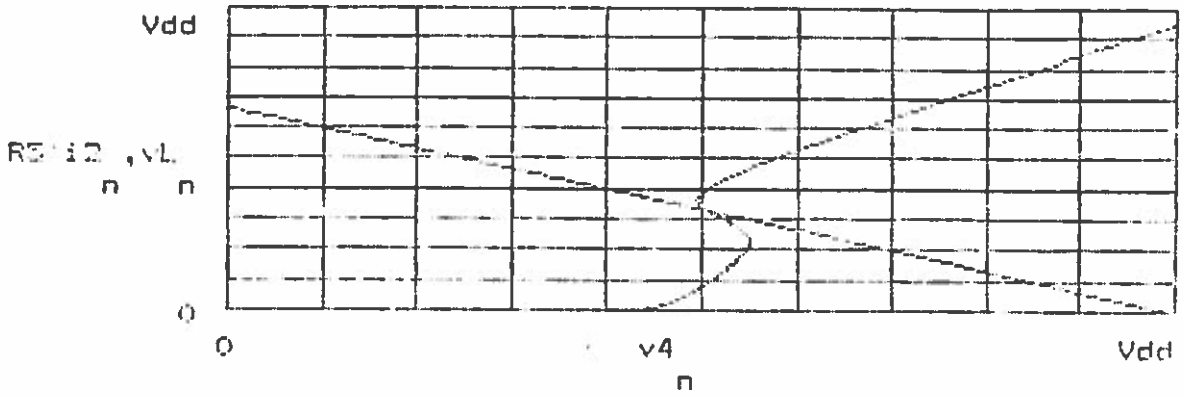


Figure 3
$i_2$ versus $v_4$

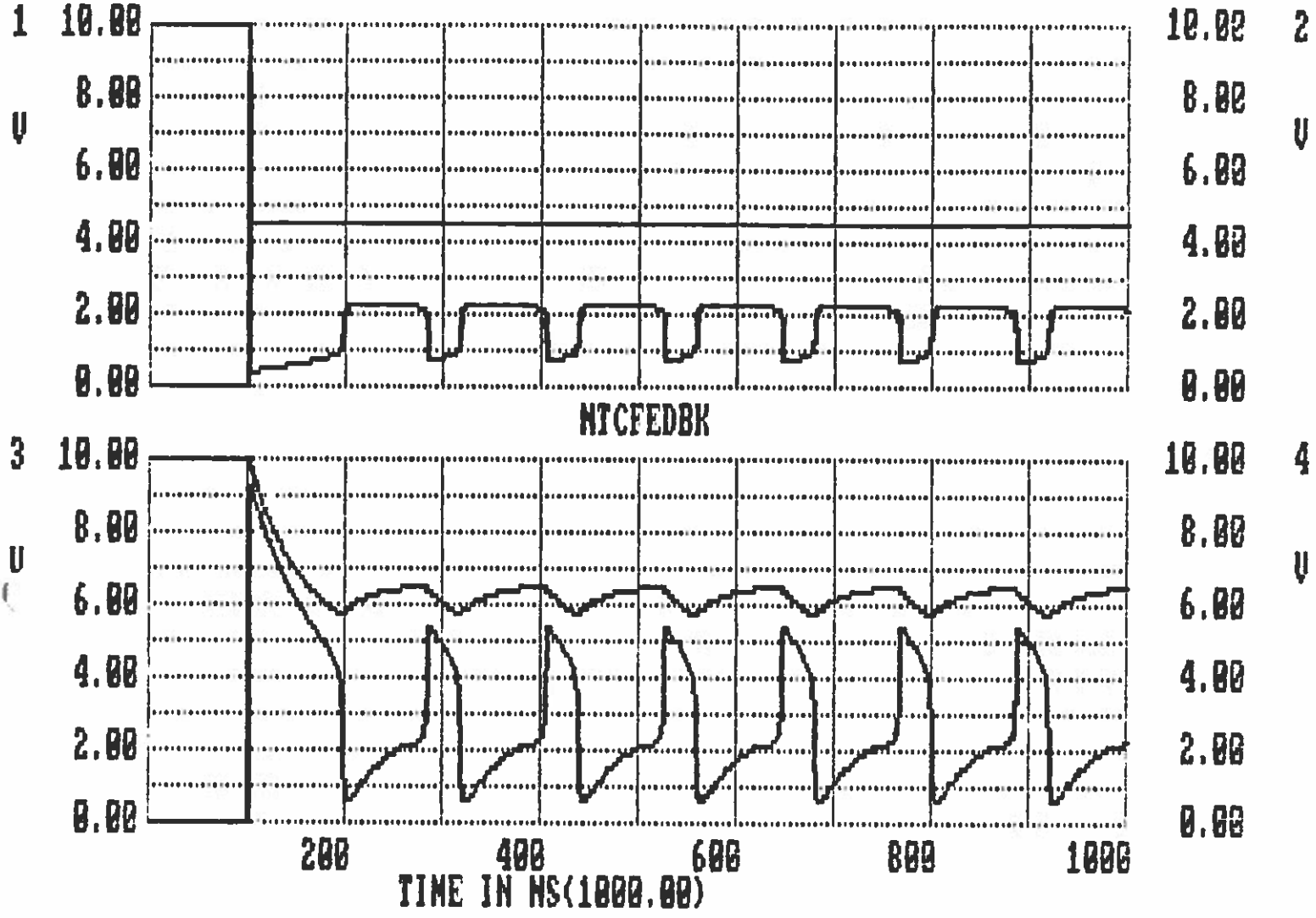


Figure 4
NTC Time Domain Signals