Multilevel Neural-Type Lattices*

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Abstract
A multilevel neural-type logic lattice is introduced following the original description of Toda. Electronic circuits for this Toda lattice are developed and CAD results presented on the soliton type of pulses it handles. Circuits are also discussed for realizing a modification of the previously introduced neural-type logic lattices.

I. Introduction

Previously multilevel neural-type logic lattices were introduced which work on the soliton principle [1]. In these information is carried on pulses that travel in the system with pulses of different heights traveling at different velocities and not interfering with each other. Electronic circuit realizations of the circuits of [1] require analog multipliers, which though possible for construction in integrated circuit form, are somewhat inconvenient. Consequently, we look here at another class of solitons [2], those from which the equations in [1] are actually transformed. These more fundamental equations have for thier nonlinearity an exponential, rather than a product, and as such should be more amenable to integrated circuit constructions since one can realize the exponentials via solid-state diodes.

II. The Basic System

The basic theory for our circuits is found in [2], an early paper (1967) by Toda where he first presents what has come to be known as the Toda lattice [3, Chap. 7]. In [2] Toda considers a uniform chain of particles with an exponential interaciton energy between adjacent particles. Put into state-variable form his equations (2.10) and (3.3) are, respectively,

$$m\dot{r}_n/dt = 2s_n - s_{n-1} - s_{n+1} \quad (1a)$$

$$\dot{s}_n/dt = -a\{1-\exp(-br_n)\} \quad (1b)$$

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Here a, b, m are positive constants. With normalized mass, m=1, and driven by intial conditions, these are shown to have the solutions (equations (3.12) & (3.6) of [2])

$$r_n = (-1/b)\cdot \ln(1+(2K\nu)^2[dn^2\{2K(\nu t+(n/\lambda))\}-(E/K)]/ab) \quad (2a)$$

$$s_n = (2kb/\nu)Z\{2K(\nu t+(n/\lambda))\} \quad (2b)$$

where

$$2K\nu=[ab/\{(sn^2(2K/\lambda))^{-1}-1+(E/K)\}]^{1/2} \quad (2c)$$

and sn, dn and Z are Jacobian elliptic functions, which, along with K, are functions of the modulus k and tabulated in terms of $m=k^2$ [4]. There are actually two solutions, a right traveling one and a left traveling one; we have arbitrarily chosen the left traveling one and obtain circuit realizations for it.

Of interest to us is the fact that the exponential term in (1b) is similar to the solid-state diode characterization [5, p. 142]

$$i = -I_s\{1-\exp(v/V_T)\} \quad (3)$$

where the saturation current, I_s, and the thermal voltage, V_T, are constants dependent upon temperature. Thus, the Toda lattice of equations (1) should have a nice realization in terms of electronic circuits where the nonlinearity is obtained simply through the use of diodes. However, in realizing (1b) via an integration one runs into a difficulty in that the charge on the integrator simply accumulates due to the diode rectification action. Consequently, it is expeditious to introduce a new difference variable

$$y_n = s_n - s_{n-1} \quad (4a)$$

Equations (1) are then rewritten as

$$m\dot{r}_n/dt = y_n - y_{n+1} \quad (4b)$$

$$\dot{y}_n/dt = -a\{1-\exp(-br_n)\}+a\{1-\exp(-br_{n-1})\} \quad (4c)$$

We do note that we could have chosen s_{n+1} as the second term in defining y_n; this has the effect of changing left going pulses into right going ones.

Toward an actual realization we first perform some normalizations. For this we multiply (4b) by α, (4c) by β, and let $s=d/dt$ to get

$$\alpha r_n = -(\alpha/m\beta s)[\beta y_{n+1} - \beta y_n] \quad (5a)$$

$$\beta y_n = -(a\beta/s)[(\exp(-(b/\alpha)(\alpha r_{n-1}))-1) - (\exp(-(b/\alpha)(\alpha r_n)-1)] \quad (5b)$$

It is, therefore, convenient to let

$$R_n = \alpha r_n \quad (5c)$$

$$Y_n = \beta y_n \quad (5d)$$

Realizing the exponentials via the diodes of (3), Fig. 1A) shows a circuit realization of the nth lattice section of this Toda lattice where we see that

$$V_T = \alpha/b \quad (6a)$$

$$C_r R = m\beta/\alpha \quad (6b)$$

$$C_v = I_s/a\beta \quad (6c)$$

Figure 1B) is identical to Fig. 1A) except that two isolation amplifiers are introduced to break some loops that could change the characteristics of the circuit. However, we found very little difference in performance between the two types of sections, and, hence, used Fig. 1A) for the simulations presented below. We then can make the following choices

$$a=b=m=1,\ I_s=1E-14,\ V_T=0.025 \quad (7a)$$

$$R=1E6,\ C_v=1E-10,\ C_r=4E-8 \quad (7b)$$

which give $\alpha=V_T$, $\beta=1E-4$. Here we have chosen $V_T=(1E-2)/4$ for numerical convenience.

Using these values a cyclic three section system was simulated using MICROCAP on an IBM PC, the circuit diagram being as shown in Fig. 2a); Fig. 2b) contains a NETLIST of node numberings for the connections. For this cyclic connection the mth and nth lattice sections are related by

$$n \equiv m \ \mathrm{Mod}(3) \quad (8)$$

while the problem of loading is avoided since each section sees another to its right and left. However, since MICROCAP would not proceed with this circuit excited by other than zero initial conditions, it was necessary to insert an external source, this being inserted on the right to charge C_v to give a positive Y_3. The pulse chosen is listed as V(t) in the NETLIST (item 44). Two different peak values were chosen to show the speedup of higher amplitude pulses. Among the effects of this external source is to put a bias on Y_n in which case a very short pulse was used so that the circuit responses are not unduly disturbed; but a theoretical analysis remains to be made on its mathematical effects. Indeed it is not clear yet as to how the resulting pulses are related to the soliton solutions given above in terms of Jacobian elliptic functions.

Refering to Fig. 1 the operation of a section can be described as follows. Consider that at a given instant Y_n is positive. This tends to make R_{n-1} negative, via the presence of Y_n on the (n-1)st section C_r integrator, which in turn forward biases the left hand nth section diode causing Y_n to decrease. R_{n-1} negative also forward biases the right hand diode of the (n-1)st section causing Y_{n-1} to go positive in which case the pulse travels to the left. The larger Y_n is the faster the (n-1)st section C_r accumulates charge causing Y_n to decrease faster (via the left hand nth section diode), in which case the pulse travels faster. At this point we can also see the effect of the alternate choice for y_n [made by choosing s_{n+1} as the second term on the right of (4a)]; a circuit based on this choice in essence reverses the right and left sides of Fig. 1, or with the labeling of Fig. 1 has pulses traveling to the right.

Typical results of the simulation are shown in Fig. 3, where the pulse shaping and propagating properties are shown. The signals Y_1, Y_2, Y_3, input pulse v(t), R_1, R_2, R_3, and diode voltage $v_{2\bullet}$ are shown in the figure for two different peak values of the input pulse (14 & 8 volts respectively). One sees that in time sequence Y_3 first forms and then it transfers to Y_2 and then to Y_1. Comparing the upper four portions of the figure with the lower four portions one sees that there is a higher velocity of propagation with the higher peaked pulses. Unfortunately, MICROCAP does not allow us to extend the response much further in time so in the future it is necessary to either simulate with a more substantial program or, better yet, to build the circuit and make real time measurements.

Once having established the feasibility of this Toda lattice realization it is next important to obtain simplified circuits. Toward that we note the very nice differential pair integrator presented in [6, Fig.5] which it seems could be used to simplify the integrator portions of the circuit.

III. Product Realization

In [1] the soliton implementations were proposed through the lattice equations

$$df_n/dt = b_n - b_{n+1} \quad (9a)$$

$$db_n/dt = (f_{n-1} - f_n)(b_n + 1) \quad (9b)$$

Since the last term necessitates insertion of a bias into the circuits, it may prove more useful to let

$$F_n = f_n,\ B_n = b_n + 1 \quad (9c)$$

to get the equations in the form

$$dF_n/dt = B_n - B_{n+1} \quad (10a)$$
$$dB_n/dt = B_n(F_{n-1} - F_n) \quad (10b)$$

It appears that the product of (10b) can be realized as part of the differential integrator mentioned above [6] where the current sources biasing the circuit can be made proportional to B_n, this following one of the standard ways of making multipliers [7, p.605]. Since the right hand sides of both (10a) and (10b) have difference signals to be integrated, they could then be conveniently realized by the differential integrator, though one would need to switch between appropriately level shifted structures to maintain the system bias levels.

IV. Discussion

Here we have presented a circuit for the Toda lattice in a form suitable for integrated circuit realization. To do this we have used solid-state diodes to realize the nonlinearities needed in any soliton system. However, for each section we have used two diodes where actually one should suffice, and, thus, we see that there is room for improvement in the circuits realized. For any use as logic elements in a neural-type computer it is of course important to have circuits that can be constructed conveniently in integrated circuit form because of the very large numbers of lattice sections that would be required.

It should be noted that this "Toda lattice" is not a lattice of the kind known as a lattice in the circuit theory and/or digital filtering fields, the term lattice having more the meaning of lattice in the a crystal lattice. However, these Toda lattices have been realized in the literature via the ladder structures of circuit theory [8][9]. Because of their possibility of avoiding the use of op-amps to realize the connection constraints of the Toda lattice equations, ladder structures are attractive. However, the ones in the literature are really not practical for integrated circuits since they rely on the use of inductors and the nonlinearity of junction capacitors (which in itself is not of the directly desired logarithmic form). Further, something like 46 sections are needed to develop the soliton pulses [9, p.682]. But by the use of gyrators for inductor replacement and use of diodes for the exponential nonlinearities it may be possible to obtain nice ladder structures; it is certainly worth further investigation.

One of the bigger problems still to be faced in making these structures practical is how to conveniently form the soliton pulses and how to inject them into the circuits. The means used here of injecting a short sharp pulse is convenient but it remains to see how many travels through the cyclic structure are needed until it is formed into any kind of soliton as well as how to accomodate the dc bias that it inserts into the traveling pulses.

The use of differntial integrators appears to make practical the Toda lattice realized by products, as in (10) above. This aspect of the topic area also needs to be further developed and constructions carried out.

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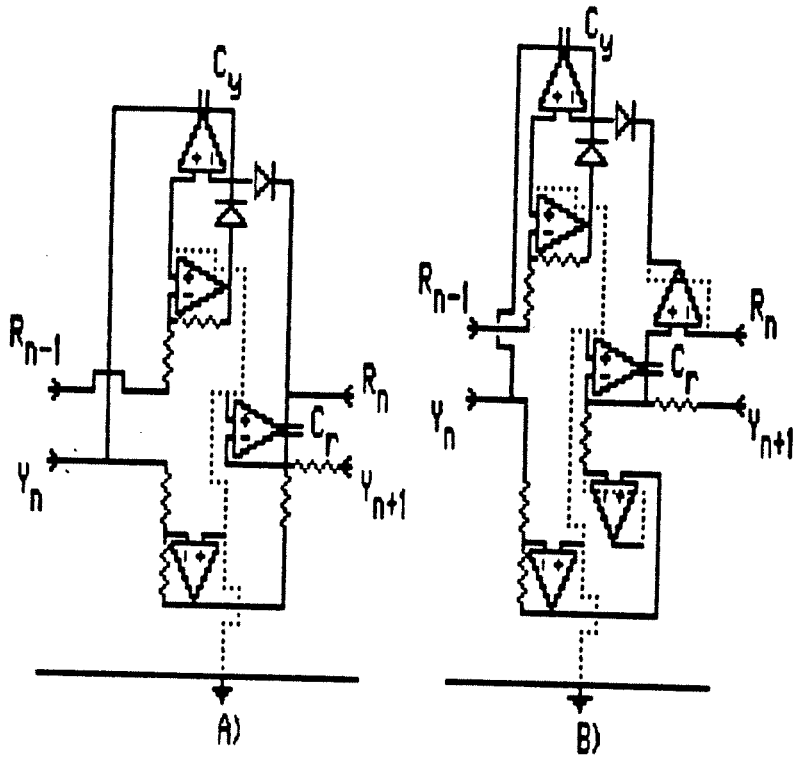

Figure 1
nth Section of Toda Lattice Circuit

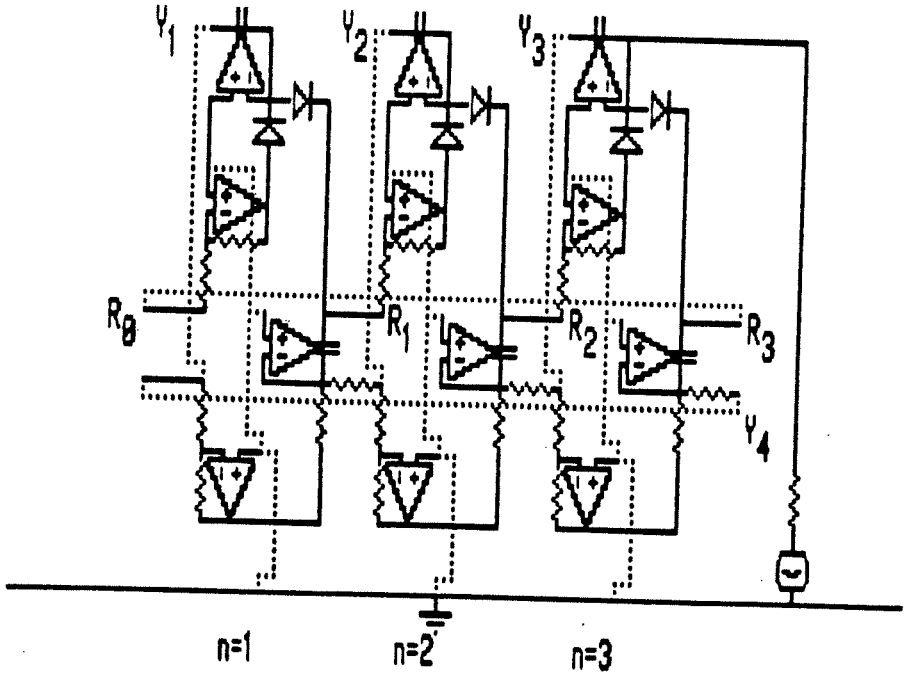

Figure 2a)
Three-Section Cyclic Connection

Figure 2b)

NETLIST

TLATST02 CIRCUIT

REF NO.	COMPONENT NAME	CONNECTIONS IN -	IN +	OUT -	OUT +	PARAMETER OR TYPE
1	CAPACITOR	9	24	0	0	1E-10
2	OPAMP	24	0	0	9	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
3	CAPACITOR	11	25	0	0	1E-10
4	OPAMP	25	0	0	11	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
5	CAPACITOR	13	8	0	0	1E-10
6	OPAMP	8	0	0	13	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
7	DIODE	16	24	0	0	6... IO= 1E-14 VZ= 200 RZ= 10 RF= 1 VT= .025 RP= 1E+07
8	DIODE	24	19	0	0	6... IO= 1E-14 VZ= 200 RZ= 10 RF= 1 VT= .025 RP= 1E+07
9	DIODE	17	25	0	0	6... IO= 1E-14 VZ= 200 RZ= 10 RF= 1 VT= .025 RP= 1E+07
10	DIODE	25	21	0	0	6... IO= 1E-14 VZ= 200 RZ= 10 RF= 1 VT= .025 RP= 1E+07
11	DIODE	15	8	0	0	6... IO= 1E-14 VZ= 200 RZ= 10 RF= 1 VT= .025 RP= 1E+07
12	DIODE	8	23	0	0	6... IO= 1E-14 VZ= 200 RZ= 10 RF= 1 VT= .025 RP= 1E+07
13	OPAMP	18	0	0	19	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
14	RESISTOR	18	19	0	0	1E6
15	RESISTOR	18	15	0	0	1E6
16	OPAMP	20	0	0	21	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
17	RESISTOR	20	21	0	0	1E6
18	RESISTOR	20	16	0	0	1E6
19	OPAMP	22	0	0	23	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
20	RESISTOR	22	23	0	0	1E6
21	RESISTOR	22	17	0	0	1E6
22	CAPACITOR	16	10	0	0	4E-8
23	OPAMP	10	0	0	16	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
24	RESISTOR	10	11	0	0	1E6
25	RESISTOR	10	1	0	0	1E6
26	CAPACITOR	17	12	0	0	4E-8
27	OPAMP	12	0	0	17	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
28	RESISTOR	12	13	0	0	1E6
29	RESISTOR	12	2	0	0	1E6
30	CAPACITOR	15	14	0	0	4E-8
31	OPAMP	14	0	0	15	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
32	RESISTOR	14	9	0	0	1E6
33	RESISTOR	14	3	0	0	1E6
34	OPAMP	5	0	0	1	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
35	RESISTOR	9	5	0	0	1E6
36	RESISTOR	5	1	0	0	1E6
37	OPAMP	6	0	0	2	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
38	RESISTOR	11	6	0	0	1E6
39	RESISTOR	6	2	0	0	1E6
40	OPAMP	7	0	0	3	6... RI= 1E+08 AO= 200000 RO= 10000 VOFF= .000001 VMAX= 30 CO= 0
41	RESISTOR	13	7	0	0	1E6
42	RESISTOR	7	3	0	0	1E6
43	RESISTOR	8	4	0	0	1E6
44	V(T)	4	0	0	0	6... P0= 0 P1= 8 P2= .0001 P3= .000101 P4= .000199 P5= .0002 P6= 1

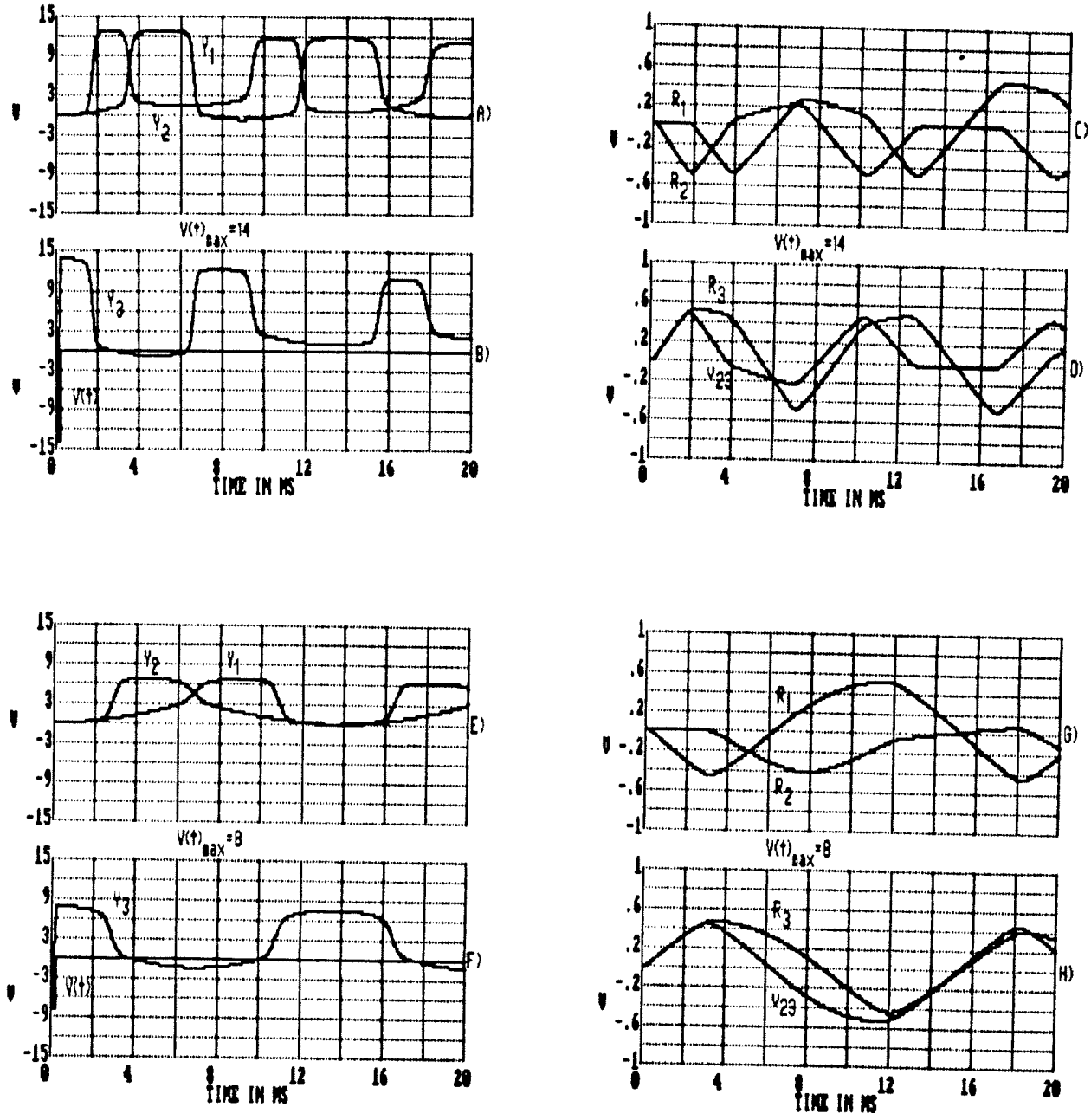

Figure 3
Typical Responses

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