Chaos Using Hysteretic Circuits*

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Abstract:
This paper will review the ongoing research in the Microsystems Laboratory in the area of analog circuits suitable for integrated circuit realization that generate chaos using hysteresis. In particular a degree two circuit using binary hysteresis [1] and a degree three circuit using bent hysteresis [2] will be covered. Some new results in the area of design of the former circuit will be covered which include analytic formulas for some parameters [3] and graphic curves for some others. The negative resistance circuit of Saito [4] will also be discussed in the same context.

References.
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[4]. T. Saito, "On a Hysteresis Chaos Generator," Proceedings of the 1985 International Symposium on Circuits and Systems, Kyoto, June 1985, pp. 847 - 849.

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