THE N-DARLINGTON STAGE: AN ACTIVE-R INTEGRATOR

Shu-Tang Liu* and Robert W. Newcomb **

*Xi'an Jiaotong University, Xi'an, Shanxi Province, The People's Republic of China
**Microsystems Laboratory, EE Dept., University of MD, College Park, MD, USA 20742

ABSTRACT

An N-Darlington stage configuration is proposed and analyzed to show that by appropriate design it can give a high gain low cut-off-frequency amplifier suitable for use as an active-R integrator. Two versions are proposed, a simplified but practical one suitable for lower frequency active-R filters and a more theroetical one which allows for much wider bandwidth filters. The design uses a special choice of parameters to give a first order transfer function with very low cut-off frequency and allows for identical transistors. A computer-aided check is carried out.

I. INTRODUCTION

Active-R circuits [1]-[4] hold considerable promise for the field of analog integrated circuits since the dynamics for active-R circuits is intrinsic to the active devices used. Thus, the internal poles of op-amps or CMOS pairs, etc., are used to realize derivatives on the state. The position of these internal poles can often be controlled by bias conditions [5] which gives some degree in flexibility for design. However, we have found that in practice this theoretically available control is very sensitive and more limited than one would like.

In order to lower the cut-off frequency of the internal pole as well as to make the theory more available to bipolar technology, we propose here the N-Darlington stage, this arising from an N-Darlington transistor, this latter being in turn a modified N-fold iteration of the normal Darlington connection [6][7]. Therefore, in theory the N-Darlington section approaches an ideal integrator as N tends to infinity and the amplifier stage parameters are properly chosen. Practically, due to approximations in the equivalent circuit used and the need to keep bias voltages within bounds, N should be somewhat restricted, to say less than ten and three or four being of most use, with the stage cut-off frequency coming into the range of tens to hundreds of Hertz, a range which, however, greatly improves the practical flexibility of active-R circuits.

The design philosophy is somewhat as follows. By the N-Darlington connection we raise the input resistance r_π as large as possible while lowering the input capacitance C_π, the product being a constant (the inverse of a lifetime). By choosing parameters properly the equivalent transistor can be kept to first order, rather than Nth order as would otherwise result. Two methods for doing this are considered, one valid for lower frequency filters and resting upon the independence of frequency effects in transistor betas in this frequency range and the other using added base to emitter resistors to compensate for beta frequency effects. Then, by embedding the equivalent transistor in a normal common emitter configuration, the dominant pole of the stage can be controlled to be small via choice of the number N and the base resistance inserted at the input to the stage.

#Research of the second author was supported in part by the US National Science Foundation under Grant ECS 83-17877.

II. THE N-DARLINGTON TRANSISTOR

We define the NPN N-Darlington transistor configuration as that shown in Fig. 1 for which we use the symbol of a normal transistor with the symbol ND. This configuration is introduced for use in the N-Darlington amplifier of Fig. 2 in order to obtain with proper design the voltage gain transfer function $K_0/(s+\omega_c)$ with ω_c low. For design of the N-Darlington amplifier we consider the small-signal design hybrid-pi equivalent circuit for each transistor T_i, i=1, ..., N including the connected conductance g_i. Since only $C_{\mu 1}$ is important of all the the $C_{\mu i}$ and since $C_{\mu 1}$ appears directly across the terminals B-C we first obtain an equivalent circuit for the N-Darlington transistor assuming $C_{\mu i} = 0$, i=1,..., N and then add $C_{\mu 1}$ at the end. Consequently we can investigate any two adjacent transitor portions of the N-Darlington transistors.

$$V_{be_i} = v_{be_i} + v_{be_{i+1}}\,,\quad I_{b_i} = i_{b_i}\,,\quad I_{c_i} = i_{c_i} + i_{c_{i+1}}$$

and $\beta_i = y_{21_i}/y_{11_i} = g_{m_i}/y_{\pi_i}$, on setting $z_{\pi_i} = 1/y_{\pi_i}$ we find

$$\frac{V_{be_i}}{I_{b_i}} = Z_{11_i} = 1/Y_{11_i} = z_{\pi_i} + z_{\pi_{i+1}}(1+\beta_i) = \left[1 + \frac{y_{\pi_i}}{y_{\pi_{i+1}}}\left(1 + \frac{g_{m_i}}{y_{\pi_i}}\right)\right]/y_{\pi_i} \qquad (1a)$$

$$\frac{I_{c_i}}{V_{be_i}} = \frac{g_{m_i} + g_{m_{i+1}}\left[\frac{y_{\pi_i}}{y_{\pi_{i+1}}}\left(1 + \frac{g_{m_i}}{y_{\pi_i}}\right)\right]}{y_{\pi_i}} = \frac{g_{m_i}}{1 + \frac{y_{\pi_i}}{y_{\pi_{i+1}}}\left(1 + \frac{g_{m_i}}{y_{\pi_i}}\right)}$$

$$[\beta_i + \beta_{i+1}(1+\beta_i)]/[z_{\pi_i} + z_{\pi_{i+1}}(1+\beta_i)] \qquad (1b)$$

With the above on hand we can iteratively combine sets of transistors 2, 3, 4,..., N at a time.

At this point we consider two different cases, depending upon the absence or presence of the extra base-emitter resistors. The first case is much more practical due to the current levels required in the second one, but the first case has a more limited frequency response. The first case is further broken up into two subcases, that of equally biased transistors and that of tapered current levels, the latter turning out to be more practical due to increased bias voltage levels required for the former.

Case 1 : $\bar{g}_i = 0$

Here

$$\beta_i(s) = \frac{g_{m_i}}{y_{\pi_{i(s)}}} = \frac{\beta_i(0)}{1+s\frac{C_i}{g_i}}, \quad \beta_i(0) = g_{m_i}/g_i \qquad (2a)$$

and we will make the assumption that $\beta_i(s)$ can be replaced by $\beta_i(0)$, that is

$$\beta_i(s) \approx \beta_i(0) \qquad (2b)$$

This assumption is equivalent to $|s|$ small enough, that is, for $s = j\omega$,

$$\omega << \min_i(g_i/C_i) = \omega_m \qquad (2c)$$

Since $z_{\pi_i}(s) = \beta_i(s)/g_{m_i}$, the assumption of (2b) also gives

$$y_{\pi_i}(s) = g_i + sC_i \approx g_i \qquad (2d)$$

From (1a) we readily find for the N transistors

$$y_{11} \approx \frac{1}{\sum_{i=1}^{N}\left[\prod_{k=1}^{i-1}(1+\beta_k)\right] z_{\pi_i}(s)} = g_\pi + sC_\pi \approx g_\pi \qquad (3)$$

To proceed further we will assume equal transistors and then break this case into two subcases by assuming that either all transistors are equally biased or that the Nth transistor handles the major part of the current.

Case 1A: Equally Biased Transistors

Since here $g_{m_i} = g_m$ for all i, equation (1b) gives, independent of s,

$$y_{21} = g_m \qquad (4a)$$

while (3) becomes with $g_i = g$, $C_i = C$, $\beta_i(0) = \beta_0$,

$$y_{11} \approx (g+sC)/\left[\sum_{i=1}^{N}(1+\beta_0)^{i-1}\right] \approx g_\pi \qquad (4b)$$

Case 1B: Nth Transistor Current Handling

Here we assume that the upper transistor collector currents are dominated by those below them via

$$i_{c_j} < \sum_{k=j+1}^{N} i_{c_k} \qquad (5)$$

In this case (3) is unchanged but, on using (2b), the transfer admittance is

$$y_{21} = \frac{g_{m_N}}{\prod_{j=1}^{n-1}\left\{1 + \frac{r_{N-j}}{\sum_{i=N+1-j}^{N}\left[\prod_{k=N-j}^{i-1}(1+\beta_k(0))\right] r_i}\right\}} \qquad (6)$$

where $r_i = 1/g_i$. Equation (6) can be obtained by using induction on the structure of Fig. 3 and the current dominance of (5).

Case 2: $\bar{g}_i \neq 0$

Although this case is capable of giving a much higher frequency of usage than Case 1, it will take a very large N to achieve this and, hence, is not as immediately practical. Consequently in order to simply present the idea we limit to the case of equally biased equal transistors for which we have

$$g = g_i, \; C = C_i, \; g_m = g_{m_i}, \; i = 1,2,\ldots,N \qquad (7)$$

When augmented by the $\bar{g}_i$, all of which may be different, the individual transistor input conductances are

$$G_i = g + \bar{g}_i \qquad (8a)$$

while in order to obtain a first order equivalent at each iterative step we crucially set

$$1 = C_i/C_{i+1} = (G_i + g_{m_i})/G_{i+1} \qquad (8b)$$

which is the same as, using (8a),

$$\bar{g}_{i+1} = \bar{g}_i + g_m \qquad (8c)$$

If, for convenience, we set $\bar{g}_1 = 0$ then

$$\bar{g}_i = (i-1)g_m$$

Use of (8) in (1) shows that for the combination of transistors T_{N-1} and T_N we get the input admittance as $(g/2)(1+s[C/g])$ and g_m for the transconductance; the resulting equivalent circuit is of the same form. Using this result again with (1) we find for T_{N-2} and the T_{N-1} & T_N combination that the input admittance is $(g/3)(1+s[C/g])$ and g_m is again the overall transconductance. Continuing and using induction we find that the hybrid-pi equivalent circuit for the entire N-Darlington transistor has

$$y_{11} = y_\pi = \frac{1}{N}(g+sC) = g_\pi + sC_\pi \;, \; y_{21} = g_m \qquad (9a)$$

It is seen that y_{11} is N times smaller than for a single transistor while

$$\beta = \frac{y_{21}}{y_{11}} = \frac{Ng_m}{g} \cdot \frac{1}{(1 + s\frac{C}{g})} = N\frac{\beta_0}{1 + s\frac{C}{g}} \quad (9b)$$

is N times as big as that of a single transistor. It should be noted that no frequency limitation is placed on the validity of (9), in contrast to (2c), this being the importance of Case 2.

However, in order to reduce the number of transistors being used and to strengthen the dominative role of C_μ to get the first order characteristic, in both cases we would construct T_1 so as to have a relatively large C_μ. Except for this, all transistors have been considered equal and biased at identical operating points except for Case 1B.

With these points in mind we comment that in order to practically realize case 2, which has the higher allowable frequency response, it is necessary to introduce the base-emitter resistors, the last of which has resistance $r_N = 1/[(N-1)g_m]$. For large N this is a small resistor which consequently draws a relatively large current. For this reason we concentrate on Case 1 in the next sections.

III. THE N-DARLINGTON STAGE

The gain of the N-Darlington stage of Fig. 2 is found by using the equivalent circuit of Fig. 3. Assuming the bias resistors R_{b1} & R_{b2} do not affect the gain, or alternatively are considered in a Norton's equivalent $R_s = 1/G_s$, straightforward analysis gives

$$\frac{V_o}{V_s} = \frac{-G_s(g_m - sC_\mu)}{s^2C_\mu C_\pi + s[G_L(C_\mu + C_\pi) + C_\mu(g_m + G_s + g_\pi)] + G_L(G_s + g_\pi)} \quad (10)$$

Under the assumptions, made reasonable by choice of T_1, R_s, and N,

$$C_\mu > C_\pi \ , \quad g_m > G_s + g_\pi \quad (11a)$$

(10) becomes

$$\frac{V_o}{V_s} = -g_m\frac{R_L}{R_s} \cdot \frac{1}{C_\mu(1 + g_mR_L)} \cdot \frac{1}{s + \frac{G_s + g_\pi}{C_\mu(1 + g_mR_L)}} \cdot \frac{1 - sC_\mu/g_m)}{1 + s\frac{R_LC_\pi}{1 + g_mR_L}} \quad (11b)$$

The pole and the zero inside the right-hand bracket are, with good design, much further from the origin than the other pole. For small enough frequencies, ω for $s = j\omega$, the right hand bracketed term aproximates 1 and (11b) becomes

$$\frac{V_o}{V_s} \approx -g_m\frac{R_LG_s}{G_s + g_\pi} \cdot \frac{1}{1 + s\left[\frac{C_\mu(1 + g_mR_L)}{G_s + g_\pi}\right]} = \frac{K_o}{1 + (s/\omega_c)} \quad (12a)$$

For example (12a) holds, subject perhaps to the approximation of (2c) in Case I, when

$$\omega << \min\left(\frac{g_m}{C_\mu}, \frac{(1 + g_mR_L)}{R_LC_\pi}\right) = \omega_M \quad (12b)$$

Now R_s, N and R_L are free to be chosen while C_μ can be adjusted to within some degree by adjusting the collector area of transistor T_1 (for example a lateral transistor gives a large C_μ). Consequently we can make the cut-off frequency

$$\omega_c = (G_s + g_\pi)/[C_\mu(1+g_mR_L)] \quad (12c)$$

as small as desired, in which case the N-Darlington amplifier approximates an ideal integrator as closely as desired, at least for low enough frequencies, $0<\omega<<\omega_M$, or in Case 1, $0<\omega<<\min(\omega_m, \omega_M)$.

It is to be observed that g_m, g and C of the individual transistors are given roughly by [7, p.45] and [8, Chap. 4] (here we have dropped the i's of Fig. 3 for convenience)

$$g_m = \frac{\alpha}{r_e}, \quad r_e = \frac{V_T}{I_E}, \quad V_T = kT/q \ , \quad \alpha = \frac{\beta_0}{1 + \beta_0} \quad (13a)$$

$$g = g_m/\beta_0 = 1/[(1+\beta_0)r_e] \quad (13b)$$

$$C = \tau g_m/\beta_0 \ , \ \tau = \text{lifetime of base majority carriers} \quad (13c)$$

Consequently

$$\tau = C/g \quad (13d)$$

and the cut-off frequency due solely to y_π is identical for the N-Darlington transistor and all its subtransistors in all cases as seen by (2d), (3) and (9a). However, it should be noted that if Case 1 can be held then it is easy to achieve the $C_\mu > C_\pi$ constraint of (11a), this being for any N in contrast to Case 2. Consequently, for Case 2 it is important to choose transistor T_1 to have a very large C_μ. This latter can be achieved by various means, for example by reversing collector and emitter designs and by using a lateral T_1. If desired, one can also add an external C_μ, though this somewhat defeats the active-R philosophy except that this external C_μ can be considerably smaller than required in an op-amp integrator for example.

IV. EXAMPLE

To confirm the theory the circuit of Fig. 3 was evaluated on SPICE II[9] for N = 1, 2, 3, and 4 under the conditions of equal (Case 1A) and unequal (Case 1B) operating points (for N = 2, T_3 & T_4 were absent, etc., in Fig. 3). In the design of the circuit of Fig. 3 it was assumed that the bias source, V_{cc}, the load resistor, R_L, and the source resistor, R_s, were all fixed beforehand (in two instances V_{cc} was raised from 24v to 40v to show the effect of this change). In all cases the same transistor model was used, its parameters being given in Table 1.

Figure 4 gives a plot of the corresponding frequency responses.

REFERENCES

[1]. J.R Brand and R. Schaumann, "Active R filters: review of theory and practice", IEE Proceedings Part G Electronic Circuits and Systems, July 1978, Vol. 2, No.4, pp. 89-101.

[2]. S. Srinivasan, "Synthesis of transfer functions using the operational amplifier pole", Int. J. Electronics, 1976, Vol. 40, No. 1, pp.5-13.

[3]. A. Soderstrand, "Design of Active R filters using only resistors and operational amplifiers", Int. J. Electronics, 1976, Vol. 40, No. 5, pp.417-432.

[4]. A. Soderstrand, "A Simple Synthesis technique for active R filters", Proceedings of the IEEE, '75 ISCAS, pp. 261-265.

[5]. R. Schaumann, "Low-Sensitivity, high-frequency, tunable active filter without external capacitors", Proceedings of the IEEE International Symposium on Circuits and Systems, 1974, pp. 438-442.

[6]. R. Gray and G. Meyer, "Analysis and Design of Analog Integrated Circuit", John Wiley & Sons, New York, 1977.

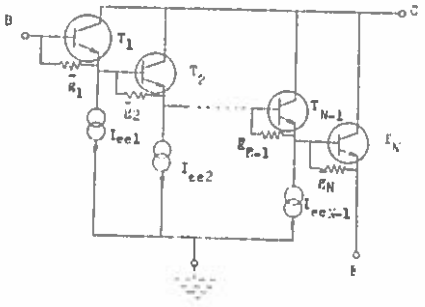
[7]. M. Herpy, "Analog Integrated Circuits", John Wiley and Sons, New York, 1980.

[8]. J.R.A. Beale, E.J. Emms, and R.J. Hilbourne, "Microelectronies", Taylor & Francis, Ltd., London, 1971.

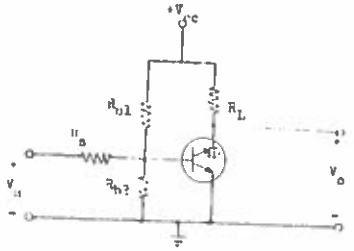
[9]. A. Vladimirescu, A.R. Newton and D.O. Pederson, "SPICE Version 2F.1 User's Guide", Dept. of Electrical Engineering and Computer Sciences. University of California, Berkeley, CA.

Table 1
Model Parameter for SPICE

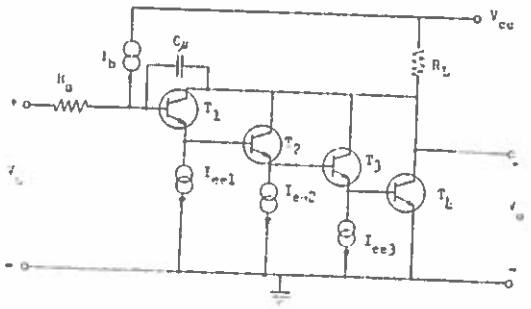
	BF	BR	VBF	IS	RB	RE	RC	TF	CJE	VJE	MJE	CJC	VJC	MJC	CJS	VJS	MJS
NPN	100	2	130 V	5×10^{-15} A	200 Ω	2 Ω	200 Ω	.35 ns	1 pf	0.7 V	0.33	0.3 pf	0.55 V	0.55	3 pf	0.52 V	0.5



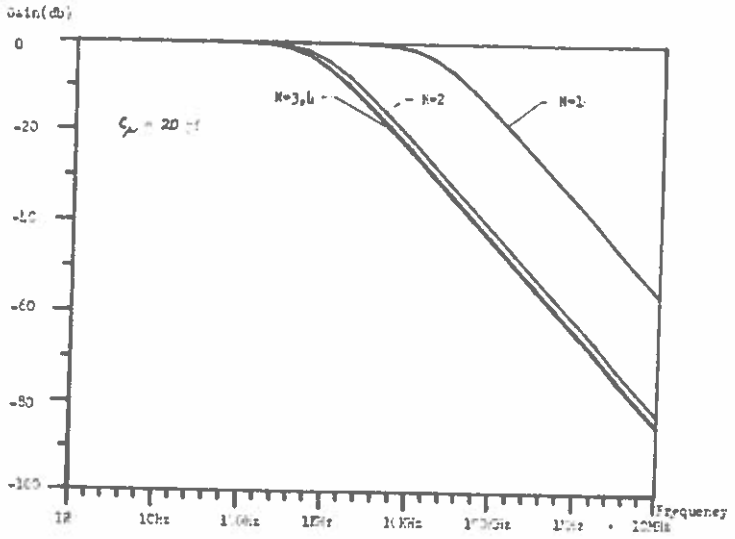
1. The N-Darlington Transistor



2. The N-Darlington Stage



3. Example Circuit



4. Frequency Response

ADVANCES IN CIRCUITS AND SYSTEMS

The Proceedings of China 1985 International Conference on Circuits and Systems

Sponsored by Academia Sinica

in Cooperation With

IEEE Circuits and Systems Society

June 10-12, 1985
Fragrant Hill Hotel
Beijing, China

Edited by

Institute of Electronics, Academia Sinica, Beijing

Science Press
Beijing, China
World Scientific
Singapore
1985