MOS Voltage Controlled OTA for Fukahori Realizations

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Abstract:
An all MOS operational transconductance amplifier (OTA) is presented which allows for linear and/or inverse linear variation of the transconductance with controlling voltages. The primary nonlinearity is eliminated following a compensation technique of Soo & Meyer such that an OTA realization of voltage adjustable state variable filters can result using the ideas of Fukahori.

I. Introduction

Fukahori [1] has presented a very useful circuit for realizing bipolar voltage-controlled tunable filters. Because of its versatility it seems profitable to obtain an MOS circuit based upon the same principles. But in looking over a number of MOS operational amplifier circuits [2] - [5] we find that modifications are necessary especially if reasonable signal swings are to be encountered. Toward this we find some excellent ideas available in the paper of Soo & Meyer [6], where the concepts can be carried over from an analog multiplier circuit to an OTA. Here we present the resulting circuit, which is given in Fig. 1.

II. The Circuit

Here we discuss the principle of operation and design of the proposed OTA. Thus, consider the circuit of Fig. 1 which is to be looked upon as the cascade of four sections. Section 3 is a gain amplifier, converting the voltage v_2 into v_3 by using a voltage to difference current converter with an active load R_3. This converter is made more linear by inserting a compensation stage, section 2, following Soo and Meyer [6], which allows for the relationship of v_3 versus v_1 to be more linear than that of v_3 versus v_2. The output section, 4, inserts voltage control linearly into the numerator of the resulting transconductance while the input section 1 inserts voltage control linearly into the denominator.

For all of the transistors we assume operation in the square-law region, for which we have the drain current I_D given by

$$I_D = k(V_{GS} - V_T)^2 \tag{1}$$

where V_{GS} = voltage gate-source, V_T = threshold voltage and k is a device constant (fixed by layout). Operated as a resistor, with the drain tied to the gate, and when $V_T = 0$, we have $V_{GS}^2 = I_D^2/(kI_D)$ or a resistance of

$$R = 1/(kI_D)^{1/2} \tag{2}$$

Turning first to section 3 of the circuit, we have using (1) [6, eq.(1)]

$$I_{D1} - I_{D2} = k_3 v_2 (2I_{DD3}/k_3 - v_2^2)^{1/2} \tag{3a}$$

$$\approx (2k_3 I_{DD3})^{1/2} v_2 \tag{3b}$$

where we make the small signal approximation

$$v_2^2 \ll 2I_{DD3}/k_3 \tag{3c}$$

The upper transistors in section 3 form a pair of active resistors of resistance R_3, for each of which $I_D = I_{DD3}/2$, is to be used in (2). Thus, on using (3b) and the value for R_3 from (2)

$$v_3 = -R_3(I_{D1} - I_{D2}) \approx -R_3(2k_3 I_{DD3})^{1/2} v_2 \tag{3d}$$

$$= -(k_3/k_{R3})^{1/2} v_2 \tag{3e}$$

The voltage v_3 is the input into section 4 for which, as at (3a) rearranged

$$I_{D3} - I_{D4} = (2k_4 I_{DD4})^{1/2}[1-(k_4/(2I_{DD4}))v_3^2]^{1/2}v_3 \quad (4a)$$

Without using the small signal approximation on v_3 in (4a), but retaining that on v_2, substitution of (3e) into (4a) gives

$$I_{D3} - I_{D4} \approx -(2k_3k_4I_{DD4}/k_{R3})^{1/2}\cdot [1-(k_3k_4/(2I_{DD4}k_{R3}))v_2^2]^{1/2}v_2 \quad (4b)$$

We will relate this output section current difference to that for section 2.

For section 2 the compensator gives [6, eq.(7)]

$$I_{11} - I_{12} = (2\underline{k}_2 I_{DD2})^{1/2}[1-(\underline{k}_2/2I_{DD2})v_2^2]^{1/2}v_2 \quad (5)$$

We see from (5) and (4b) that $I_{11} - I_{12}$ and $I_{D3} - I_{D4}$ are proportional if we set

$$k_3k_4/(2k_{R3}I_{DD4}) = \underline{k}_2/(2I_{DD2}) \quad (6a)$$

Since we will wish to vary I_{DD4} and the k's are constants, we set

$$I_{DD2} = I_{DD4} \quad (6b)$$

Under the assumption of (6a), we have from (4b) and (5)

$$I_{D3} - I_{D4} = -[(k_3k_4I_{DD4})/(\underline{k}_2k_{R3}I_{DD2})]^{1/2}(I_{11}-I_{12}) \quad (7)$$

Next we evaluate this in terms of the input to section 2, v_1. As for Eq.(3a)

$$I_{11} - I_{12} = (2k_2I_{DD2})\ [1-(k_2/(2I_{DD2}))v_1^2)^{1/2}v_1 \quad (8)$$

and substitution into (7) gives

$$I_{D3} - I_{D4} = -[(2k_2k_3k_4I_{DD2})/(\underline{k}_2k_{R3})]^{1/2}\cdot [1-(k_2/(2I_{DD2}))v_1^2)^{1/2}v_1 \quad (9a)$$

Since we have a small signal assumption on v_2 we will have one on v_1, that is,

$$v_1^2 \ll 2I_{DD2}/k_2 \quad (9b)$$

and (9a) becomes

$$I_{D3} - I_{D4} = -[(2k_2k_3k_4I_{DD4})/\underline{k}_2k_{R3})]^{1/2}v_1 \quad (9c)$$

Next we incorporate the behavior of section Here again small signal behavior is assumed, tha is

$$v_{in}^2 \ll 2I_{DD1}/k_1 \quad (10a$$

in which case, noting that the upper two transistors form a resistor R_1,

$$v_1 \approx -R_1(2k_1I_{DD1})^{1/2}v_{in} \quad (10b$$

Using (2) we have for the left resistor R_1

$$R_1 = 1/[(I_{DR1}+\underline{I}_1)k_{R1}]^{1/2} \quad (11a$$

in which we will assume

$$I_{DR1} \gg \underline{I}_1 \quad (11b$$

Thus, (11a) becomes

$$R_1 \approx 1/(I_{DR1}k_{R1})^{1/2} \quad (11c$$

The result will be the same for the right resis R_1.Substituting (11c) into (10b) gives the volt gain for the first section as

$$v_1 \approx -[(2k_1I_{DD1})/(I_{DR1}k_{R1})]^{1/2}v_{in} \quad (12$$

Equation (12) is to be substituted into (9c yield the overall transfer characteristics. But before doing this we note the means of varying current sources for I_{DR1} and I_{DD4}. Here we construct the current sources as MOS transistor with $V_T = 0$. From (1) we then have

$$I_{DR1} = \underline{k}_{r1}v_{GS1}^2 \quad (13$$

$$I_{DD4} = \underline{k}_4v_{GS4}^2 \quad (13$$

To vary the current source values we, therefore, simply vary the gate to source voltages of MOS transistors having zero threshold voltages.

Noting that the output current I_o is $I_{D4} - I_{D3}$, substitution of (13a,b) into the result of (12) into (9c) finally yields

$$I_o = -K[v_{GS4}/v_{GS1}]v_{in} \qquad (14a)$$

where

$$K = 2[(k_1k_2k_3k_4k_5I_{DD1})/(k_{M1}k_{M2}k_{M3})]^{1/2} \qquad (14b)$$

We see via (14a) that we have achieved the desired goal, that of having a transconductance, g_m, linearly variable in numerator and denominator, $g_m = -K[v_{GS4}/v_{GS1}]$, with the variations arising in an easily realized manner.

III. Discussion

Here we have introduced a voltage variable OTA. This is of course just a first step and much more needs to be done. Especially the circuit needs to be tested both on the computer and via physical constructions. Indeed it may be possible to incorporate some simplifications and optimizations. For example, in some cases it may be possible to replace the full four stage circuit by just the first stage and put voltage variation in I_{DD1}. Or it may be desired to obtain square law variation of g_m in which case the present circuit can be retained with voltage variation added again via I_{DD1}. It should also be observed that a number of commercial voltage variable OTA's are available, vor example the RCA CA3080A. But we are unaware as yet of any with the flexibility of the circuit presented here as well as with the advantages offered by MOS technology.

Acknowledgments

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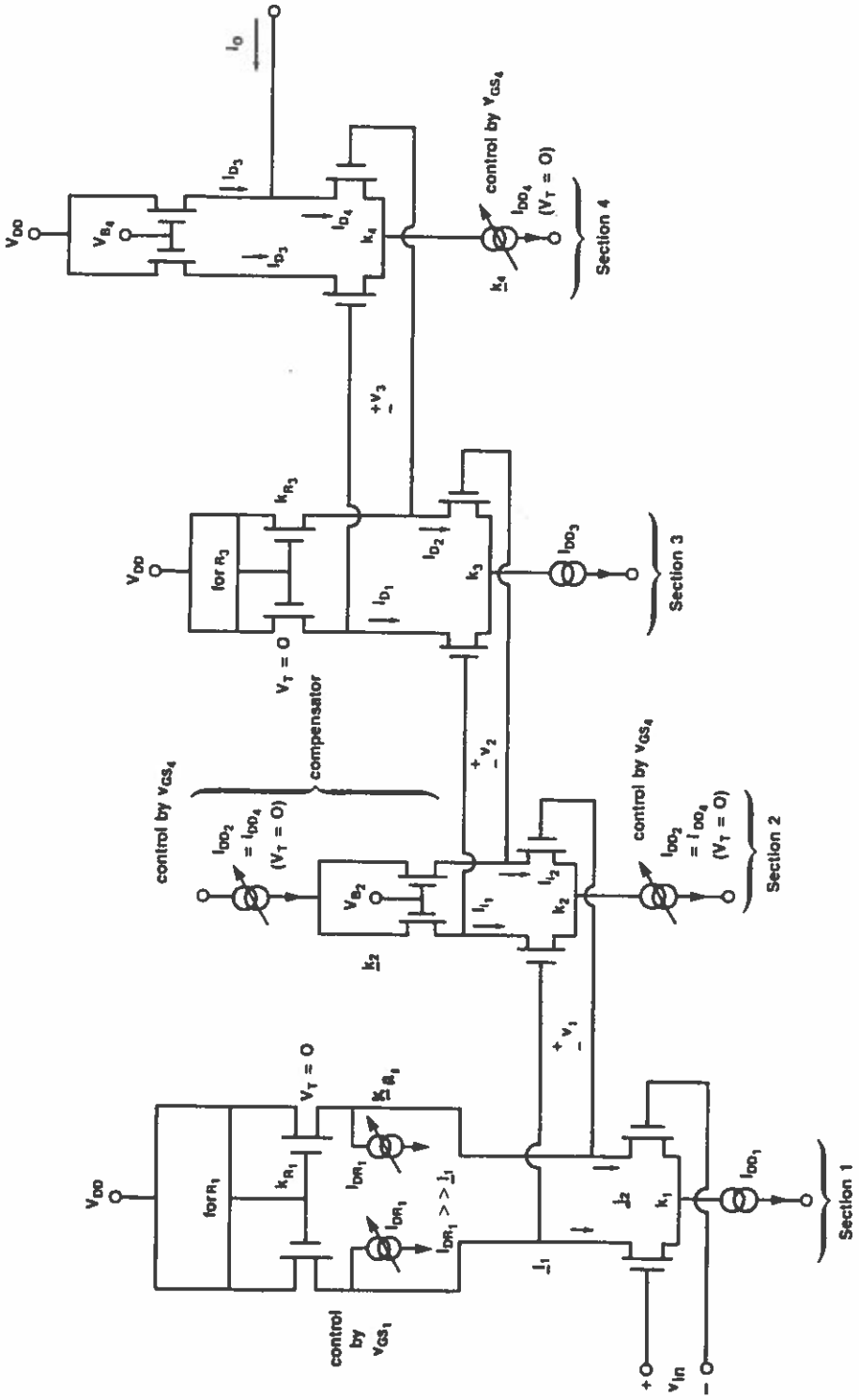

FIGURE 1
MOS OTA

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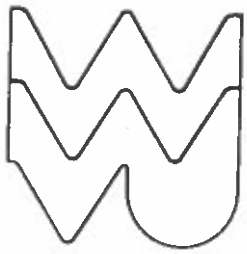

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