252

AN MOS UNIVERSAL CIRCUIT+

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"Il ne peut être un homme honnête
qui cesse d'écrire ses poemes.
Il tue la veracité." [1]

I. Introduction

Equilibrium points can serve as a basis for the study of different aspects of nonlinear differential systems. For example one aspect that could be of interest in design is that the state-space of structurally stable second order systems can be decomposed into cells [2,p.175] which are bounded by equilibrium points and associated trajectories. Consequently, it is of interest to have electronic circuits which can realize prescribed equilibrium points. For structurally stable second order systems there are five types of equilibrium points of interest: the stable and unstable nodes, the stable and unstable foci, and saddle points.

Chaikin [3,p.194] has presented a vacuum tube circuit, called the Universal Circuit, which will realize all of these structurally stable equilibrium points (located at the origin), each such point being realized by an appropriate setting of resistors in the circuit. With the change to solid-state technology it is of interest to have a universal circuit realized in MOS technology. This is presented in the next section, Fig. 1, with the linearized state-variable equations. Biasing is then considered and shifting to equilibrium points other than at the origin outlined.

II. An MOS Universal Circuit

Figure 1 shows the circuit of interest. This is obtained from that of Chaikan [3,p.194] by suitable modifications reflecting the change from triodes to n-channel MOS devices with improvement in the bias circuitry.

We will assume that the transistors are biased to operate in the square-law region and then we linearize about the operating point. Thus we assume the drain current law to be

$$i_D = K(v_{GS} - V_T)^2 \tag{1}$$

where v_{GS} is the gate-source voltage and K & V_T are device constants. If the operating point values are $i_D = I_D$, $v_{GS} = V_{GS}$, then, in terms of small signal quantities $i_d = i_D - I_D$, $v_{gs} = v_{GS} - V_{GS}$, (1) is

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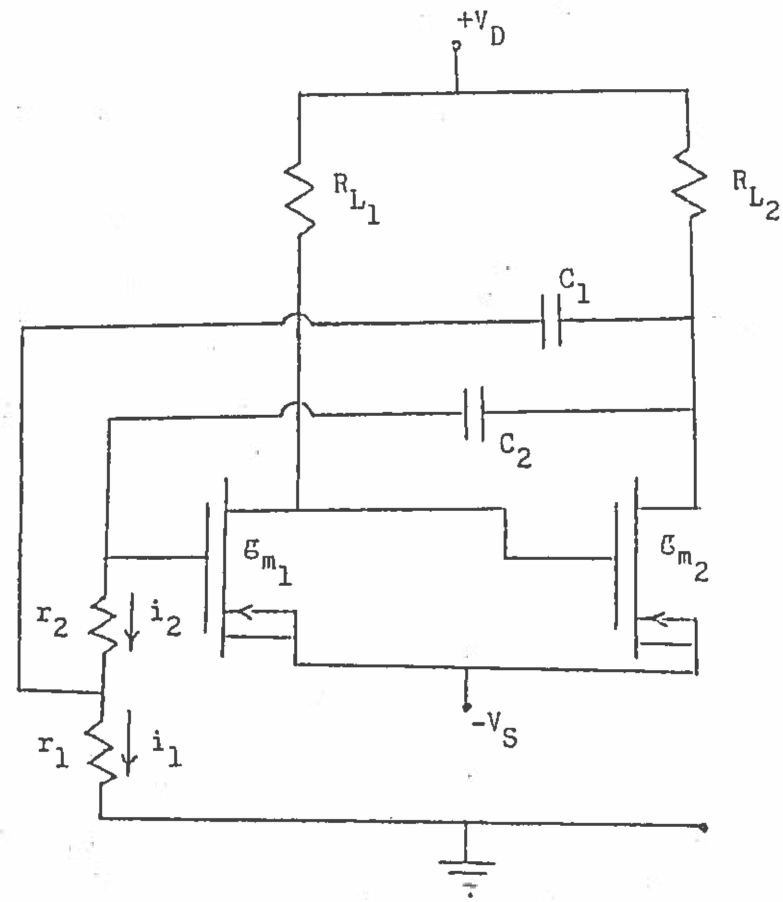

Figure 1
An MOS Universal Circuit

$$i_d = g_m v_{gs} + K v_{gs}^2 \tag{2a}$$

in which

$$g_m = 2K(V_{GS} - V_T) \quad , \quad I_D = KV_{GS}^2 \tag{2b}$$

The linearized MOS model is then

$$i_d = g_m v_{gs} \tag{2c}$$

Using (2c) a straightforward analysis of the circuit gives the state-variable equations

$$\frac{di_1}{dt} = \frac{1}{(R_{L_1} + \alpha r_1)C_1} [-\alpha i_1 + (\{1 + \frac{C_1}{C_2}\}\alpha - \frac{C_1}{C_2}) i_2] \tag{3a}$$

$$\frac{di_2}{dt} = \frac{1}{r_2 C_1} [i_1 - \{1 + \frac{C_1}{C_2}\} i_2] \tag{3b}$$

where

$$\alpha = 1 - (g_{m_1} R_{L_1})(g_{m_2} R_{L_2}) \tag{3c}$$

Equations (3) are identical to those of Chaikan [3,p.194] if $R = R_{L_2}$, $g = g_{m_2}$, $k = g_{m_1} R_{L_1}$ are chosen. Hence, by choosing $\alpha = -1$ with R constant, by varying r_1 and r_2 any of the structurally stable equilibrium points can be obtained with the design graph [3,p.196] remaining exactly valid. However, practically α other than -1 may be more convenient since $g_{m_1} R_{L_1}$ and $g_{m_2} R_{L_2}$ are the gains of the respective amplifier stages. Therefore we obtain the characteristic polynomial, P(s), of the system from which one can design for arbitrary roots for any prescribed α, $\alpha < 1$.

The state-variable equations (3a,b) are of the 2-vector form

$$\frac{di}{dt} = Ai, \quad A = \begin{bmatrix} \dfrac{-\alpha}{(R_{L_1} + \alpha r_1)C_1} & \dfrac{(1 + \frac{C_1}{C_2})\alpha - \frac{C_1}{C_2}}{(R_{L_1} + \alpha r_1)C_1} \\ \dfrac{1}{r_2 C_1} & \dfrac{-(1 + \frac{C_1}{C_2})}{r_2 C_1} \end{bmatrix} \tag{4a}$$

from which the characteristic polynomial is

$$P(a) = \det(s1_2 - A) = s^2 + \left[\frac{\alpha}{(R_{L_1} + \alpha r_1)} + \frac{(1 + \frac{C_1}{C_2})}{r_2}\right] \cdot \frac{1}{C_1} s + \left[\frac{1}{(R_{L_1} + \alpha r_1) r_2 C_1 C_2}\right] \tag{4b}$$

where 1_2 is the 2 x 2 identity matrix.

III. Biasing

Biasing of the universal circuit of Fig. 1 is relatively straightforward. To simplify the presentation let us assume that both transistors are identical and write $K = K_1 = K_2$, $V_T = V_{T_1} = V_{T_2}$. Using the notation introduced at (2) (with V_{DS} the drain-source bias voltage) we have, by inspection of Fig. 1 and (1)

$$V_{GS_1} = V_S \tag{5a}$$

$$I_{D_1} = K(V_S - V_T)^2 \tag{5b}$$

$$V_{DS_1} = V_{GS_2} \tag{5c}$$

$$= -R_{L_1} I_{D_1} + V_D + V_S \tag{5d}$$

$$I_{D_2} = K\,(V_{GS_2} - V_T)^2 \tag{5e}$$

$$V_{DS_2} = -R_{L_2} I_{D_2} + V_D + V_S \tag{5f}$$

Therefore we choose V_S to have $V_{GS_1} > V_T$, say $V_S = aV_T$, $a \geq 2$. Conveniently we next choose V_D, say $V_D = V_S$. V_{DS_1} is chosen to place the bias point in the square-law region; for this $V_{DS_1} = V_S$ might be considered such that both transistors have the same gate voltage. At this point R_{L_1} is fixed by (5d)

$$R_{L_1} = \frac{V_D + V_S - V_{DS_1}}{K(V_S - V_T)^2} \tag{5g}$$

Consequently I_{D_2} is fixed and R_{L_2} chosen via (5f) for a desired V_{DS_2}. Possible are

$$V_S = V_D = V_{GS_1} = V_{GS_2} = V_{DS_1} = V_{DS_2} \doteq aV_T \tag{6a}$$

giving

$$R_{L_1} = R_{L_2} = \frac{a}{(a-1)^2} \cdot \frac{1}{KV_T} \tag{6b}$$

Typical numbers for the MC14007 are $K = 0.6 \times 10^{-3}$, $V_T = 2$ for which on choosing $a = 2$ gives $V_S = V_D = V_{GS_2} = V_{DS_1} = V_{DS_2} = 4$ and $R_L = 1.7K\Omega$.

The circuit of Fig. 1 then becomes biased to give an equilibrium point at $i = \underline{0}$. The equilibrium point can be shifted to other points of state-space by inserting current sources between the tops of r_1 & r_2 and ground (for negative equilibrium point coordinates) or the V_D node (for positive equilibrium point coordinates). These current sources can be realized by standard transistor circuits [4,p.109] but the above bias equations need slight modification since (5a) no longer holds.

"sache que des empires sont tombes
faute d'avoir resu le souffle de poeme". [1]

References

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