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SEMISTATE DESIGN THEORY*

Binary and Swept Hysteresis

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Abstract. Using semistate theory forward and reverse binary hysteresis operators are defined from which design equations result for relevant circuits. Through variation of the design parameters swept hysteresis is introduced and experimental results presented on it.

1. Introduction

Although hysteresis occurs natually in a number of systems, as for example from friction in mechanical controllers [1,p.8], it also can now be specifically designed into a system to obtain desirable properties. For example, hysteresis can be used to prevent bouncing due to noise [2,p.353], as for automated typing systems, or for the generation of action-potential kinds of pulses in neural-types microsystems [3]. Unfortunately the mathematics of hysteresis has not really kept pace with engineering developments and, thus, although catastrophe theory has led to new insights [4,p.70] it and the theory of hysterants [5] leave much to be desired, especially in terms of the dynamics of the process.

Previously we have shown [6] that semistate theory [7] gives a significantly meaningful way of describing hysteresis derived from a CMOS pair (CMOS = complementary Metal-Oxide Silicon). Here we continue this train of thought by generalizing to the concept of binary hysteresis operators mathematically realized through specified sets of semistate equations. These semistate equations can then be practically realized by Schmitt trigger types of circuits [8,p.498] [9,p.292]. Within this framework, through identification with the semistate equations, we are able to give design formulas for circuit parameters in terms of the four (axes intercept) parameters defining binary hysteresis. This in turn leads us to the possibility of varying the hysteresis. Consequently we introduce the notion of "swept

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hysteresis'' for which some experimental results are given to illustrate the practicality of the concept. Swept hysteresis is hysteresis which sweeps in time over a given region of the hysteresis-curve plane in a controlled manner. It appears that swept hysteresis could have important uses for adaptive neural-type microsystems as well as in the areas of subharmonic and chaos generation. In any event the theory of binary hysteresis presented here should be of interest since it appears that such hysteresis can be used as the basic building block for general classes of hysteresis [10].

2. Binary hysteresis: semistate, design theory

In Figure 1a is given the usual picture of what we will call ''binary'' hysteresis, this curve being classically described by [11,p.56]

$$y = \begin{cases} H_+ & \text{for} \begin{cases} u_+ \angle u \text{ or} \\ u_- \le u \le u_+, \text{ if } y_0 = H_+ \end{cases} \\ H_- & \text{for} \begin{cases} u_- \le u \le u_+, \text{ if } y_0 = H_- \text{ or} \\ u < u_- \end{cases} \end{cases} \tag{1}$$

Here H_+, H_-, u_+, u_- are real parameters characterizing the hysteresis and for which we will assume

$$H_- < H_+, u_- \le u_+ \tag{2}$$

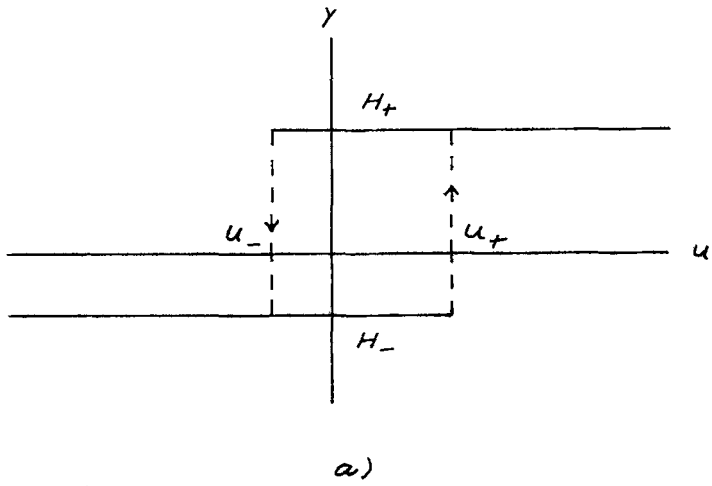
while y_0 is meant to be the ''previous value of y''. As well as the forward hysteresis of Figure 1a there is a reverse binary hysteresis as shown in Figure 1b and for which suitable changes in (1) are clear.

The mathematics of binary hysteresis, as given via (1), is, however, rather mysterious since it is only the presence of y_0 which salvages this hysteresis from being a multivalued phenomena. For sure, the need for y_0 in (1) indicates that hysteresis is a dynamic process for which one naturally would assume the presence of something like a state. But customarily Figure 1 represents the ''static'' situation for which, though, if it truly did, no y_0 would be required in the mathematical description (1). With these comments in mind we see why we are naturally led to a semistate description of hysteresis.

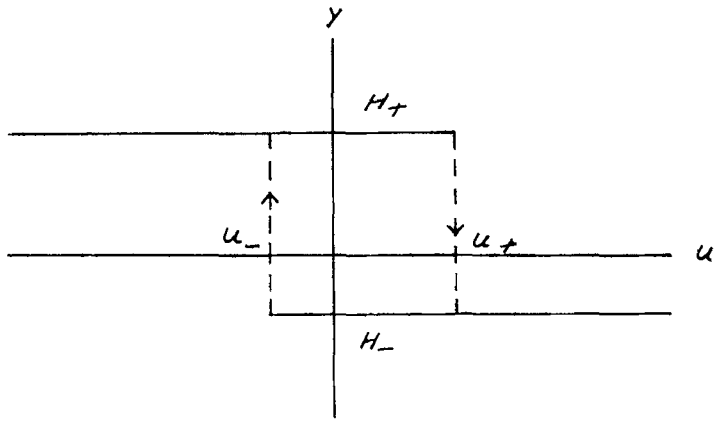
To more fully characterize binary hysteresis we conceive of a dynamic operator, $H_B(\cdot,\cdot)$, the output, y, of which depends upon the input, u, and the initial semistate x_0:

$$y = H_B(u,x_0) \tag{3}$$

This operator is to be taken such that in the truly static case it becomes a multivalued function, one of the graphs of Figure 1. Next we introduce a



a)



b)

Figure 1.Binary hysteresis curves.
(a) Forward
(b) Reverse

semistate realization of $H_B(\cdot,\cdot)$, one for each of the forward and backward types. These realizations uniquely specify the corresponding hysteresis operators $H_B(\cdot,\cdot)$. The converse, though, is not true; for example another realization than the one to be given for the reverse binary

hysteresis would result by a change in sign in defining the output (or the input) in the forward hysteresis semistate equations.

For the forward binary hysteresis we take as a set of semistate equations realizing $H_B(\cdot,\cdot)$

$$\epsilon\dot{x}_1 + (1+a)x_1 - a\,x_2 = u \tag{4a}$$

$$x_2 - f(x_1 - X_a) = 0 \tag{4b}$$

$$y = x_2 \tag{4c}$$

where $f(\cdot)$ is the step function shown in Figure 2

$$f(x_1) = H_+\,1(x_1) + H_-1(-x_1) \tag{5}$$

with $1(\cdot)$ the unit-step function and $x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$ the semistate. In terms of the constants of Figure 1a the constants a and x_a are specified as

$$a = (u_+ - u_-)/[(H_+ - H_-) - (u_+ - u_-)] \tag{6a}$$

$$X_a = u_+ + \frac{a}{1+a}H_- = \tfrac{1}{2}[(u_+ + u_-) + \frac{a}{1+a}(H_+ + H_-)] \tag{6b}$$

The parameter ϵ controls the time-constant for the dynamics with the static curve of Figure 1a found by letting $\epsilon \to 0$.

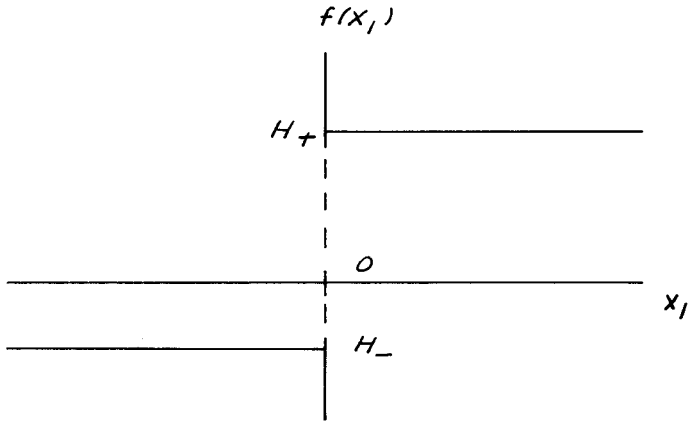


Figure 2. Graph of $f(\cdot)$ of (5).

To check that the semistate equations (4) with (5) do give the binary hysteresis of Figure 1a we then set $\epsilon = 0$, solve (4a) for x_2,

$$x_2 = (1 + \tfrac{1}{a})x_1 - \tfrac{1}{a}u \tag{7}$$

and set the right side of (7) equal to $f(x_1 - X_a)$ by (4b) and (5). This last step is equivalent to plotting (7) as a load line on the curve for $f(x_1 - X_a)$ in Figure 2 with u as a variable parameter, as illustrated in Figures 3a. From Figure 3a the graph of Figure 1a is readily visualized while the values of (6) are calculated to achieve coincidence using the relevant intersection points.

For the reverse binary hysteresis we take as a set of semistate equations

$$\epsilon \dot{x}_1 + (1+b)x_1 - x_2 - bX_b = 0 \tag{8a}$$

$$x_2 - f(x_1 - u) = 0 \tag{8b}$$

$$y = x_2 \tag{8c}$$

where again $f(\cdot)$ is as in (5). In terms of the constants of Figure 1b

$$b = [(H_+ - H_-)/(u_+ - u_-)] - 1 \tag{9a}$$

$$X_b = (1 + \frac{1}{b})\, u_+ - \frac{1}{b} H_+ \tag{9b}$$

while the corresponding load line, $x_2 = (1 + b)\, x_1 - bX_b$, now plots aginst the nonlinearity which becomes variable with u when plotted on the x_1, axis, as per Figure 3b.

Next it is important to note that insertion of the dynamics, $\epsilon \neq 0$, of the first of the semistate equations, (4a) or (8a), gives a unique motion for the solution trajectory [12, p.20] such that the hysteresis operator yields a single valued output rather than a multiple valued one as the static solutions would otherwise "imply" via Figure 3. In practice $\epsilon \neq 0$ is guaranteed by the presence at least of parasitics.

The semistate description is seen to yield an accurate characterization of the binary hysteresis operator using single valued functions. It also points out the structural stability of the hysteresis operator in that small changes in the parameters of the semistate equations and in the graph of $f(\cdot)$ do not destroy the essential characteristic (unless $u_+ = u_-$ in which case a non-hysteretic curve becomes hysteretic under small perturbations).

Because of this structural stability, physical constructs of binary hysteresis are possible. Indeed a number of op-amp circuits are known [2, pp. 342-344] [9, p. 292], Figure 4 giving respective realizations for the hysteresis of Figure 1. Thus, with the semistate equations now on hand we can give design formulas for achieving a desired binary hysteresis characteristic. In Figure 4 C is an op-amp input capacitance which is generally parasitic but which could be externally augmented.

By basic circuit analysis of Figure 4a the describing equations are, $G = 1/R$

$$R_i C \dot{v}_c + (1 + R_i G_f)\, v_c - R_i G_f v_o = v_i \tag{10a}$$

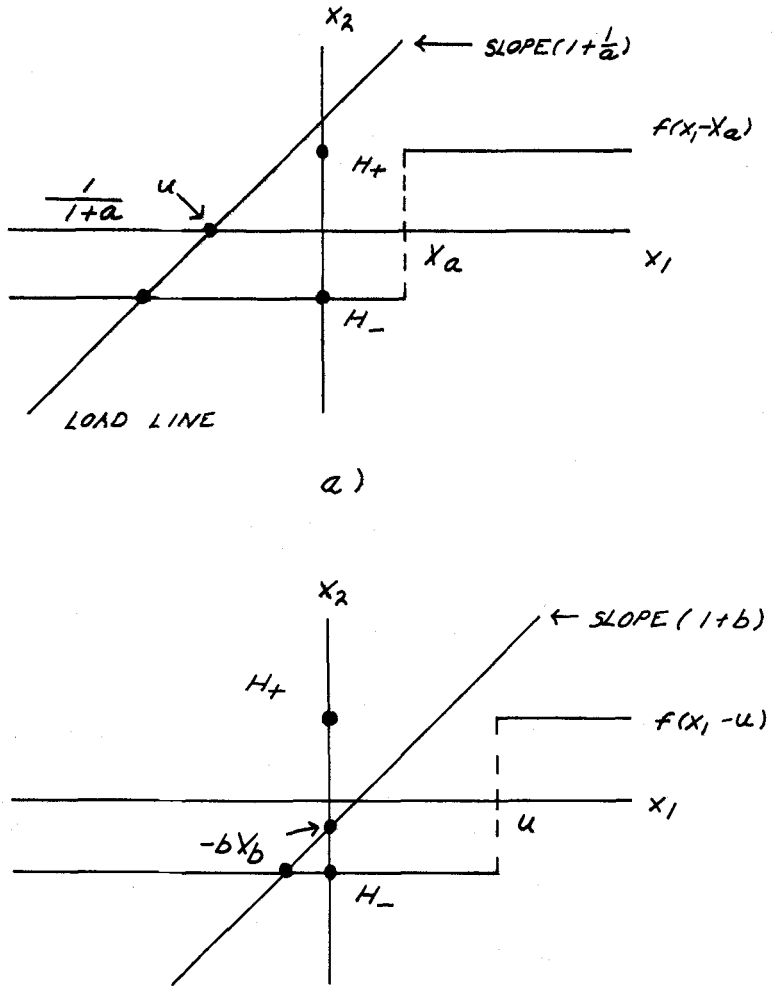


Figure 3. Creation of binary hysteresis via semistate intersections.
(a) As *u increases* the one intersection changes to two and then back to one by motion of the load line to the right.
(b) As *u decreases* the one intersection changes to two and then back to one by motion of the $f(\cdot)$ curve to the left.

$$v_o - f(v_c - V_a) = 0 \tag{10b}$$

while for Figure 4b

$$R_2 C \dot{v}_c + (1 + R_2 G_1) v_c - v_o - R_2 G_1 V_b = 0 \tag{11a}$$

$$v_o - f(v_c - v_i) = 0 \tag{11b}$$

where $f(\cdot)$ is the op-amp input-output DC characteristic and C is, as mentioned above, the input capacitance indicated for the op-amps. Since op-amp input-output characteristics closely follow the step-function $f(\cdot)$ of Figure 2, with amplitudes V_+ & V_-, equations (10) and (4), respectively (11) and (8),

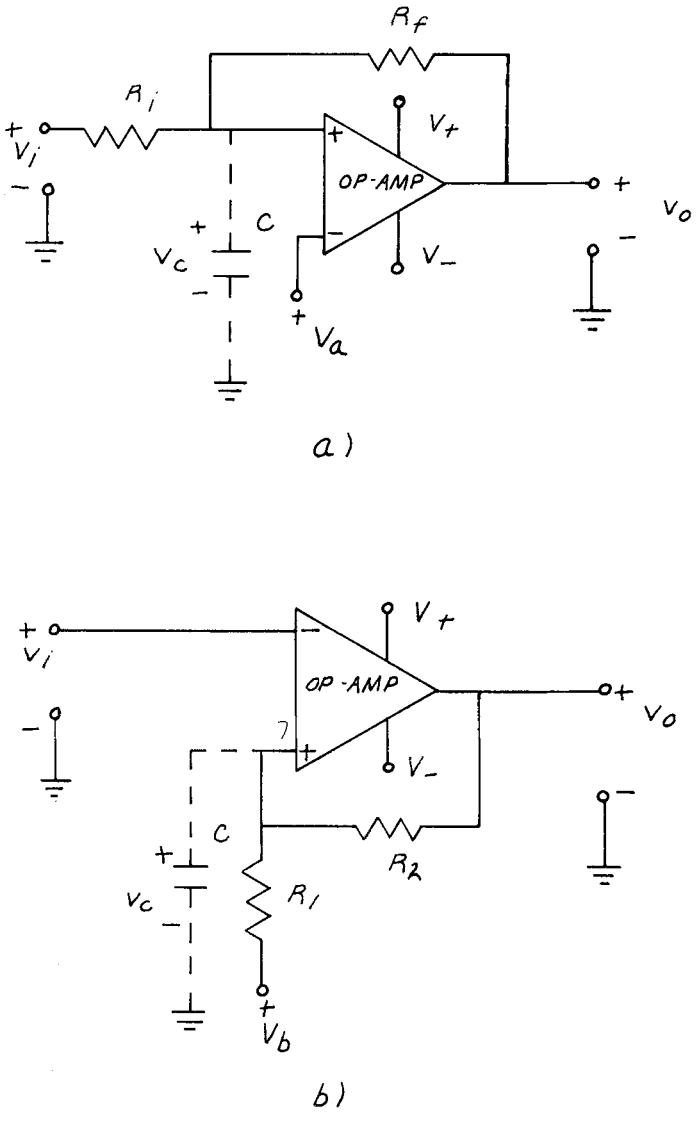


Figure 4. Binary hysteresis realization circuits.
(a) Forward
(b) Reverse

are seen to mirror each other. Thus by equating coefficients

$$a = R_i G_f, \quad X_a = V_a; \quad b = R_2 G_1, \quad X_b = V_b \tag{12}$$

are identified. However, in a normal design situation we would be given the hysteresis curves of Figure 1, that is, H_+, H_-, u_+, and u_-, and desire a circuit, as in Figure 4, to realize it. Using (6) & (9) with (12) and the op-amp $f(\cdot)$ we have

$$V_+ = H_+, \quad V_- = H_- \tag{13a}$$

$$R_i G_f = (u_+ - u_-)/[(H_+ - H_-) - (u_+ - u_-)] \tag{13b}$$

$$V_a = u_+ + \frac{R_i G_f}{1 + R_i G_f} H_- \tag{13c}$$

$$R_2 G_1 = [(H_+ - H_-)/(u_+ - u_-)] - 1 \tag{13d}$$

$$V_b = \left(1 + \frac{1}{R_2 G_1}\right) u_+ - \frac{1}{R_2 G_1} H_+ \tag{13e}$$

These specify the bias values, V_+ & V_-, for the op-amps, the reference voltages, V_a & V_b, needed, and the resistor ratios, R_i/R_f & R_2/R_1, necessary to achieve a prescribed static binary hysteresis curve. Solving equations (13) we obtain for the hysteresis curve parameters in terms of circuit parameters

$$H_+ = V_+, \quad H_- = V_- \tag{14a}$$

$$u_+ = \begin{cases} V_a - \dfrac{R_i G_f}{1 + r_i G_f} V_- & \text{Forward} \quad \text{(14b)} \\ \dfrac{R_2 G_1}{1 + R_2 G_1} \left[V_b + \dfrac{1}{R_2 G_1} V_+\right] & \text{Reverse} \quad \text{(14c)} \end{cases}$$

$$u_- = \begin{cases} V_a - \dfrac{R_i G_f}{1 + r_i G_f} V_+ & \text{Forward} \quad \text{(14b)} \\ \dfrac{R_2 G_1}{1 + R_2 G_1} \left[V_b + \dfrac{1}{R_2 G_1} V_-\right] & \text{Reverse} \quad \text{(14c)} \end{cases}$$

It should also be noted that the circuit used to produce reverse hysteresis can be cascaded with an inverting amplifier to produce forward hysteresis and similarly for forward to reverse.

3. Swept hysteresis

The presence of the reference voltages, V_a & V_b, in Figure 4, or, what is the

same thing, the parameters X_a & X_b in the semistate equations (4b) and (8a), opens up fascinating avenues since these may be separately varied. In particular, as seen from Figure 3, by suitably varying X_a, or X_b, the hysteresis curve can be horizontally swept over any desired region. Once this is recognized it is clear that by varying H_+ & H_- (i.e. the bias voltages V_+ & V_-) the hysteresis curve can be vertically swept. Since the binary hysteresis curve has four parameters, $(H_+\ H_-, u_+, u_-)$, a check of eqs. (13) or (14) shows that the natural fourth circuit element to vary is the resistance ratio, $R_i G_f$ or $R_2 G_1$. Overall, by varying the bias and reference voltages and the circuit resistance ratios various hysteresis regions can be swept through. The manner of sweeping the hysteresis depends upon the variations used in the parameters. Since these variations can generally be carried out electronically, these variations are almost limitless. Hence the varieties of swept hysteresis are almost limitless. Experimental results for several situations are next given.

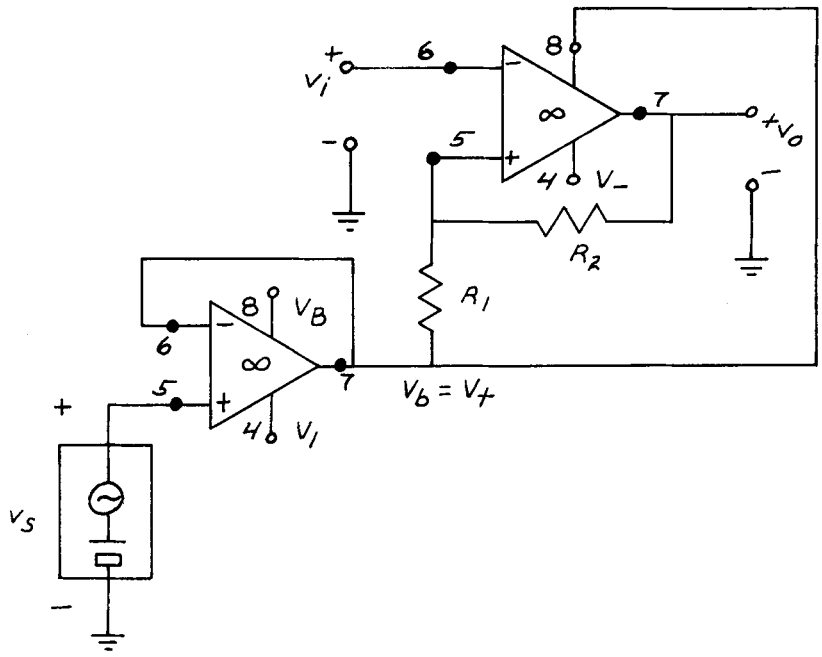
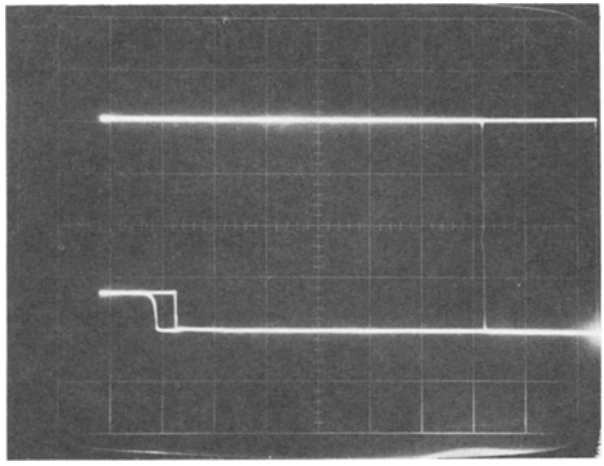
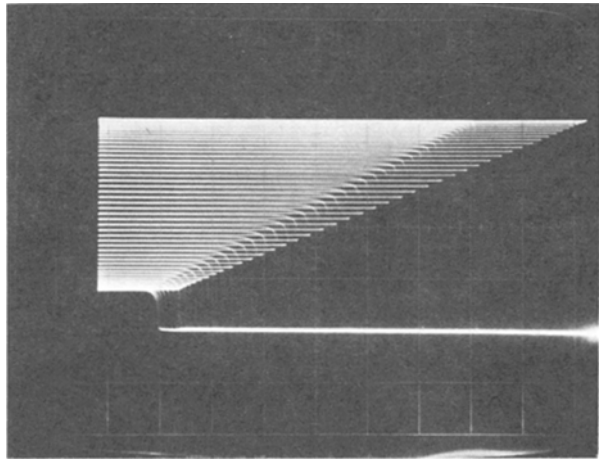


Figure 5. Circuit for simultaneous variation of $V_b = V_+$.

Figure 5 shows a configuration by which V_b and V_+ can be simultaneously varied in phase. For the ease of experimentation $V_b = V_+$ is set, but clearly $V_b \neq V_+$ can easily be obtained by various means (for example, through the insertion of another op-amp amplifier). Figure 6 shows experimental results, with Figure 6a giving the results for a square-wave and



(a)



(b)

Figure 6. Swept hysteresis from circuit of $V_b = V_+$.
Vertical = 2 v. div, Horizontal = 1 v/div; (0,0) at center
op-amps = MC1458CP (pin numbers as in Figure 5)
R_1 = 30K, R_2 = 100K, $V_B = +4v$, $V_- = -4v$
$v_{s\min} = -2.5v$, $v_{s\max} = +4v$, $1Hz$
v_i = sine wave at $10Hz$, $v_{i\min} = -4.4v$, $v_{i\max} = +5.5v$
(a) v_s = square wave
(b) v_s = sine wave

Figure 6b for a sine-wave parameter varying source. The former, Figure 6a, thus shows the limits through which the latter, Figure 6b, is sweeping since the peak amplitudes are equal [$v_{s_{\min}} = -2.5v$, $v_{s_{\max}} = +4v$ varied at 1Hz; v_i is a sine wave at 10Hz]. Note that with the measuring equipment on hand (primarily a Tektronix 561 oscilloscope) the vertical lines in Figure 6b have not reproduced well. In actual fact the true display shows a set of vertical lines continuously present between -3v and $+5.5$v of the horizontal scale. Note also that H_- can equally easily be varied as H_+ has been here.

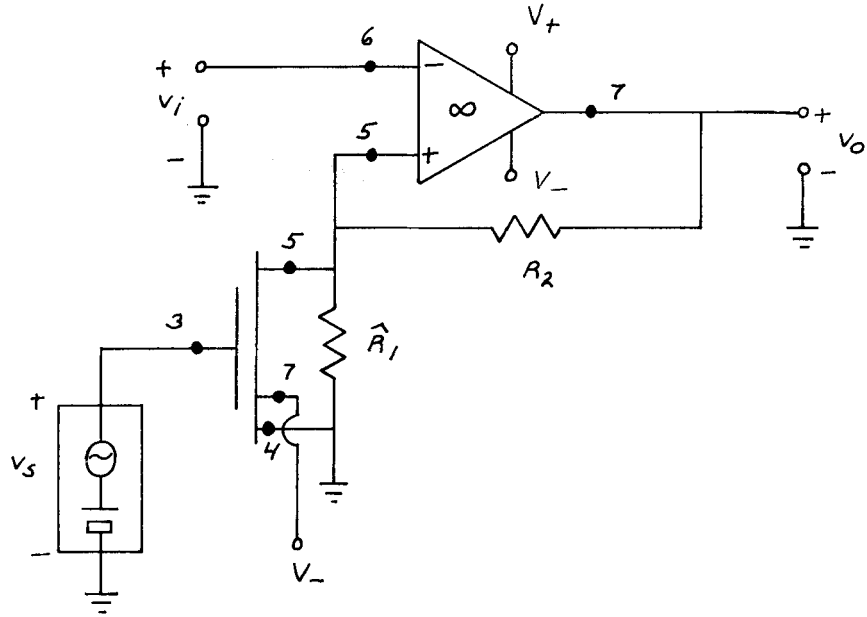
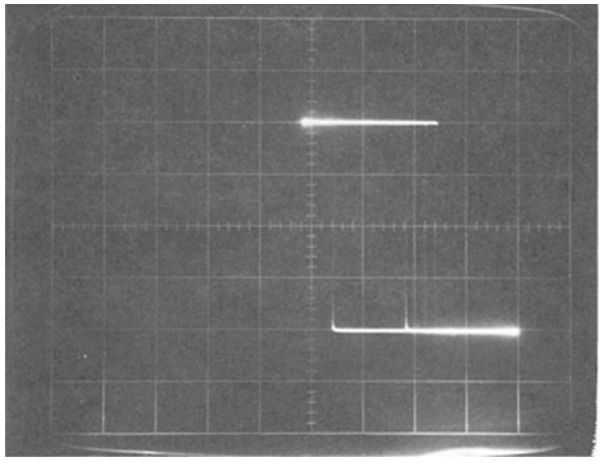


Figure 7. Circuit for variation of R_1.

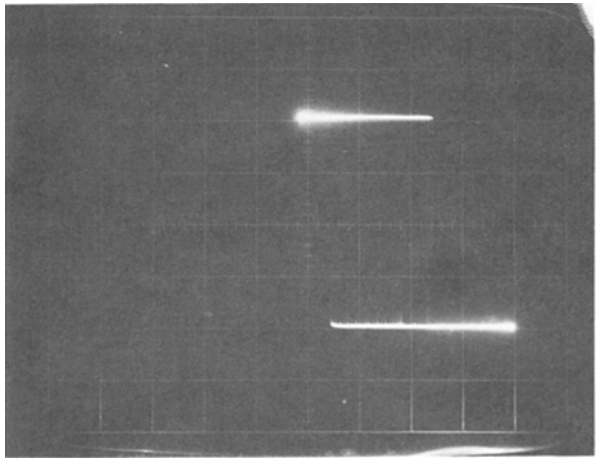
Figure 7 shows a configuration for varying R_1 using the gate voltage controlled drain-source resistance of an MOS transistor. Figure 8a shows the resulting hysteresis change for a square-wave gate-source voltage v_s, ($v_{s_{\max}} = +2$v, $v_{s_{\min}} = +1$v, varied at 100Hz); the left-most and right-middle traces are for the MOS transistor turned off. Figure 8b shows the result for a corresponding sine-wave v_s (again the trace has not reproduced well, there being a continuous set of vertical lines between $+0.4$v and $+2.4$v of the horizontal scale).

4. Discussion

Here we have given semistate equations for binary hysteresis, these semistate equations, (4) & (8) with (5), corresponding to physical realiza-



(a)



(b)

Figure 8. Swept hysteresis from circuit of Figure 7.
Vertical = 2 v/div, Horizontal = 1 v/div; (0,0) at center
op-amp = MC1458CP, n-channel MOS = MC14007CP (pin numbers as in Figure 7)
R_1 = 30K , R_2 = 30K , V_+ = +4v, V_- = −4v
$v_{s\min}$ = +1v, $v_{s\max}$ = +2v, 100Hz
v_i = sine wave at 10Hz, $v_{i\min}$ = +0.5v, $v_{i\max}$ = +4v
(a) v_s = square wave
(b) v_s = sine wave

tions, Figures 4a and 4b, in terms of op-amps. The dynamics of the semistate equations correspond to an input capacitance at the op-amp imput, this usually being a parasitic in practical realizations. Since the parasitics are ususally small the time constants associated with the semistate equations containing dynamics are also small, i.e. ϵ small. Thus, responses quickly approach the values determined by $\epsilon = 0$, that is, the responses are primarily in the slow (or steady state) manifolds determined by $\epsilon = 0$. However, if large input capacitances occur in the circuits given or if the time-scale is decreased (by operation with higher frequency signals) then the dynamics serves to do more than guarantee a unique response and much altered behavior results. For this reason the experimental results have been recorded here for low input frequencies to present the essential hysteresis phenomena represented by the slow manifolds of the solutions space.

The semistate equations allow time dependent parameters and when any of these parameters are time-wise varied a swept hysteresis results. Several cases have been illustrated in Figures 5 through 8 for the reverse hysteresis case. Analytically the reverse hysteresis case is rather interesting since the semistate equations (8) are not in the canonical form of [7] (in contrast the ones, (4), of forward hysteresis are). Letting $\bar{x}_1 = x_1 - u$ does eliminate u from the nonlinearity of (8b) but introduces a derivative on u in (8a) which in turn can be eliminated by letting $x_3 = u$. Thus canonical semistate equations for reverse binary hysteresis are

$$\epsilon\dot{\bar{x}}_1 + \epsilon\dot{x}_3 + (1+b)\,\bar{x}_1 - x_2 - bX_b = -(1+b)\,u \tag{15a}$$

$$x_2 - f(\bar{x}_1) = 0 \tag{15b}$$

$$x_3 = u \tag{15c}$$

$$y = x_2 \tag{15d}$$

It should be noted that these canonical semistate equations are still of degree one in the derivative operator (as seen by setting $\hat{x}_1 = \bar{x}_1 + x_3$ and using $\hat{x}_1$, x_2 & x_3 as semistate variables.)

Binary hysteresis is relatively easily realized and according to Soviet results [10] should be useful in obtaining other types of hysteresis. Nevertheless its mathematical descriptions are somewhat involved, at least when compared with some other types of hysteresis, for example that used in characterizing thermostats [13]. And another type of hytsteresis, that arising from a series connections of positive and negative nonlinear resistors [14], appears useful and is under investigation. One concludes that a unified theory of hysteresis still remains to be developed but that results in this direction are becoming available.

Acknowledgments

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