The Semistate Description of Nonlinear Time-Variable Circuits

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Abstract—**It is shown that, by the possible use of circuit equivalences, circuits satisfying rather light assumptions possess the semistate description**

$$\mathcal{A}\dot{x}+\mathcal{B}(x,t)=\mathcal{D}u$$
$$y=\mathcal{F}x$$

where u = input, y = output, x = semistate, and $\mathcal{A}$, $\mathcal{D}$, $\mathcal{F}$ are constant operators. The semistate can be chosen as tree branch voltages and link branch currents; a determination of consistent initial semistates is given which stems from a forward stepping solution equation. An appropriate reduction with attendant signal-flow graph for design is obtained in the linear time-invariant case.

I. Introduction

PRACTICAL INTEREST in integrated circuits (IC's) where the primary elements are truly nonlinear points out the importance of having a theory of nonlinear circuits relevant to IC realizations. To be sure, the past with its rich and varied history of nonlinear circuit analysis [1]–[4] has made important contributions, yet there are limitations which can be severe when practical IC's are considered. For example, present theories rely upon state-variable equations to describe the circuit dynamics, whereas circuits of interest may not possess a state-variable representation [5, p. 404]. Since the very first problem met in the analysis or design of a nonlinear circuit is that of what description to use, it is clear that it is necessary to have other than state-variable descriptions available in order to just begin some analyses or designs. Of course, if possible, one would like a more general description and a description which contains the state variable one as a special case when it exists. Such is the semistate description to be presented here.

The semistate equations can be put into the canonical form of the abstract above and arise very naturally through methods used in writing circuit equations, that is by combining the laws of the circuit elements through the laws of interconnection (Kirchhoff's current and voltage laws). The details of this formulation are given in Section III. But in order to achieve the canonical form, it is convenient to use some basic equivalences—these are given in Section II. Because arbitrary initial semistates can not be prescribed, it is important to know which are allowed, thus leading to the consideration in Section IV of consistent initial conditions. And, of course, in the case of linear time-invariant circuits we should be able to give complete solutions; for this purpose the previous results using the Drazin inverse [6] are known so Section V goes into other aspects. Finally, the concept of the semistate opens up many avenues for both practice and theory some of which are discussed in Section VI.

Manuscript received December 4, 1979; revised July 11, 1980.
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II. Circuit Equivalence

The key to getting a simple canonical form for the semistate equations is the use of several circuit equivalences. The equivalences of interest are of two types: the first uses gyrators to convert to admittance-type descriptions and the second places nonlinearities in resistive elements to allow the use of linear dynamics.

The gyrator has a rich history [7] but for our purposes, it is taken as the two-port described in admittance form by

$$\begin{bmatrix} 0 & g(t) \\ -g(t) & 0 \end{bmatrix}\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix}=\begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} \quad \text{(II-1)}$$

where $g(\cdot)$ is the gyration conductance; the circuit representation is that of Fig. 1. A main property of the gyrator is that it turns a one-port network N into its dual with respect to g, $N^d(g)$, defined by

$$[v^d,i^d]\in N^d(g) \Leftrightarrow i^d=gv,\ i=gv^d,\ [v,i]\in N. \quad \text{(II-2)}$$

The important equivalence is shown in Fig. 1(b). Fig. 2(a) shows the special result of loading port two of Fig. 1(b) by a short circuit, which then leads to the other equivalences of Fig. 2.

Fig. 3. shows two-port equivalences of importance to us. The first three parts show how to convert other than voltage-controlled current sources (VCCS) to VCCS's. Thus the current-controlled voltage source (CCVS) is seen in Fig. 3(c) to have the equivalent of the cascade of three two-ports each of which has an admittance type description, as seen by applying parts (a) and (b) of the figure. In terms of the equivalences given, others are readily obtained, as, for example, for n-port transformers or nonlinear coupled coils.

Through the equivalence of replacing inductors by capacitors, we can guarantee that on an admittance type basis all dynamics arise through derivative operators; no integrals need occur for finite circuits. If a nonlinear capacitor occurs, then the equivalence of Fig. 4 [8] shows how this in turn can be replaced by nonlinear resistive-type elements and a linear (unit) capacitor (even in the active

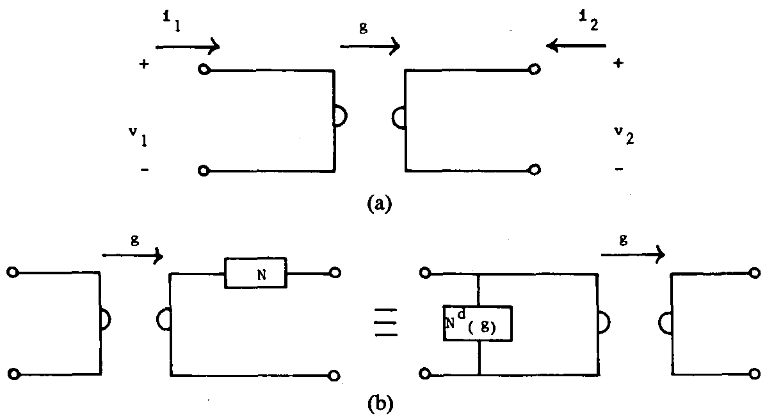

Fig. 1. (a) Gyrator. (b) Basic duality equivalence.

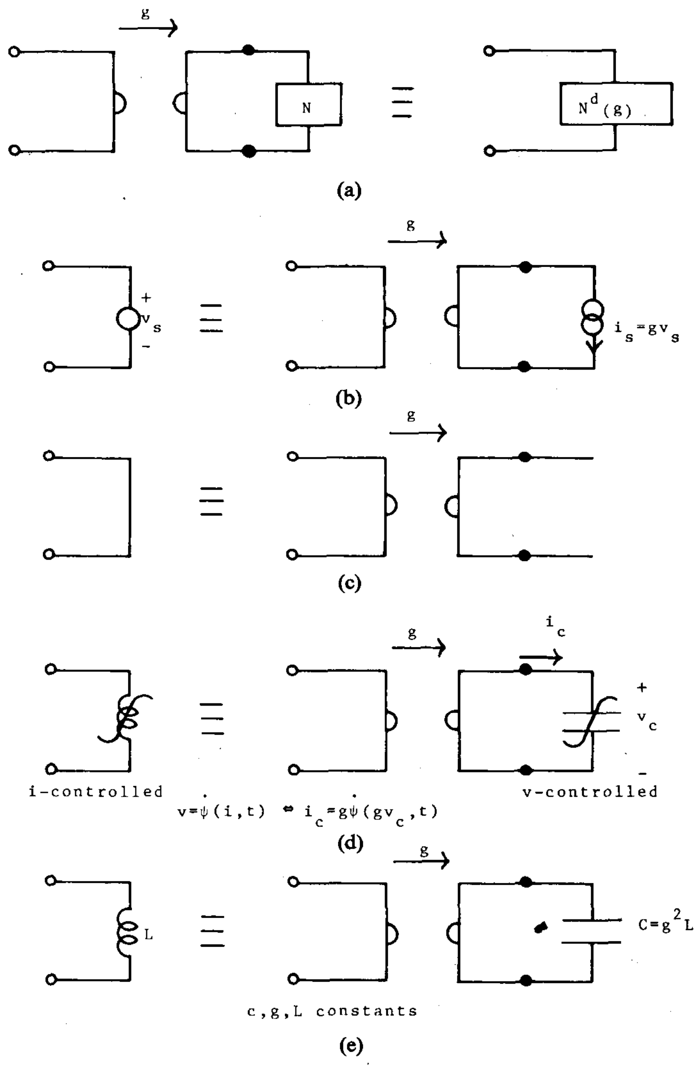

Fig. 2. (a) Basic one-port duality. Special Cases: (b) Voltage source replacement. (c) Short circuit replacement. (d) Current-controlled inductor replacement. (e) Time-invariant inductor replacement.

case). This results because

$$i=\dot{q}(v,t)=\frac{\partial q}{\partial t}+\frac{\partial q}{\partial v}\dot{v} \qquad \text{(II-3a)}$$

$$=\frac{\partial q}{\partial t}+[1-a(v,t)]i_c \qquad \text{(II-3b)}$$

where

$$a(v,t)=1-\frac{\partial q}{\partial v} \qquad \text{(II-3c)}$$

is a voltage dependent CCCS gain parameter; the CCCS is converted to a VCCS by Fig. 3(b).

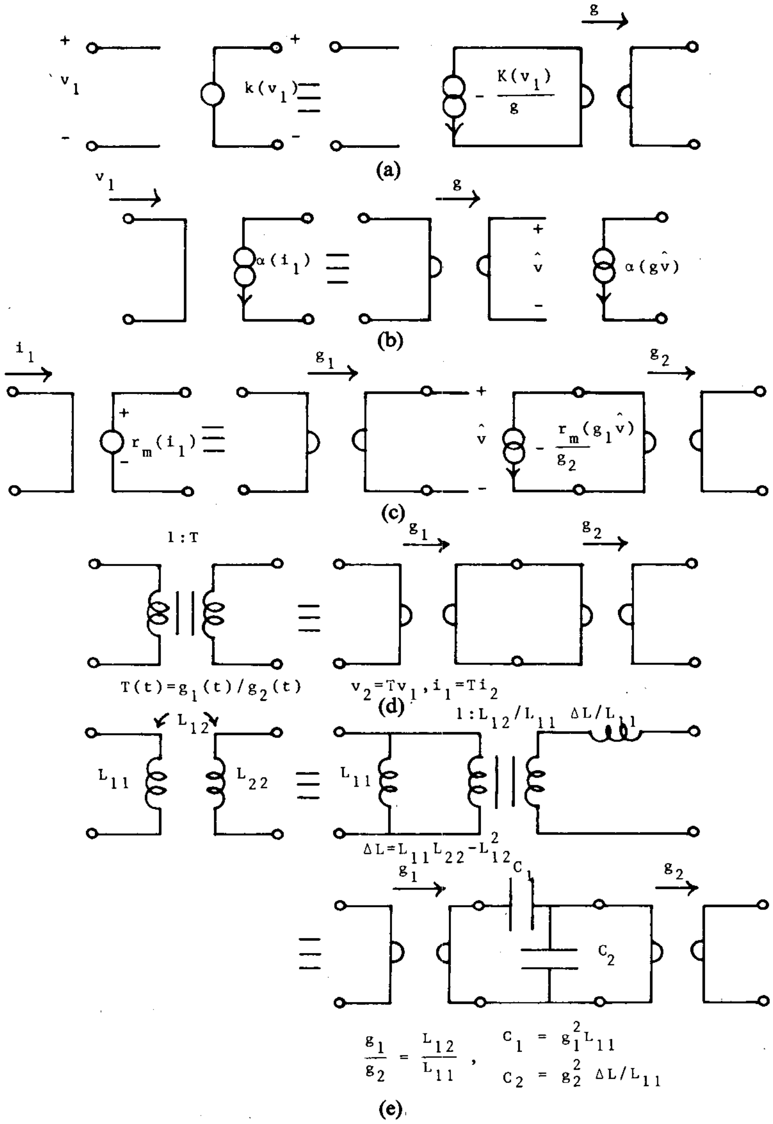

Fig. 3. Two-port equivalences. (a) VCVS. (b) CCCS. (c) CCVS. (d) Ideal linear transformer. (e) Time-invariant linear coupled coils.

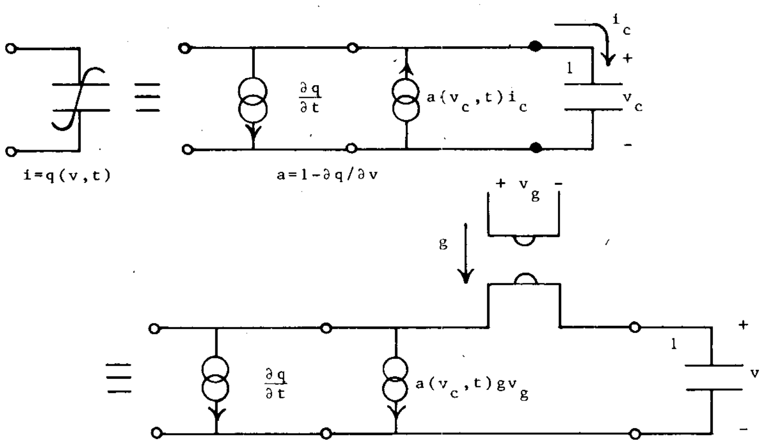

Fig. 4. Linear dynamics for nonlinear voltage-controlled capacitor.

Since, more often than not, active devices are incorporated in practical nonlinear circuits, we have need for useful equivalent circuits of these, as for example, those of operational amplifiers [5, p. 114], [9], bipolar [5, pp. 77, 100], [10], and MOS [11] transistors; and at times, the equivalents of other components become important, as for example, those of the nullator and norator in terms of gyrators and (positive and negative) resistors [12, p. 13] or

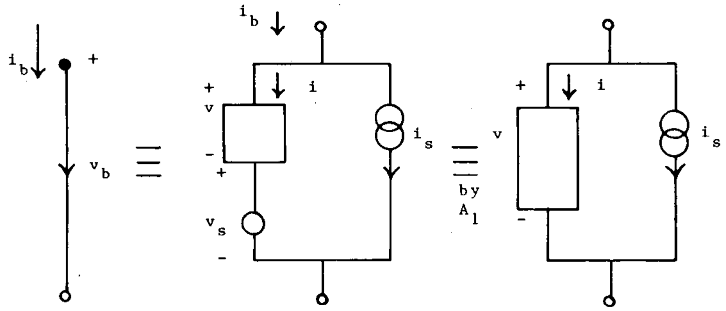

Fig. 5. General branch.

linear time-variable capacitors in terms of time-variable gyrators and fixed (positive and negative) capacitors and resistors [13]. The list grows with each new device and, consequently, only the most basic equivalents have been explicitly exhibited here.

III. The Semistate Equations

The desired canonical form for the semistate equations results by using an equivalent circuit in which all elements have an admittance type of description. By use of equivalences of the type of the last section we can generally arrive at this form of equivalent circuit. Consequently, it will now be assumed that we have on hand an equivalent circuit for which:

A_1) all input independent sources are current sources (see Fig. 2(b));

A_2) all controlled sources are VCCS's (see Fig. 3(a)–(c));

A_3) all dynamic elements are unit capacitors (see Figs. 2(d), 3(e), and (4);

A_4) all other components have admittance-type descriptions (see Figs. 2(c) and 3(d)).

It should be pointed out that there are practical circuits that are not known to have such an equivalent circuit, such as some circuits exhibiting hysteresis.

To finish our suppositions we assume that there are a finite number of components in the equivalent circuit and that the connections within it are fixed (that is, any switching is done through changes in the circuit elements). The (equivalent) circuit then has a (fixed) graph the branches of which can be taken of the form of Fig. 5 where independent current sources are placed across the ports of other elements (which may be open circuits). If there are b such branches we have the b-vector equations

$$i_b = i_s + i \qquad \text{(III-1a)}$$

$$v_b = v_s + v = v, \qquad v_s \equiv 0 \qquad \text{(III-1b)}$$

while if v_t and i_l are the t-vector of tree branch voltages and the l-vector of link currents then

$$v_b = \tilde{\mathcal{C}} v_t \qquad \text{(III-2a)}$$

$$i_b = \tilde{\mathcal{T}} i_l \qquad \text{(III-2b)}$$

where $\mathcal{C}$ is the cut-set matrix, $\mathcal{T}$ is the tie-set matrix and $\tilde{}$ denotes matrix transpose.

By (III-2) any voltages and currents, or linear combinations of them, in the circuit can be expressed as linear combinations of the tree branch voltages and link currents. In particular this will be true of output quantities y in which case we have

$$y = \mathcal{F}\begin{bmatrix} v_t \\ i_l \end{bmatrix} \qquad \text{(III-3)}$$

for some constant matrix $\mathcal{F}$.

Equations (III-1)–(III-3) are Kirchhoff's laws which are completed by the laws of the circuit elements. These we write, by our assumption of admittance type descriptions, as

$$i = \mathcal{Y}_b(p, t, v) \qquad \text{(III-4)}$$

where $p = d/dt$ is the derivative operator. Here $\mathcal{Y}_b(\cdot,\cdot,\cdot)$ is the branch by branch admittance operator, which in fact is allowed to be multiple valued.

Now, if there are c capacitors, all assumed of unit capacitance by assumption A_3), we are free to put these (as a convenience) in the first c branches. Letting 1_c denote the $c \times c$ identity, 0_{b-c} the $(b-c)\times(b-c)$ zero, and $\dotplus$ the direct sum, we can express the branch by branch admittance operator as

$$\mathcal{Y}_b(p, t, v) = p[1_c \dotplus 0_{b-c}]v + \mathcal{Y}_G(t, v) \qquad \text{(III.5)}$$

where $\mathcal{Y}_G$ is the (branch-by-branch) conductance operator describing the noncapacitor, noninput source elements (it may have zeros in the capacitive branch positions). Combining all equations, except (III-3), so far stated in this section:

$$\mathcal{T} i_l = i_s + p(1_c \dotplus 0_{b-c})\tilde{\mathcal{C}} v_t + \mathcal{Y}_G(t, \tilde{\mathcal{C}} v_t). \qquad \text{(III.6a)}$$

Two of the terms in (III-6a) can be written as

$$p(1_c \dotplus 0_{b-c})\tilde{\mathcal{C}} v_t - \tilde{\mathcal{T}} i_l = \left[p(1_c \dotplus 0_{b-c})\tilde{\mathcal{C}}, -\tilde{\mathcal{T}}\right]\begin{bmatrix} v_t \\ i_l \end{bmatrix}. \qquad \text{(III-6b)}$$

Further, we can take the nonzero entries of i_s as the inputs (that is, entries of the input vector u), and, thus we can write

$$i_s = -\mathcal{D} u \qquad \text{(III-6c)}$$

for some constant matrix $\mathcal{D}$. Combining the (III-6) equa-

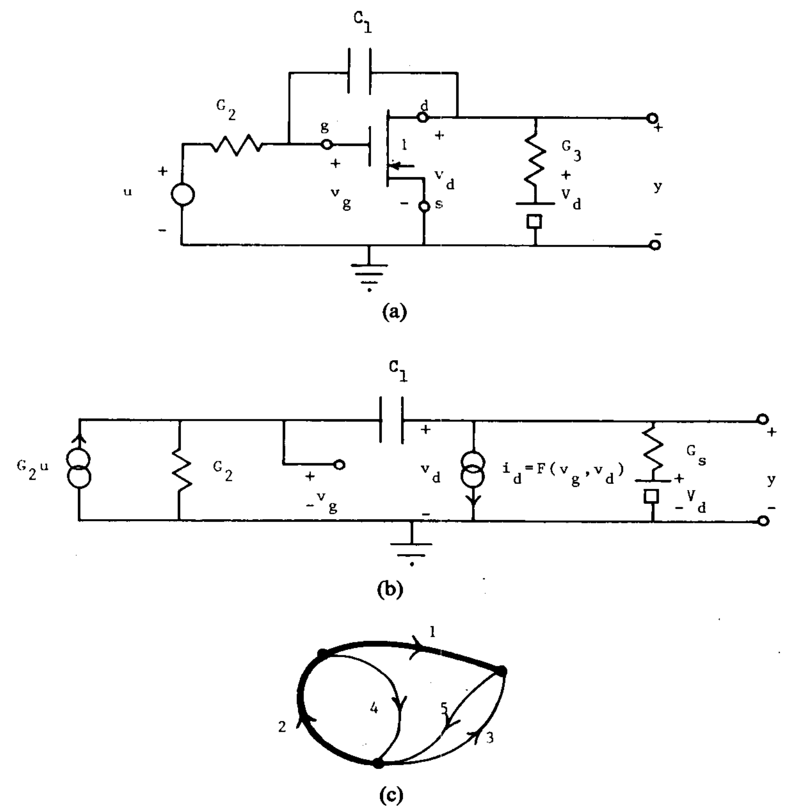

Fig. 6. (a) MOS example circuit with (b) equivalent and (c) graph.

tions and adjoining the output equation, (III-3), gives

$$\mathcal{A}\dot{x}+\mathcal{B}(x,t)=\mathcal{D}u \qquad \text{(III-7a)}$$

$$y=\mathcal{F}x \qquad \text{(III-7b)}$$

where

$$x=\begin{bmatrix} v_t \\ i_l \end{bmatrix}=\text{semistate} \qquad \text{(III.8a)}$$

$$\mathcal{A}=\left[(1_c\dot{+}0_{b-c})\tilde{\mathcal{C}},0_{b\times l}\right] \qquad \text{(III.8b)}$$

$$\mathcal{B}(x,t)=\left[0_{b\times t},-\tilde{\mathcal{T}}\right]x+\mathcal{Y}_G\left(t,\left[\tilde{\mathcal{C}},0_{b\times l}\right]x\right) \qquad \text{(III.8c)}$$

with $0_{b\times l}$ being the b-by-l zero matrix and $\dot{}$ denoting time differentiation. It should be noted that $\mathcal{A}$ is a constant $b\times b$ matrix of rank c and that in the case of time-invariant circuit elements the (algebraic) operator $\mathcal{B}$ is independent of t, $\mathcal{B}(x,t)=\mathcal{B}(x,0)$. Equation (III-8) are one of many possibilities and, hence, we will call any set of equations of the form of (III-7) (with possibly functionals of u added on the right-hand sides) which completely represent a circuit a set of *semistate equations* for the circuit; those in the exact form of (III-7) will be called *canonical*.

Example III-1:

Consider the MOS amplifier of Fig. 6(a) which has the appropriate equivalent circuit of Fig. 6(b), for which Norton's Theorem has been used. It will be assumed that the transistor is described by [11]

$$i_d=F(v_g,v_d)$$
$$=\left[f(v_2-V_T)-f(v_g-v_d-V_T)\right](1+l|v_d|)$$

$$f(z)=Kz^2 1(z)$$

where $1(\cdot)$ is the unit step function and K, V_T, and l are transistor (gain, turn-on, and channel-length modulation) constants. The circuit graph is specified in Fig. 6(c) where the tree is taken (for convenience) as branches 1 and 2. We have by inspection

$$\tilde{v}_t=[v_1,v_2] \quad \tilde{i}_l=[i_3,i_4,i_5]_b$$

$$\tilde{i}_s=[0,G_2u,0,0,0]$$

$$\mathcal{C}=\begin{bmatrix} 1 & 0 & 1 & 0 & -1 \\ 0 & 1 & 1 & -1 & -1 \end{bmatrix}$$

$$\mathcal{T}=\begin{bmatrix} -1 & -1 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix}=\begin{bmatrix} C_1pv_1 \\ G_2v_2 \\ G_3(v_3-V_d) \\ 0 \\ F(v_4,v_5) \end{bmatrix} \quad i_s=\begin{bmatrix} 0 \\ G_2 \\ 0 \\ 0 \\ 0 \end{bmatrix}u$$

$$x=\begin{bmatrix} v_1 \\ v_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix}_b \quad y=[-1,-1,0,0,0]x.$$

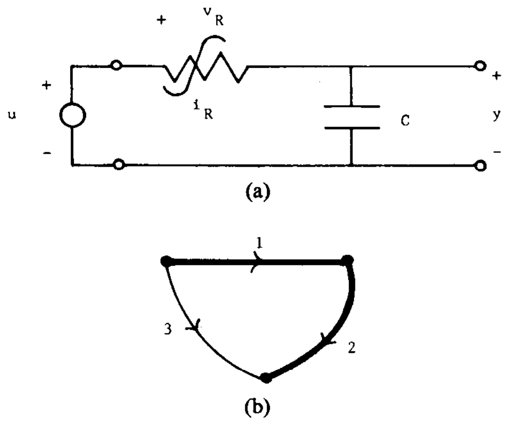

Fig. 7. (a) Circuit with semistate but no state equations. (b) Graph.

The semistate equations are then, by (III-7), (III-8)

$$\begin{bmatrix} C_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \dot{x} + \begin{bmatrix} x_3 - x_5 \\ G_2 x_2 + x_3 - x_4 - x_5 \\ G_3(x_1 + x_2 - V_d) - x_3 \\ -x_4 \\ F(-x_2, -x_1 - x_2) - x_5 \end{bmatrix} = \begin{bmatrix} 0 \\ G_2 \\ 0 \\ 0 \\ 0 \end{bmatrix} u$$

$$y = [-1, -1, 0, 0, 0]x.$$

Example III-2:

Consider the circuit of Fig. 7(a) which has been proven to have no state equations [5, p. 404] when

$$v_R = -3i_R + i_R^3.$$

Using the graph of Fig. 7(b) we have

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} -1 \\ -1 \\ 1 \end{bmatrix} [i_3]$$

$$x = \begin{bmatrix} v_1 \\ v_2 \\ i_3 \end{bmatrix} \qquad y = v_2$$

$$pCv_2 = -i_3$$

$$u = v_1 + v_2$$

$$v_1 - (+3i_3 - i_3^3) = 0.$$

Semistate equations are then

$$\begin{bmatrix} 0 & C & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \dot{x} + \left(\begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & -3 \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \\ x_3^3 \end{bmatrix} \right) = \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} u$$

$$y = [0, 1, 0]x.$$

We conclude that semistate equations will exist when state variable ones may not, while, if $\mathcal{A}$ is nonsingular at (III-7a), the state-variable equations are special cases of semistate ones. It is also of interest to reduce the semistate equations to state-variable form. This is a matter of diagonalizing $\mathcal{A}$, $\mathcal{A} = 1_r \dotplus 0_{b-r}$, and then eliminating variables ($b-r$ variables from the last $b-r$ equations when $\mathcal{A} = 1_r \dotplus 0_{b-r}$); as shown by Example III-2, this elimination may not always be possible.

IV. Consistent Initial Conditions—Solution Formulation

Because the coefficient matrix $\mathcal{A}$ of $\dot{x}$ in the semistate equation may be singular, the semistate equations need not allow all possible initial conditions. Those which are allowed we call consistent. More precisely, x_0 is a *consistent* initial semistate at $t = t_0$ if there exists a semistate $x(t)$, for t near t_0, such that

$$x(t_0) = x_0 = \lim_{0 < \delta t \to 0} x(t_0 + \Delta t). \qquad \text{(IV-1)}$$

In obtaining the constraint on given initial conditions x_0 we will also obtain a means for solution of the semistate equations.

The details are somewhat messy but to pursue the consistency constraint on x_0 we write

$$\dot{x} = \lim_{\Delta t \to 0} \frac{x(t + \Delta t) - x(t)}{\Delta t} \qquad \text{(IV-2a)}$$

and expand $\mathcal{B}$ in a Taylor series expansion

$$\mathcal{B}(x, t)|_{t = t_0 + \Delta t} = \mathcal{B}_0 + \left(\frac{\partial \mathcal{B}}{\partial t} \right)_0 \Delta t + (\nabla_x \mathcal{B})_0 (x(t_0 + \Delta t) - x(t_0)) + \cdots \qquad \text{(IV-2b)}$$

where the subscript zero denotes evaluation at $t = t_0$ and ∇_x is the vector gradient (hence, ∇_x is a $b \times b$ matrix). These expressions we set into the dynamic portion of the semistate equations, (III-7a), evaluated at $t = t_0$. Combining multiples of $x(t_0 + \Delta t)$ gives

$$x(t_0 + \Delta t) = [\mathcal{A} + (\nabla_x \mathcal{B})_0 \Delta t]^{-1} \{ [\mathcal{A} + (\nabla_x \mathcal{B})_0 \Delta t] x(t_0) + (\mathcal{D} u_0 - \mathcal{B}_0) \Delta t + \cdots \}. \qquad \text{(IV-3)}$$

Next we apply (IV-1) to (IV-3); thus

$$x_0 = \lim_{0 < \Delta t \to 0} \{ [\mathcal{A} + (\nabla_x \mathcal{B})_0 \Delta t]^{-1} [(\mathcal{A} + (\nabla_x \mathcal{B})_0 \Delta t) x_0 + (\mathcal{D} u_0 - \mathcal{B}_0) \Delta t + \cdots] \} \qquad \text{(IV-4)}$$

where now the subscript zero means evaluation at $x = x_0$, $t = t_0$. We conclude that in order for x_0 to be an allowed initial semistate it should satisfy the constraint of (IV-4). Because $[\mathcal{A} + (\nabla \mathcal{B})_0 \Delta t]^{-1}$ may have poles in Δt at zero, more than just the first-order terms in Δt on the right of (IV-4) may be needed to accurately determine the consistency of x_0.

In the case of linear time-invariant (LTI) circuits a more explicit evaluation can be made since $\mathcal{B}(x, t) = \mathcal{B} \cdot x$ with $\mathcal{B}$ a constant $b \times b$ matrix. Then $\mathcal{B}_0 = \mathcal{B} \cdot x_0$, $(\nabla_x \mathcal{B})_0 = \mathcal{B}$ in which case two of the x_0 terms written in

(IV-4) cancel; since there are no higher order terms, the constraint is

$$\lim_{0<\Delta t \to 0} \left\{ \left(1_b - [\mathcal{A}+\mathcal{B}\Delta t]^{-1}\mathcal{A}\right)x_0 - [\mathcal{A}+\mathcal{B}\Delta t]^{-1}\mathcal{D}u(t_0)\Delta t \right\} = 0. \quad \binom{\text{LTI}}{\text{case}} \quad \text{(IV-5)}$$

In the zero input situation we then see that x_0 must lie in the null space of $1_b - [\mathcal{A}+\mathcal{B}\Delta t]^{-1}\mathcal{A}$. Also it is seen that necessarily $[\mathcal{A}+\mathcal{B}\Delta t]$ is nonsingular for small nonzero Δt, a condition known to be needed to guarantee uniqueness of solutions [14, p. 418]

If we have on hand consistent initial conditions we see that (IV-3) directly gives a means for the computer aided solution of the semistate equations, for which it is seen necessary that $[\mathcal{A}+(\nabla_x\mathcal{B})_0\Delta t]$ be nonsingular. Assuming this nonsingularity one then has a wealth of material available to aid in obtaining a solution [5]. Consequently our examples for this section concern only initial conditions.

Example IV-1:

We return to Example III-2 where

$$\nabla_x\mathcal{B} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 3(x_3^2-1) \end{bmatrix}$$

$$\mathcal{B}_0 = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & -3 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}_0 + \begin{bmatrix} 0 \\ 0 \\ x_{30}^3 \end{bmatrix}.$$

The right-hand side of (IV-4) is

$$\begin{bmatrix} 0 & C & \Delta t \\ \Delta t & \Delta t & 0 \\ \Delta t & 0 & 3(x_{30}^2-1)\Delta t \end{bmatrix}^{-1} \cdot \begin{bmatrix} Cx_{20} \\ u_0\Delta t \\ 2x_{30}^3\Delta t \end{bmatrix}$$

$$= \frac{-1}{\Delta t^2[3C(x_{30}^2-1)+\Delta t]} \cdot \begin{bmatrix} 3\Delta t^2C(x_{30}^2-1)(x_{20}-u_0)-2x_{30}^3\Delta t^3 \\ -3\Delta t^2C(x_{30}^2-1)x_{20}-2x_{30}^3\Delta t^3+u_0\Delta t^3 \\ -\Delta t^2Cx_{20}-2Cx_{30}^3\Delta t^2+Cu_0\Delta t^2 \end{bmatrix}.$$

Taking the limit in Δt gives, for (IV-4),

$$\begin{bmatrix} x_{10} \\ x_{20} \\ x_{30} \end{bmatrix} = \begin{bmatrix} u_0 - x_{20} \\ x_{20} \\ [(x_{20}-u_0)+2x_{30}^3]/3(x_{30}^2-1) \end{bmatrix}.$$

The last of these is $x_{30}^3 - 3x_{30} = -x_{10}$ which is seen by inspection of the circuit to be the voltage on the nonlinear resistor (recall that $i_3 = -i_1$). Thus we have consistent initial conditions as: x_{20} = arbitrary, $x_{10} = 3x_{30} - x_{30}^3 = u_0 - x_{20}$ (note that this holds also when $x_{30}^2 = 1$ for which the x_{30} equation of the vector equation above is verified by L'Hospital's rule).

Example IV-2:

As an LTI example we consider the circuit of Fig. 8 which has a capacitive loop. The dynamical semistate equations can be written as

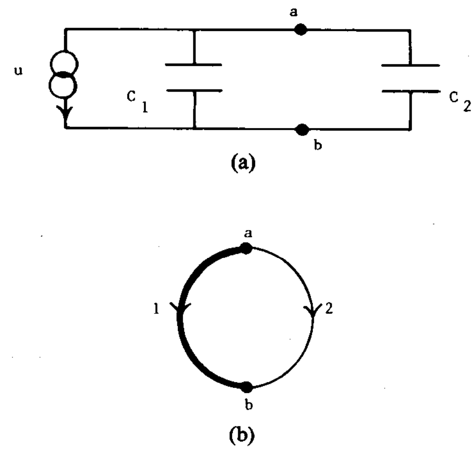

Fig. 8. Capacitive loop example circuit.

$$\begin{bmatrix} C_1 & 0 \\ C_2 & 0 \end{bmatrix}\dot{x} + \begin{bmatrix} 0 & 1 \\ 0 & -1 \end{bmatrix}x = \begin{bmatrix} -1 \\ 0 \end{bmatrix}u$$

$$x = \begin{bmatrix} v_1 \\ i_2 \end{bmatrix}_b.$$

Then

$$\mathcal{A}+\mathcal{B}\Delta t = \begin{bmatrix} C_1 & \Delta t \\ C_2 & -\Delta t \end{bmatrix}$$

and in the zero input case (IV-5) is

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \left\{ \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} + \frac{1}{\Delta t\,(C_1+C_2)} \cdot \begin{bmatrix} -\Delta t(C_1+C_2) & 0 \\ C_1C_2 - C_1C_2 & 0 \end{bmatrix} \right\} \begin{bmatrix} x_{10} \\ x_{20} \end{bmatrix}$$

$$= \begin{bmatrix} 0 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x_{10} \\ x_{20} \end{bmatrix}$$

or x_{10} = arbitrary, $x_{20} = 0$. Thus with no input, any voltage can be placed across the capacitors and no current will flow.

It is of interest to consider nonconsistent initial conditions [15]. Equation (IV-3) is the one to look at where we see that if $x_0 = x(t_0)$ is not consistent then $x(t_0+)$ will not equal $x(t_0)$ in which case impulsive behavior would occur in $\dot{x}$, though not necessarily in x. Thus in the last example we have for any x_0

$$x(t_0+\Delta t) = [\mathcal{A}+\mathcal{B}\Delta t]^{-1}\mathcal{A}x_0 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}x_0 = \begin{bmatrix} x_{10} \\ 0 \end{bmatrix}$$

irrespective of x_{20}.

V. Linear Time-Invariant Circuits

As concerns linear time-invariant circuits the theory of analysis is rather complete and available elsewhere [6]. In particular the use of the Drazin inverse yields solutions directly in the time domain. Rather than repeat what is available, only the transfer function and reduction to state-variable equations will be touched upon here.

For linear time-invariant circuits the canonical semistate equations take the form

$$\mathcal{A}\dot{x}+\mathcal{B}x=\mathcal{D}u \tag{V-1a}$$

$$y=\mathcal{F}x \tag{V-1b}$$

where $\mathcal{B}$, as well as all coefficient matrices, is a constant matrix. An equivalent system of semistate equations is found by multiplying (V-1a) by a nonsingular matrix P and transforming the semistate by a nonsingular matrix Q, to get

$$\bar{\mathcal{A}}\dot{\bar{x}}+\bar{\mathcal{B}}\bar{x}=\bar{\mathcal{D}}u \tag{V-2a}$$

$$y=\bar{\mathcal{F}}\bar{x} \tag{V-2b}$$

with

$$x=Q\bar{x} \tag{V-2c}$$

$$\bar{\mathcal{A}}=P\mathcal{A}Q \quad \bar{\mathcal{B}}=P\mathcal{B}Q$$

$$\bar{\mathcal{D}}=P\mathcal{D} \quad \bar{\mathcal{F}}=\mathcal{F}Q. \tag{V-2d}$$

Taking (bilateral) Laplace transforms of (V-1) gives

$$[\mathcal{A}s+\mathcal{B}]\mathcal{L}[x]=\mathcal{D}\mathcal{L}[u] \tag{V-3a}$$

$$\mathcal{L}[y]=\mathcal{F}\mathcal{L}[x] \tag{V-3b}$$

from which we see that two equivalent semistate descriptions (of the same dimension, b) are related by

$$\bar{\mathcal{A}}s+\bar{\mathcal{B}}=P[\mathcal{A}s+\mathcal{B}]Q. \tag{V-4}$$

Such are called equivalent pencils and are well studied in the mathematical literature where canonical forms can be found [16, p. 37]. Thus if $\mathcal{A}$ has rank c then it can be diagonalized to $1_c \dotplus 0_{b-c}$, following which the lower right $(b-c)\times(b-c)$ submatrix of (the transformed) $\mathcal{B}$ can be diagonalized to $0_{b-c-a}\dotplus 1_a$ where a is its rank. The resulting 1_a in $\mathcal{B}$ can be used to get zeros in all other positions of the last a rows and columns; we achieve

$$\bar{\mathcal{A}}s+\bar{\mathcal{B}}=\left[\begin{array}{c|c|c} s1_c & & \\ \hline & 0_{b-c-a} & \\ \hline & & 0_a \end{array}\right]+\left[\begin{array}{c|c|c} \bar{\mathcal{B}}_{11} & \bar{\mathcal{B}}_{12} & \\ \hline \bar{\mathcal{B}}_{21} & 0_{b-c-a} & \\ \hline & & 1_a \end{array}\right]. \tag{V-5}$$

Further, in (V-5) the symmetric part of $\bar{\mathcal{B}}_{11}$ can be diagonalized by an orthogonal congruency transformation while $\bar{\mathcal{B}}_{21}$ and $\bar{\mathcal{B}}_{12}$ can then be made upper and lower triangular respectively. In the linear time-invariant case we have just seen that we can transform the semistate equations to the form (where the $\bar{\ }$ has been dropped for simplicity of notation)

$$\begin{bmatrix} p1_c+\mathcal{B}_{11} & \mathcal{B}_{12} & 0 \\ \mathcal{B}_{21} & 0 & 0 \\ 0 & 0 & 1_a \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}=\begin{bmatrix} \mathcal{D}_1 \\ \mathcal{D}_2 \\ \mathcal{D}_3 \end{bmatrix}u \tag{V-6a}$$

$$y=[\mathcal{F}_1,\mathcal{F}_2,\mathcal{F}_3]\begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix}. \tag{V-6b}$$

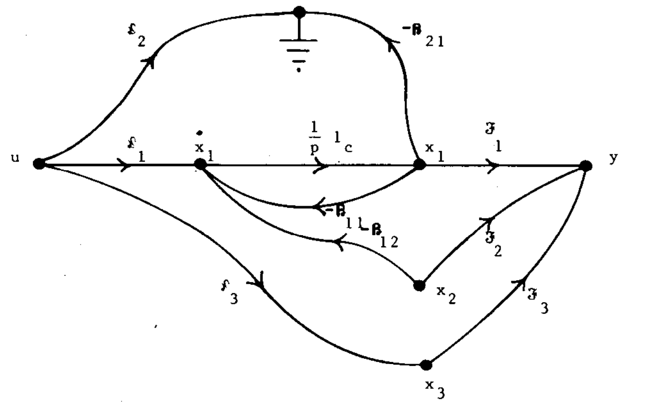

Fig. 9. Signal-flow graph for canonical linear time-invariant semistate equations.

where the semistate has been partitioned according to the partition of $\mathcal{A}s+\mathcal{B}$, and $\mathcal{B}_{11}$, $\mathcal{B}_{12}$, and $\mathcal{B}_{21}$ may have the form just mentioned. Fig. 9 gives a "signal-flow graph" configuration of this canonical form where the ground represents a forced constraint to zero (realized by grounding the output of an op amp, say). Clearly, if $b-c=a$ then (V-6) reduces to the classical state-variable equations written as

$$(p1_c+\mathcal{B}_{11})x_1=\mathcal{D}_1u \tag{V-7a}$$

$$y=\mathcal{F}_1x_1+\mathcal{F}_3\mathcal{D}_3u. \tag{V-7b}$$

If the pencil $\mathcal{A}s+\mathcal{B}$ is nonsingular then the transfer function $T(s)$, $\mathcal{L}[y]=T(s)\mathcal{L}[u]$, follows directly from (V-3)

$$T(s)=\mathcal{F}[\mathcal{A}s+\mathcal{B}]^{-1}\mathcal{D} \tag{V-8}$$

and this has the same form for all pencils equivalent to $\mathcal{A}s+\mathcal{B}$. When the rank c of $\mathcal{A}$ is less than its size, b, then $T(s)$ may achieve poles at infinity as a result of the "infinite" elementary divisors of the pencil [16, p. 27]. This is perhaps most clearly illustrated by the simple example to follow. But first it is noted that in the case where $[\mathcal{A}s+\mathcal{B}]$ is singular the transfer function may still exist if in transforming to an equivalent pencil the transformed input and output matrices, $\bar{\mathcal{D}}$ and $\bar{\mathcal{F}}$, have appropriate zeros.

Example V-1:

Using the simplest applicable equivalent circuit of the transistor, Fig. 10(a), through the equivalent circuit of part (b) of the figure, has the semistate equations

$$\begin{bmatrix} C & 0 \\ 0 & 0 \end{bmatrix}\dot{x}+\begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix}x=\begin{bmatrix} 0 \\ 1 \end{bmatrix}u \quad x=\begin{bmatrix} v_c \\ i_E \end{bmatrix}$$

$$y=[0,\alpha R]x.$$

Then

$$[\mathcal{A}s+\mathcal{B}]^{-1}=\begin{bmatrix} Cs & -1 \\ -1 & 0 \end{bmatrix}^{-1}=\begin{bmatrix} 0 & -1 \\ -1 & -Cs \end{bmatrix}$$

and the transfer function is

$$T(s)=-\alpha RCs=[0,\alpha R]\begin{bmatrix} 0 & -1 \\ -1 & -Cs \end{bmatrix}\begin{bmatrix} 0 \\ 1 \end{bmatrix}.$$

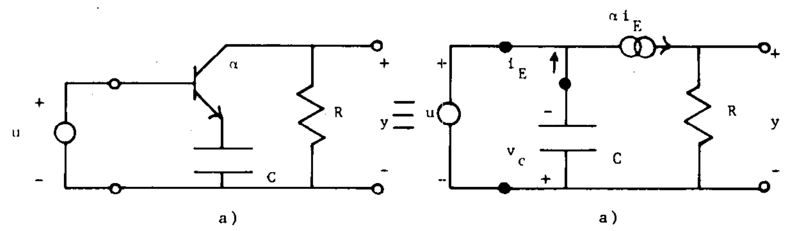

Fig. 10. Circuit for $T(s)$ with pole at infinity.

It is of interest to investigate the consistent initial condition constraint for this example. From (IV-5) we have, for $t_0 = 0$,

$$\lim_{0<\Delta\to 0}\left\{\begin{bmatrix} x_{10} \\ \frac{C}{\Delta t}x_{10}+x_{20}\end{bmatrix}+\begin{bmatrix} u(0) \\ \frac{Cu(0)}{\Delta t}\end{bmatrix}\right\}=0$$

which requires $x_{10}=v_c(0)=-u(0)$, $x_{20}=i_E(0)=0$. It should be observed that, on taking the (unilateral) Laplace transform of the semistate equations,

$$\begin{bmatrix} X_1(s) \\ X_2(s)\end{bmatrix}=\begin{bmatrix} 0 & 1 \\ -1 & -Cs\end{bmatrix}\cdot\begin{bmatrix} Cx_1(0-) \\ U(s)\end{bmatrix}$$

showing that $x_2(0_+)\neq 0$ results from $v_c(0_-)\neq -u(0)$ in which case an impulse is present, negating the meaning of consistency embodied in (IV-1) (where we could read $x_0 = x(t_0-)$).

VI. Discussion

Semistate theory has been shown here to be a natural for the analysis of circuits since the semistate equations result directly from Kirchhoff's and element laws if the tree branch voltages and link currents are chosen to form the semistate. But these are not the only variables which may be chosen, as is concretely exhibited by Example V-1. Still, in setting up the canonical form of the semistate equations it may be necessary to revert to an equivalent circuit through equivalences of the type given in Section II whose use guarantees linear constant transformations on three terms (the derivative of the semistate, the input, and the semistate in the output equation). Of course the use of the equivalences makes for larger dimension semistates, as for example each gyrator inserted means two more branches in the circuit graph and two more components in the semistate. But it is seen that a very large class of circuits fall into those describable by semistate equations, including many nonlinear and time-variable ones. In the formulation given here emphasis has been placed upon admittance type of formulations where all dynamics is placed in capacitors, this because of the practical importance of such for integrated circuits. But it should be clear that other formulations are equally possible, for example, impedance type of descriptions by duality or any hybrid type. Too, the class of unicursal circuits [17] naturally fits into the description and, hence, unicursal types of hysteresis are covered. But unfortunately the more practical types of hysteresis simply obtainable from MOS amplifiers have not yet been fit in, nor have diodes such as described by $i=(i+v)1(i)$. In any event state-variable descriptions are essentially special cases where $\mathcal{E}=1_b$, and, whenever state-variable equations exist, they can be derived from the semistate ones.

As with all nonlinear differential equations the general semistate equations are not easy to solve. But (IV-3) gives an equation of promise for computer-aided analysis on which to begin studies by stepping the solution forward by small steps Δt. Beyond that, though, the semistate equations have the particularly nice property that the input is isolated in a term appearing linearly in the dynamical equations. Consequently, some of the more powerful results on undriven nonlinear differential equations seem possible to extend to driven ones particularly in obtaining canonical square-law systems amenable to algebraic techniques [18] or equivalent linear ones [19]. In any event, through (IV-3) we are able, in (IV-4), to obtain the initial conditions permissible for obtaining solutions (right continuous at the initial time). In the linear time-invariant situation complete solutions have previously been given through the use of the Drazin inverse, and, hence, other aspects have been discussed here. Still other aspects, such as stability, in a somewhat different, but similar, framework can be found in the creative work of Rosenbrock [20]. It should be commented, though, that (IV-5) for consistency of x_0 differs in form from the one used with the Drazin inverse theory but has always numerically yielded the same results; a direct proof of the equivalence would be welcomed. An alternate formulation following the Drazin inverse type theory is under development by Campbell [21], while his book [22] gives relevant comments on calculations.

One of the distinct advantages of state-variable theory is its direct use in design, for example the setting up of a system through a signal-flow graph incorporating integrators. For the field of electronic and integrated circuits this has led to revolutionary designs [23], [24, ch. 8]. Consequently, one could hope for similar breakthroughs by the use of semistate variables, a first step toward which is given in Fig. 9.

Finally it should be commented that undoubtedly many other classes of systems, besides electrical circuits, should be subject to semistate equations. Consequently, a general mathematical treatment of canonical semistate equations and their systems seems well in order.

Acknowledgment–Dedication

It was during a visit to Sopot, Poland, that discussions with B. Dziurla, who suggested the name "semistate," led to our developments of these ideas. As one of the author's favorite cities Sopot holds a beauty which is as all-pervading as the semistate theory—to this the work is dedicated. The interest and assistance in improvement of S. Campbell, T. Dwyer, and J. Stokes and the figure drafting of G. Cribb, is also gratefully acknowledged.

Sopot is a tourist town—innumerable cafes await custom. In Oliwa—the westernmost district of Gdańsk, adjacent to Sopot—a must for all who visit: the Cathedral with its park. [25, pp. 96, 97, 103].

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